



PSMN013-100PS

N-channel 100V 13.9mΩ standard level MOSFET in TO220.

10 August 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in TO220 package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Improved dynamic avalanche performance
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}$; $T_j \leq 175 \text{ }^\circ\text{C}$		-	-	100	V
I_D	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$; Fig. 1	[1]	-	-	68	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 2		-	-	170	W
T_j	junction temperature			-55	-	175	$^\circ\text{C}$
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 100 \text{ }^\circ\text{C}$; Fig. 12		-	19.4	25	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 13	[2]	-	10.8	13.9	$\text{m}\Omega$
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; Fig. 15 ; Fig. 14		-	17	-	nC

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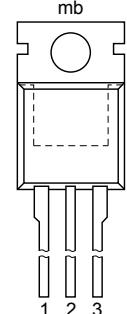
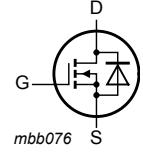
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 10 \text{ V}$; $I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; Fig. 14 ; Fig. 15		-	59	-	nC
Avalanche ruggedness							
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $I_D = 68 \text{ A}$; $V_{\text{sup}} \leq 100 \text{ V}$; unclamped; $R_{GS} = 50 \Omega$		-	-	128	mJ

[1] Continuous current is limited by package

[2] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain	 TO-220AB (SOT78)	

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN013-100PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-100PS	PSMN013-100PS

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$		-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175^\circ\text{C}$; $T_j \geq 25^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100^\circ\text{C}$; Fig. 1	[1]	-	47	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25^\circ\text{C}$; Fig. 1	[1]	-	68	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$; Fig. 3		-	272	A
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 2		-	170	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25^\circ\text{C}$	[1]	-	68	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$		-	272	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25^\circ\text{C}$; $I_D = 68\text{ A}$; $V_{sup} \leq 100\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$		-	128	mJ

[1] Continuous current is limited by package

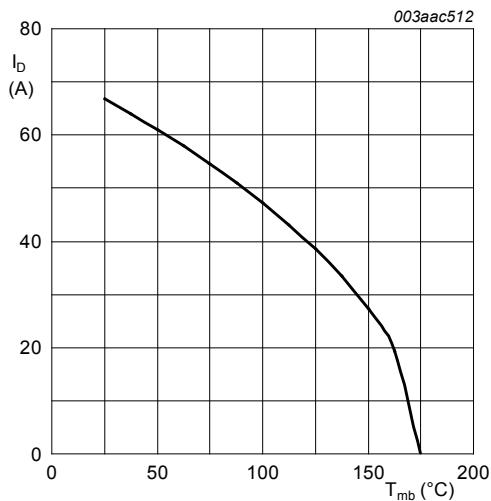


Fig. 1. Continuous drain current as a function of mounting base temperature

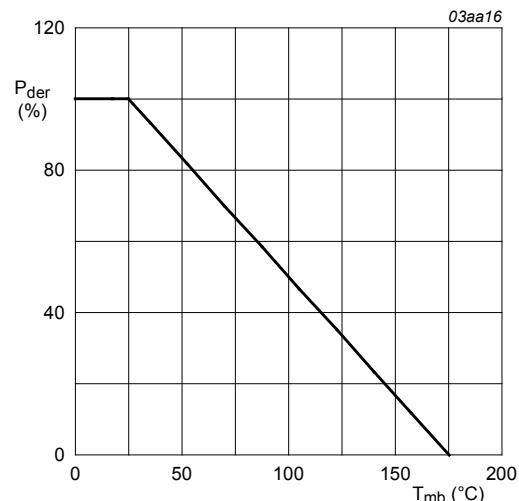


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$

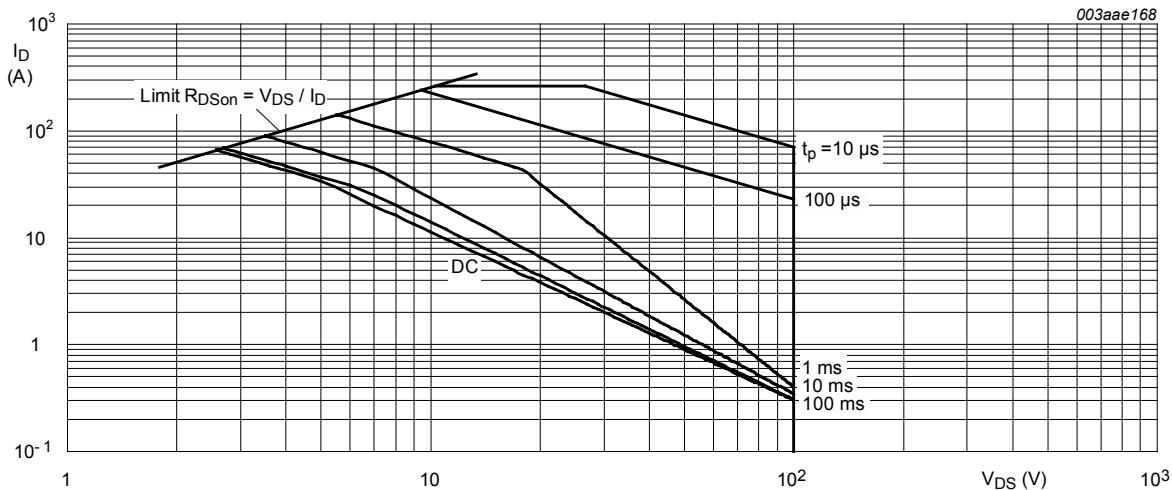


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

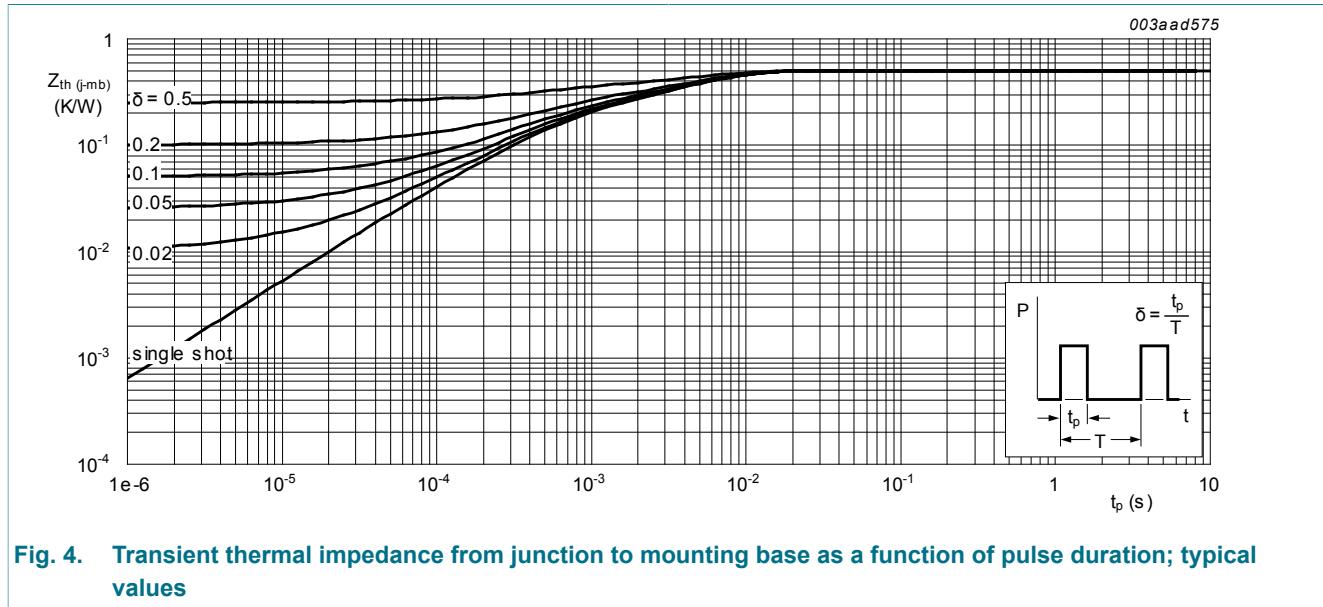
$T_{mb} = 25^\circ\text{C}$; I_{DM} is a single pulse

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.5	0.9	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air		-	60	-	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$		90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10		1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11		2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 10		-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$		-	-	100	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	0.06	2	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ Fig. 12		-	19.4	25	$\text{m}\Omega$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 175 \text{ }^\circ\text{C}$; Fig. 12		-	29.5	38.9	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 13					
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$		-	1	-	Ω
Dynamic characteristics							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15		-	59	-	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 10 \text{ V}$					
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15		-	13.8	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 15		-	9.2	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge						
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 15 ; Fig. 14		-	17	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V}$; Fig. 15 ; Fig. 14		-	4.4	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 16		-	3195	-	pF
C_{oss}	output capacitance						
C_{rss}	reverse transfer capacitance						
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 50 \text{ V}$; $R_L = 2 \Omega$; $V_{GS} = 10 \text{ V}$; $R_{G(\text{ext})} = 4.7 \Omega$; $T_j = 25 \text{ }^\circ\text{C}$		-	20.7	-	ns
t_r	rise time						
$t_{d(\text{off})}$	turn-off delay time						
t_f	fall time						
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 15 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 17		-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = 100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$		-	52	-	ns
Q_r	recovered charge						

[1] Measured 3 mm from package.

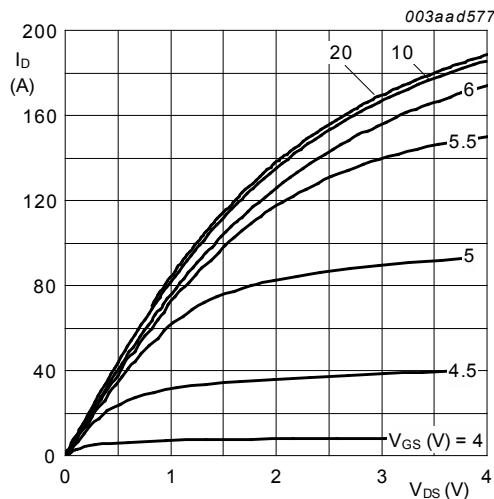


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_J = 25^\circ C$

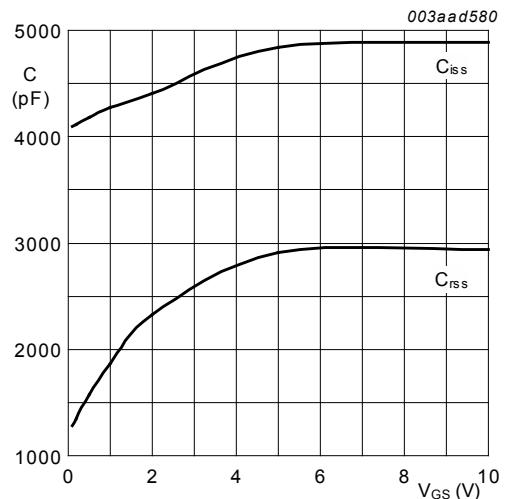


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$V_{DS} = 0 V; f = 1 MHz$

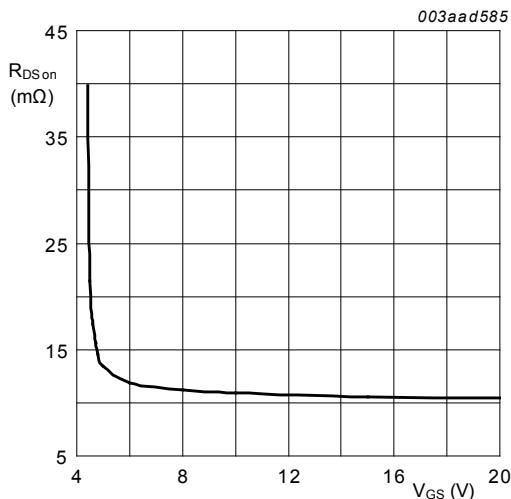


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_J = 25^\circ C$

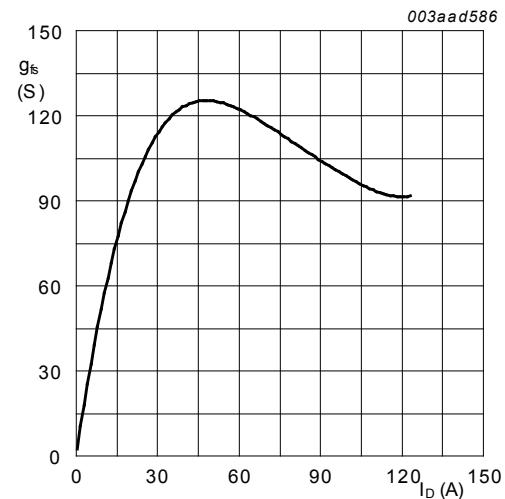


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25^\circ C; V_{DS} = 15 V$

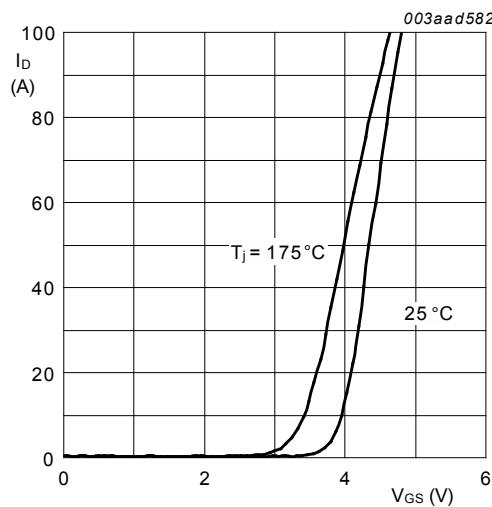


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DSon}$$

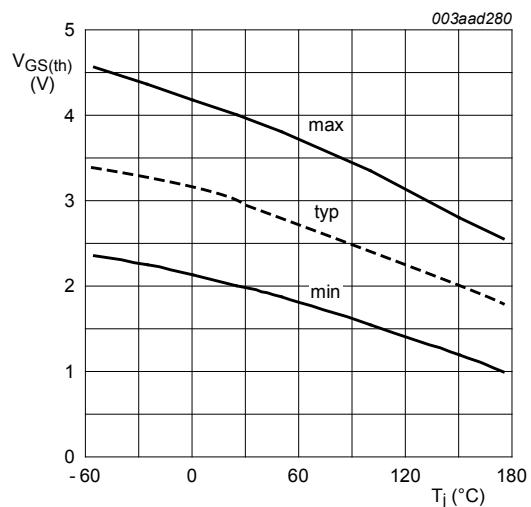


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

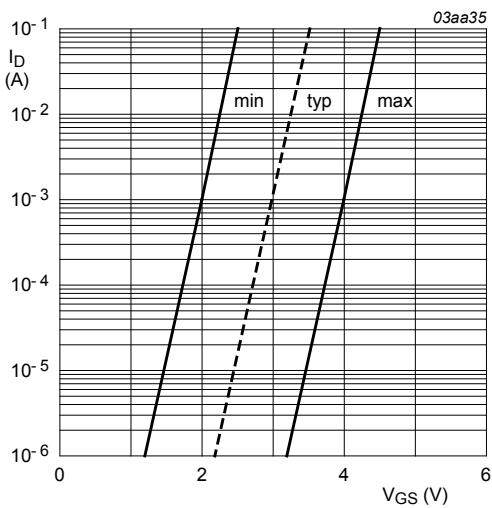


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

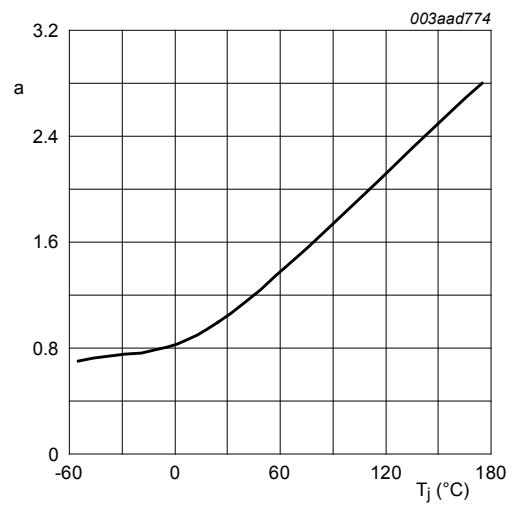


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

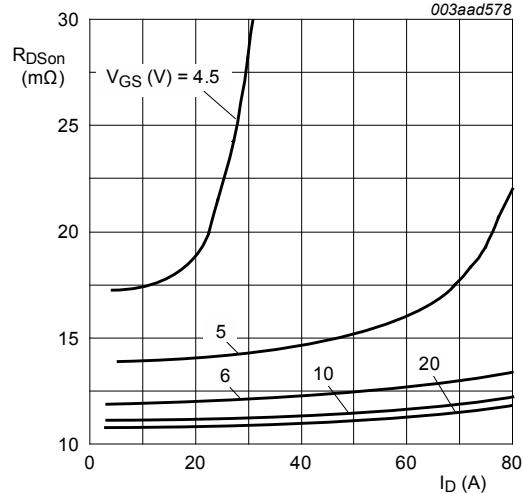


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C$

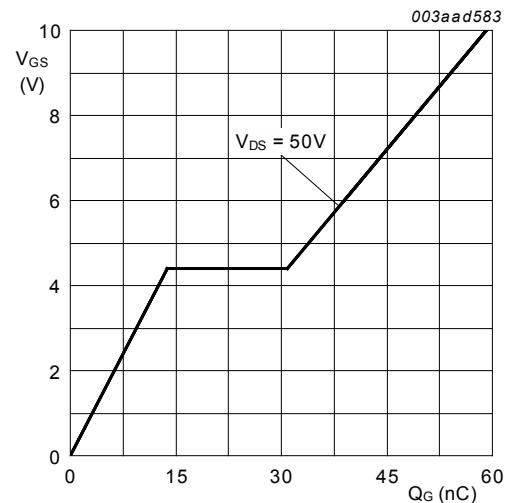


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 25A$

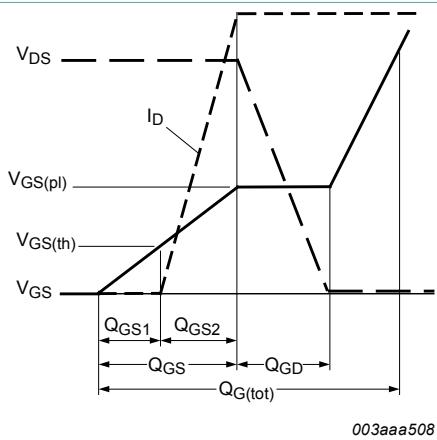


Fig. 15. Gate charge waveform definitions

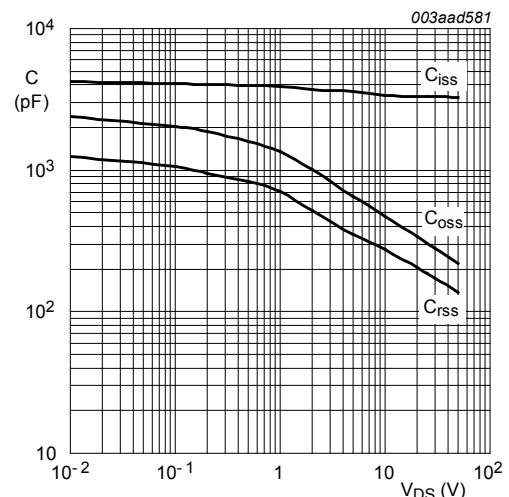


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

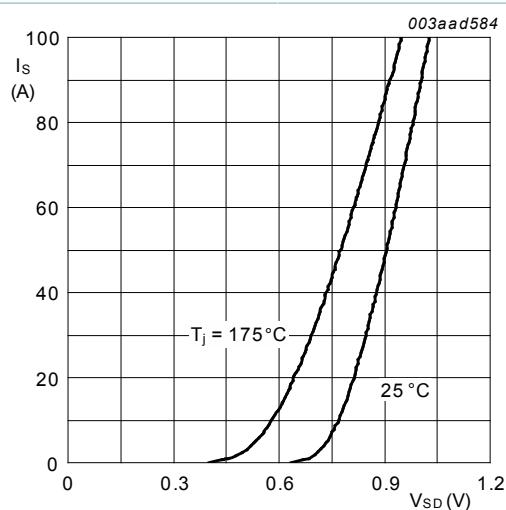
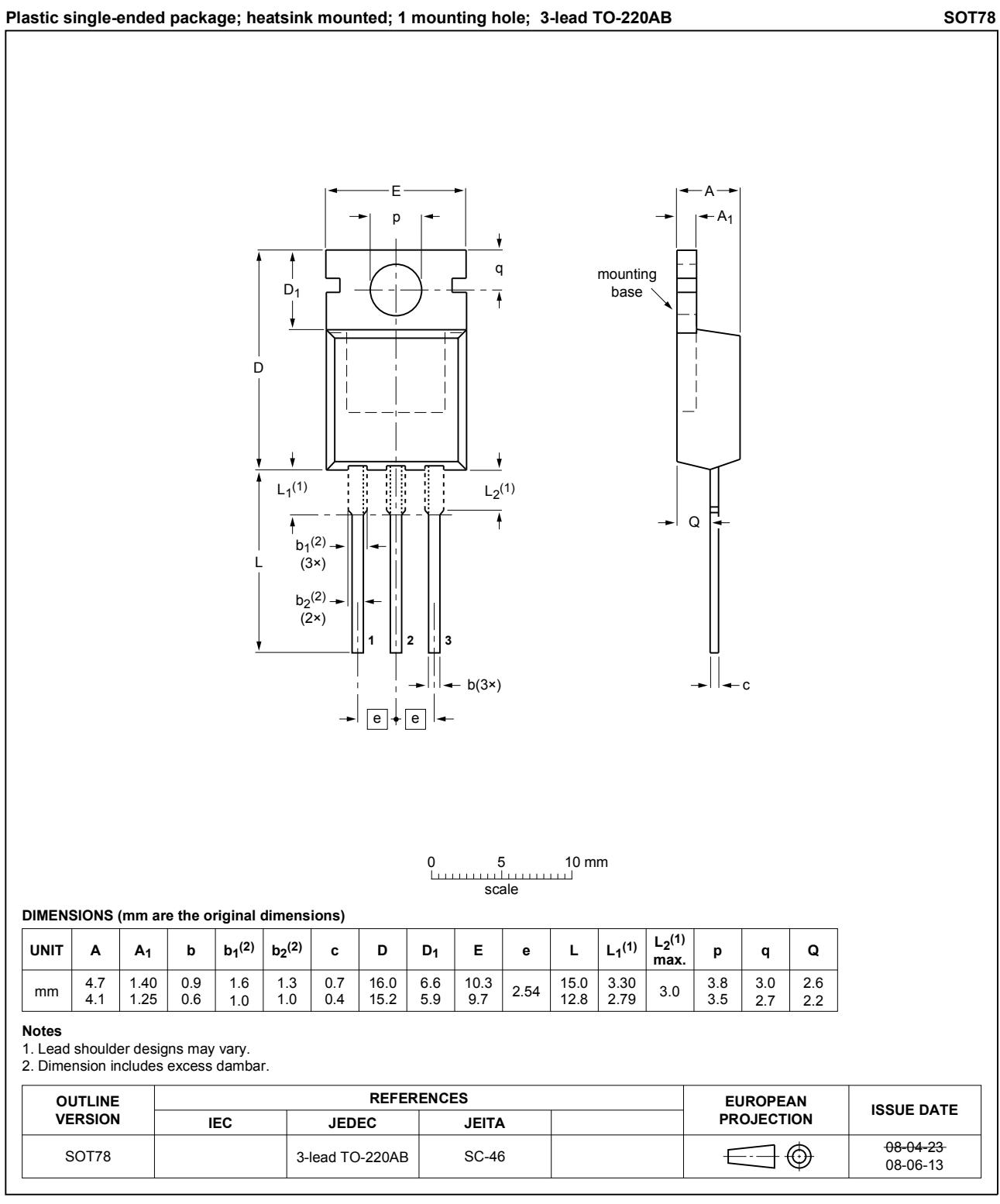


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

8. Package outline



9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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