

PSMN035-150P

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 04 — 16 November 2009

Product data sheet

1. Product profile

1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Switched-mode power supplies

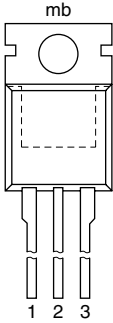
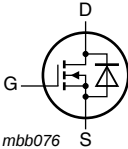
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	150	V
		$T_{mb} = 25\text{ °C}$; see Figure 1 and 2	-	-	50	
			-	-	-	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 3	-	-	-	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; V_{DS} = 120\text{ V}; T_j = 25\text{ °C}$; see Figure 13	-	33	45	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$; see Figure 11 and 12	-	30	35	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT78 (TO-220AB)

3. Ordering information

Table 3. Ordering information

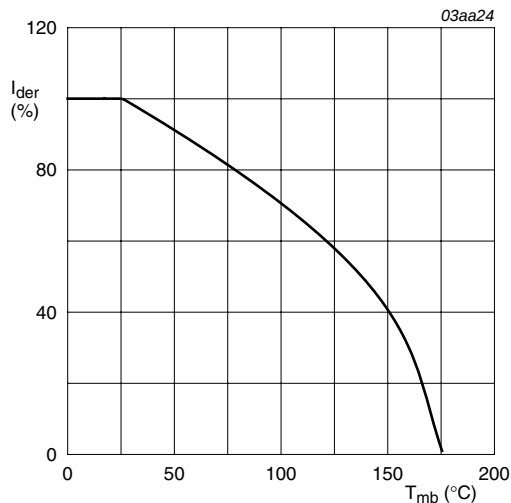
Type number	Package		Version
	Name	Description	
PSMN035-150P	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

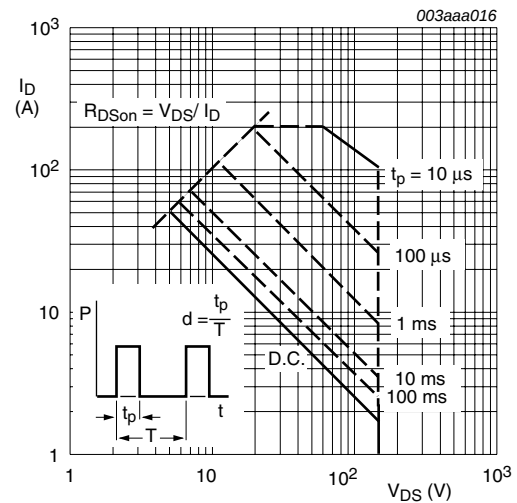
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	150	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ }^{\circ}\text{C}$; $T_j \geq 25\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	150	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$T_{mb} = 100\text{ }^{\circ}\text{C}$; see Figure 1 and 2	-	36	A
		$T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 1 and 2	-	50	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	200	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 3	-	250	W
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	50	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ }^{\circ}\text{C}$	-	200	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $I_D = 47\text{ A}$; $V_{sup} \leq 50\text{ V}$; unclamped; $t_p = 0.1\text{ ms}$; $R_{GS} = 50\text{ }\Omega$; see Figure 4	-	460	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $R_{GS} = 50\text{ }\Omega$; unclamped; see Figure 4	-	50	A



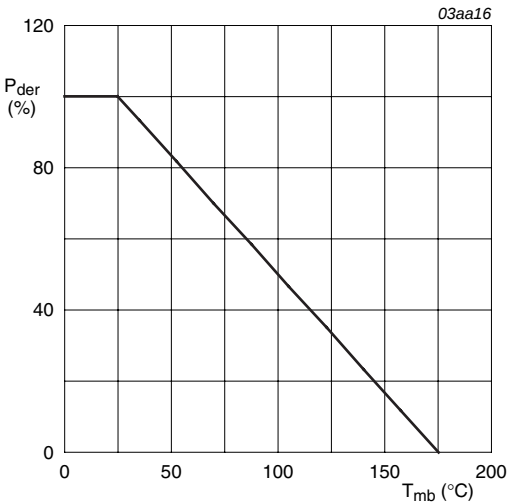
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



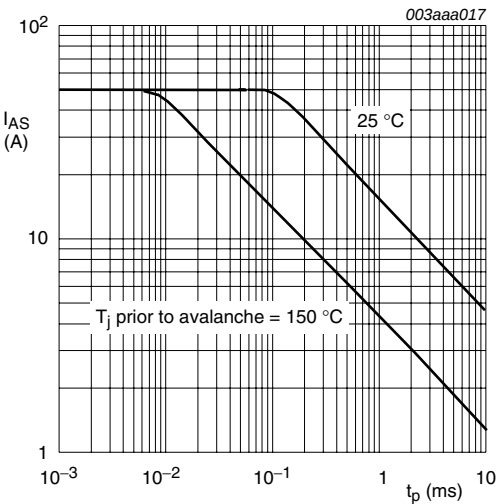
$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is single pulse

Fig 2. Safe operating area; continuous and peak drain currents as a function of drain-source volt



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 3. Normalized total power dissipation as a function of mounting base temperature



Unclamped inductive load; $V_{DS} \leq 15V$; $R_{GS} = 50\Omega$; $V_{GS} = 10V$

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.6	-	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	-	60	K/W

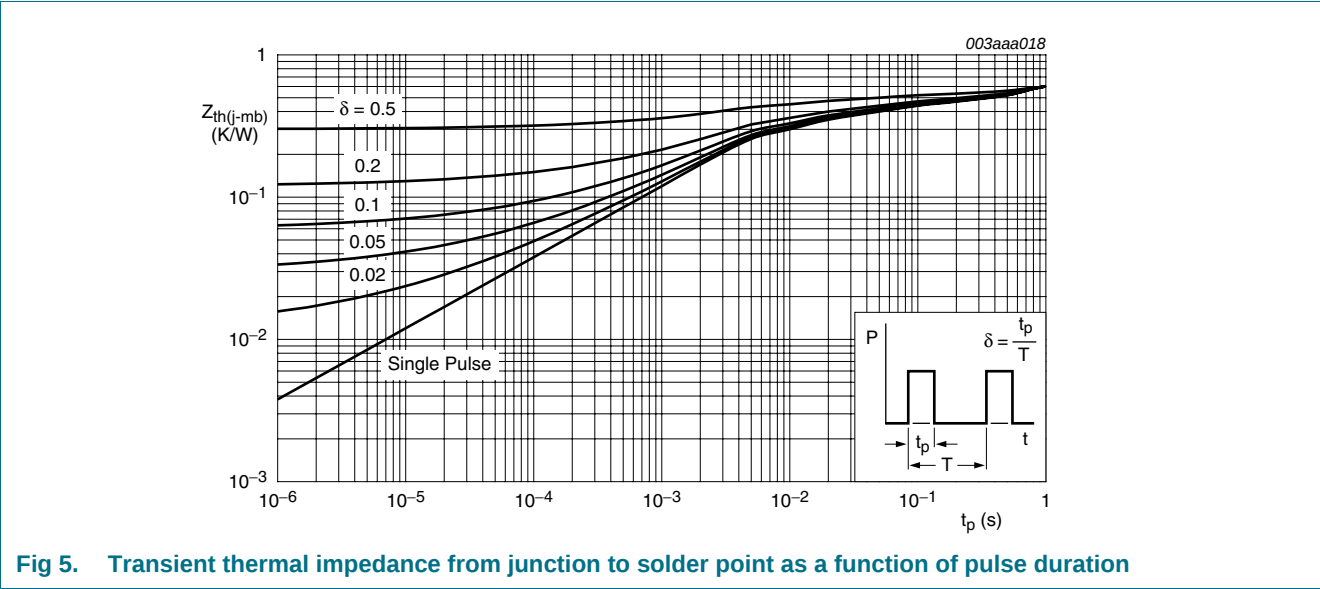
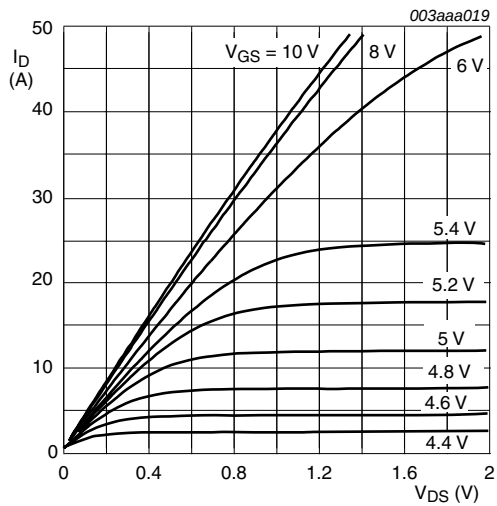


Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

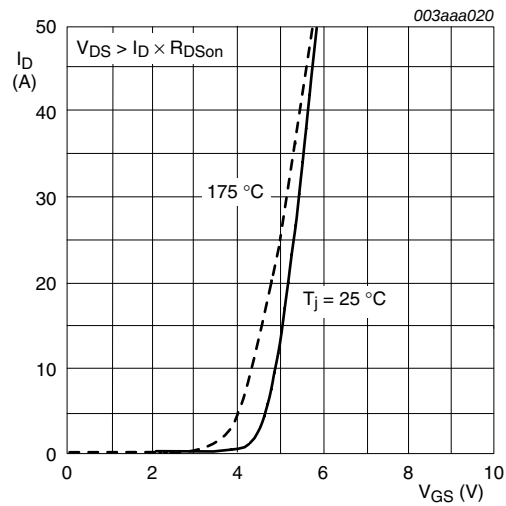
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	150	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10	2	3	4	V
I _{DSS}	drain leakage current	V _{DS} = 150 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
		V _{DS} = 150 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 11 and 12	-	-	98	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11 and 12	-	30	35	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 50 A; V _{DS} = 120 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 13	-	79	-	nC
Q _{GS}	gate-source charge		-	17	-	nC
Q _{GD}	gate-drain charge		-	33	45	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 14	-	4720	-	pF
C _{oss}	output capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 13	-	456	-	pF
C _{rss}	reverse transfer capacitance		-	208	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 75 V; R _L = 1.5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5.6 Ω; T _j = 25 °C	-	25	-	ns
t _r	rise time		-	138	-	ns
t _{d(off)}	turn-off delay time		-	79	-	ns
t _f	fall time		-	93	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C	-	118	-	ns
Q _r	recovered charge	V _{DS} = 30 V; T _j = 25 °C	-	0.66	-	nC



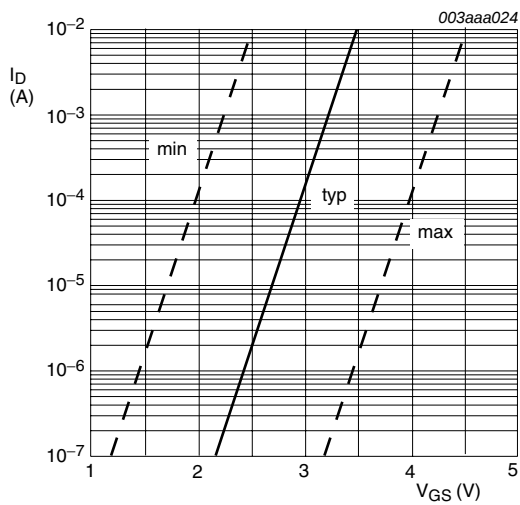
$T_j = 25^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



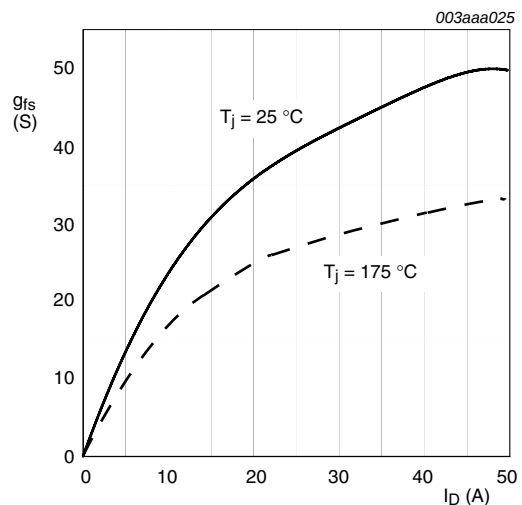
$T_j = 25^\circ\text{C}$ and 175°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



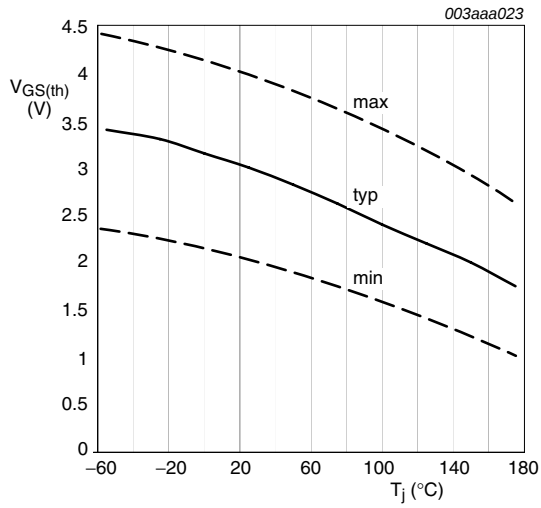
$T_j = 25^\circ\text{C}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



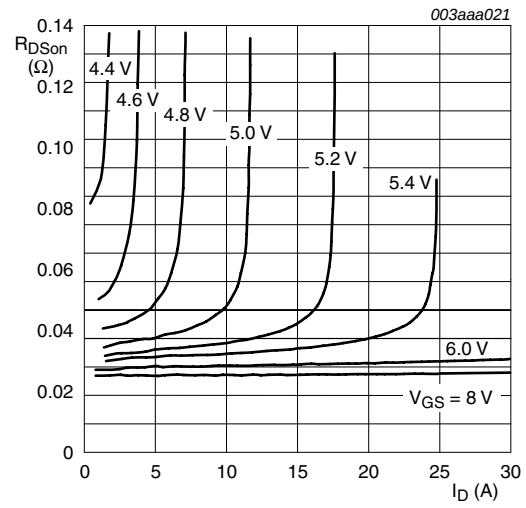
$T_j = 25^\circ\text{C}$ and 175°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 9. Forward transconductance as a function of drain current; typical values



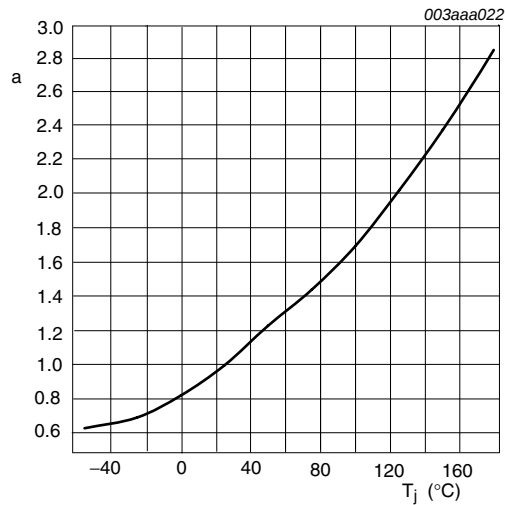
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



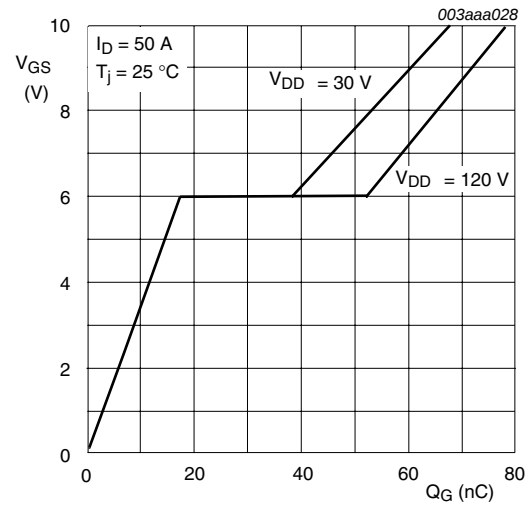
$$T_j = 25^\circ\text{C}$$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



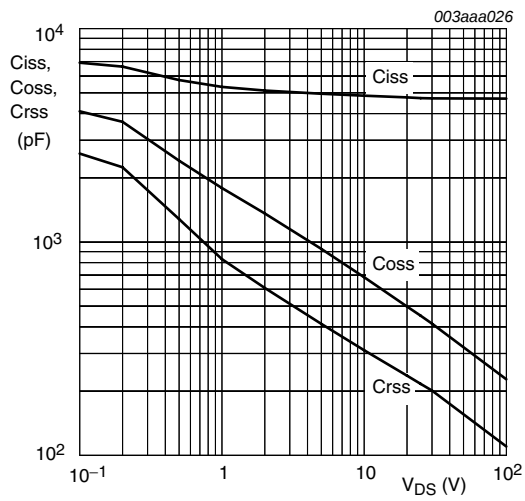
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



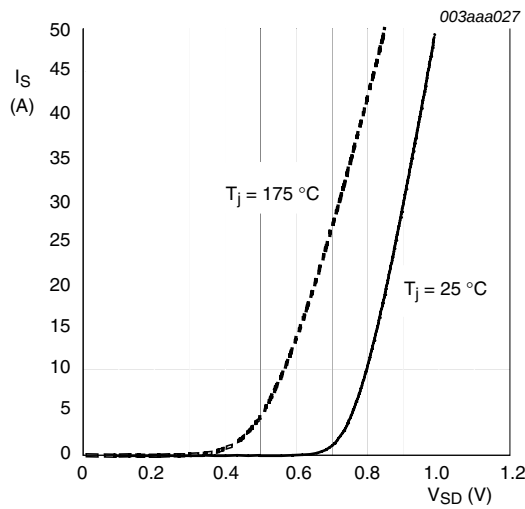
$$I_D = 50 \text{ A}; T_j = 25^\circ\text{C}$$

Fig 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^{\circ}C \text{ and } 175^{\circ}C; V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB SOT78

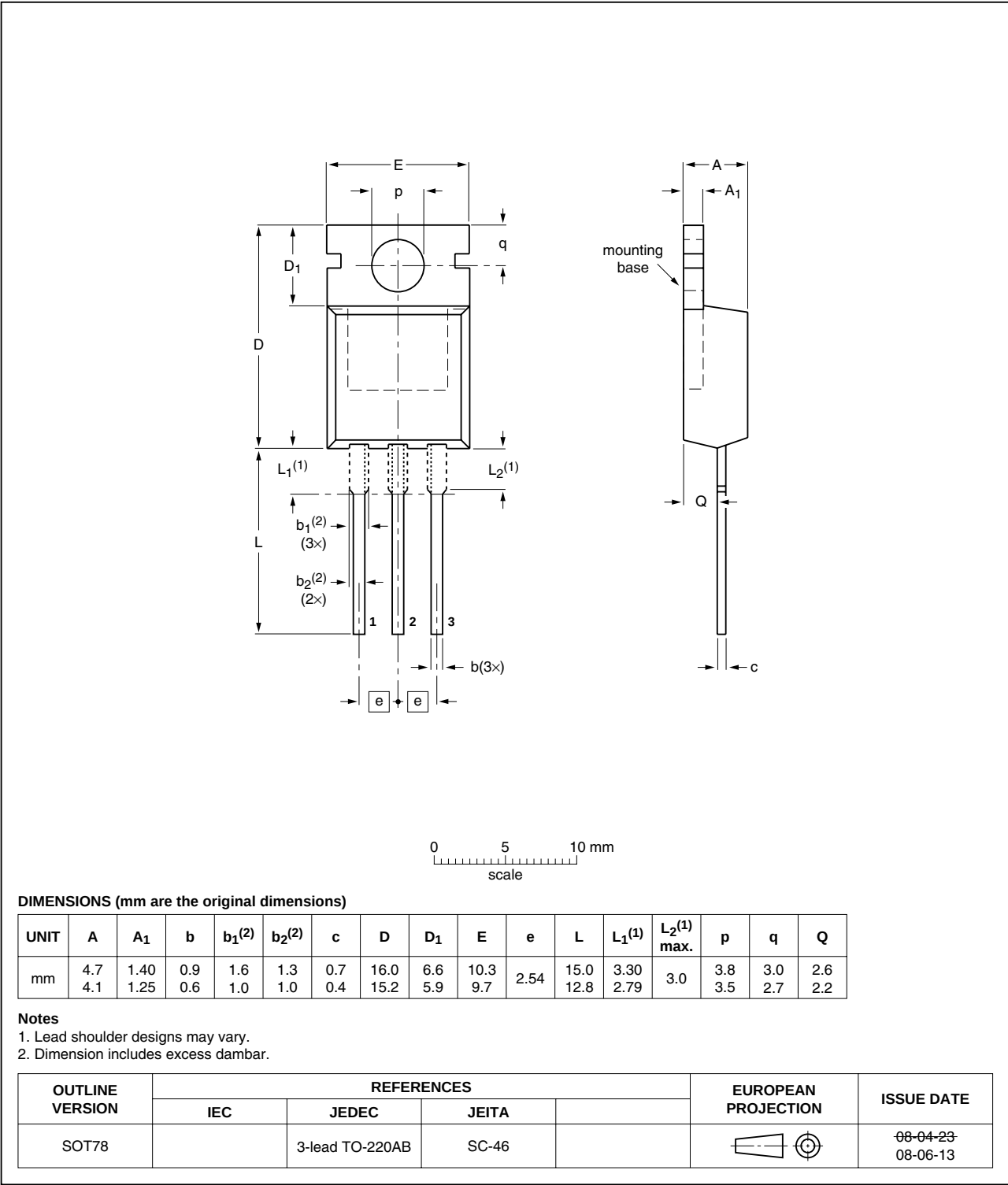


Fig 16. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN035-150P_4	20091116	Product data sheet	-	PSMN035-150_SERIES_HG_3
Modifications:				
• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number PSMN035-150P separated from data sheet PSMN035-150_SERIES_HG_3.				
PSMN035-150_SERIES_HG_3	20000328	Product specification	-	PSMN035-150_SERIES_2
PSMN035-150_SERIES_2	19990801	Product specification	-	PSMN035-150_SERIES_1
PSMN035-150_SERIES_1	19990201	Objective specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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