



PSMN2R2-40PS

N-channel 40 V 2.1 mΩ standard level MOSFET

22 February 2013

Product data sheet

1. General description

Standard level N-channel MOSFET in TO220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

3. Applications

- DC-to-DC convertors
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

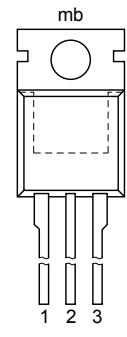
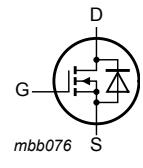
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$		-	-	40	V
I_D	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V};$ Fig. 3 ; Fig. 1		-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C};$ Fig. 2		-	-	306	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 12	[1]	-	1.75	2.1	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10 \text{ V}; I_D = 80 \text{ A}; V_{DS} = 20 \text{ V};$ Fig. 14 ; Fig. 15		-	25	-	nC

[1] Measured 3 mm from package.

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	drain	 TO-220AB (SOT78)	

6. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description	Version	
PSMN2R2-40PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78	

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R2-40PS	PSMN2R2-40PS

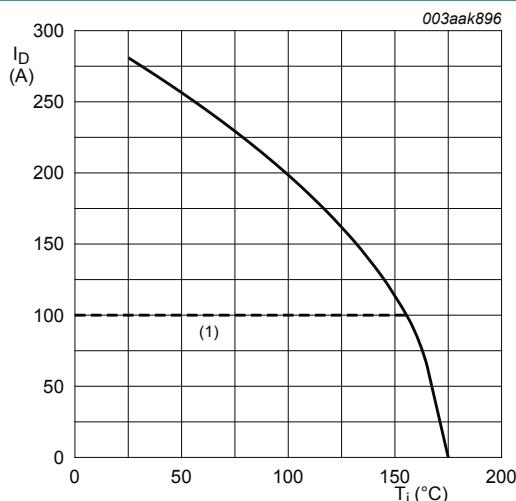
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$	-	40	V
V_{DGR}	drain-gate voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 175^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100^\circ\text{C}$; Fig. 1	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25^\circ\text{C}$; Fig. 3 ; Fig. 1	-	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$; Fig. 3	-	1122	A

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	306	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 µs; T _{mb} = 25 °C	-	1122	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 40 V; unclamped; R _{GS} = 50 Ω	-	1.24	J



(1) Capped at 100 A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

V_{GS} ≥ 10 V

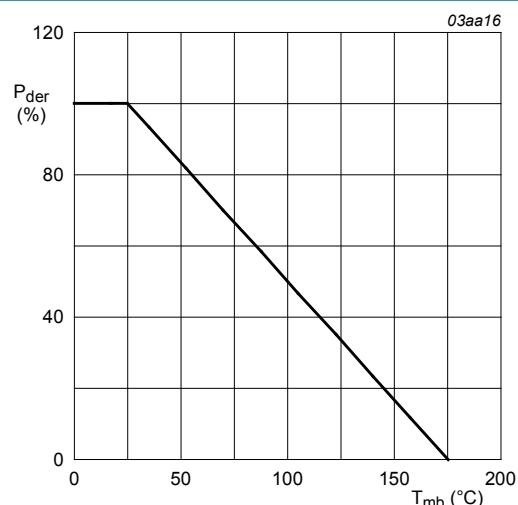


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$

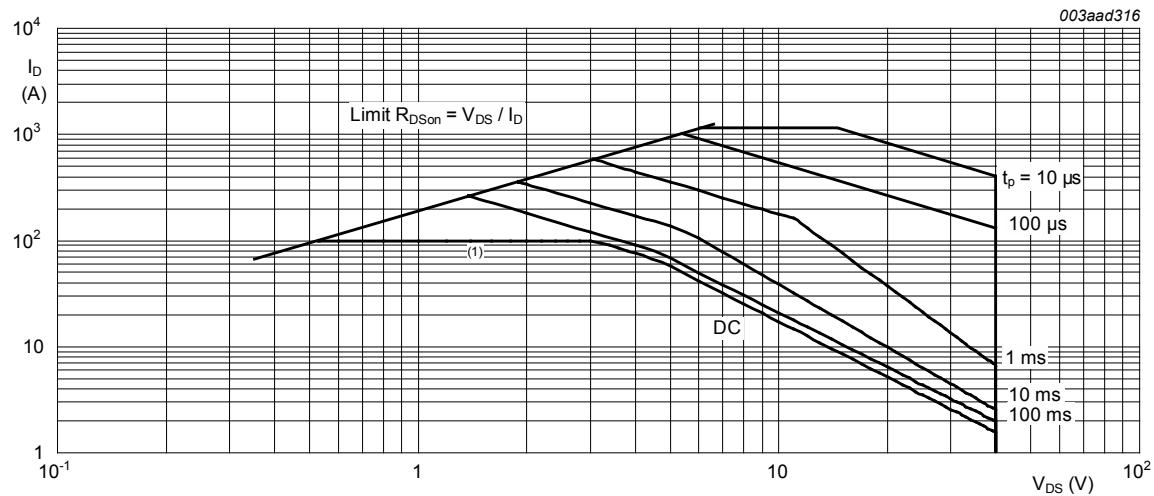


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ\text{C}$; I_{DM} is a single pulse; (1) Capped at 100 A due to package

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.25	0.5	K/W

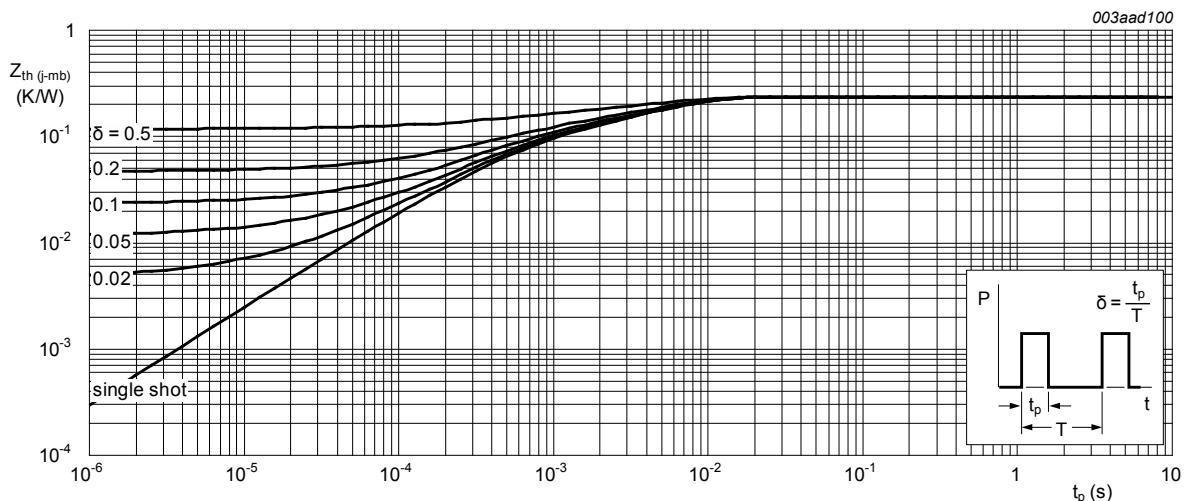


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

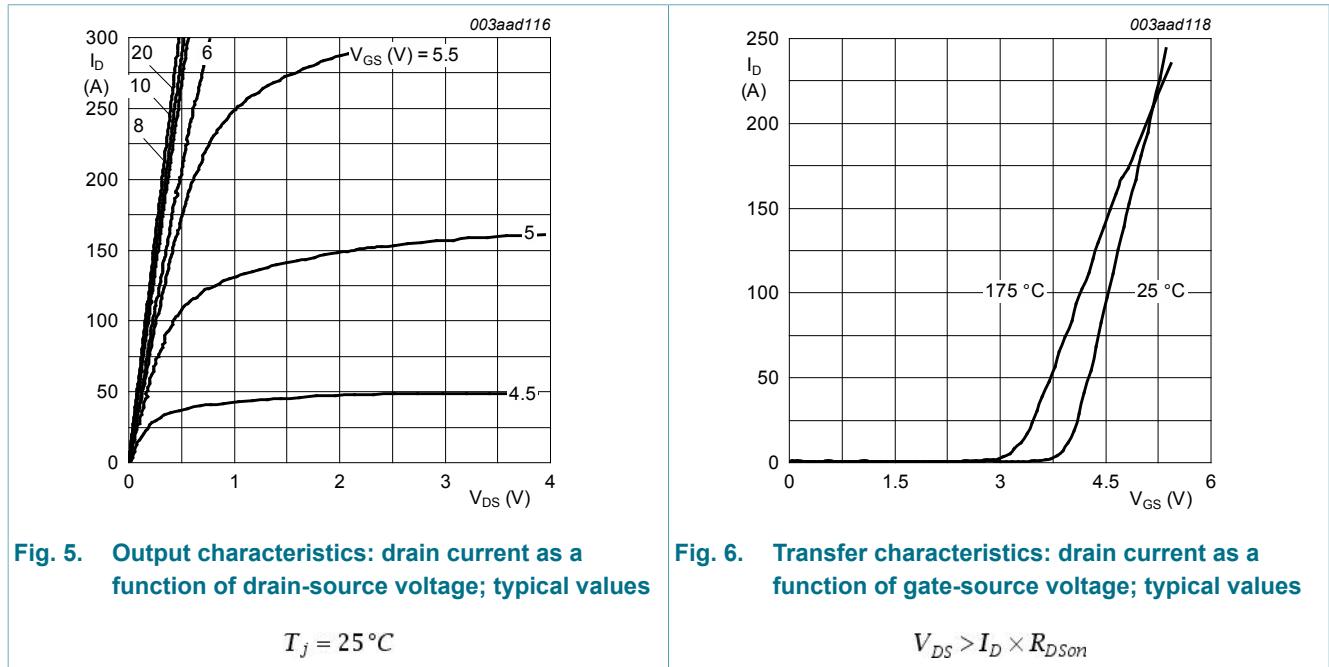
Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$		36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55^\circ C$ Fig. 10		-	-	4.6	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175^\circ C$ Fig. 10		1	-	-	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$ Fig. 11 ; Fig. 10		2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	10	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125^\circ C$		-	-	200	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 100^\circ C$ Fig. 12 ; Fig. 13		-	2.4	2.85	$m\Omega$
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C$ Fig. 12 ; Fig. 13		-	3.25	3.9	$m\Omega$
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$ Fig. 12	[1]	-	1.75	2.1	$m\Omega$
R_G	internal gate resistance (AC)	$f = 1 MHz$		-	1	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$		-	110	-	nC
		$I_D = 80 A; V_{DS} = 20 V; V_{GS} = 10 V$ Fig. 14 ; Fig. 15		-	130	-	nC
Q_{GS}	gate-source charge			-	42	-	nC
				-	24	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	18	-	nC
				-	25	-	nC
Q_{GD}	gate-drain charge			-	4.95	-	V
				-	8423	-	pF
C_{iss}	input capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz$		-	1671	-	pF
		$T_j = 25^\circ C$; Fig. 16		-			

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{rss}	reverse transfer capacitance			-	814	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20$ V; $R_L = 0.25$ Ω; $V_{GS} = 10$ V;		-	33.2	-	ns
t_r	rise time	$R_{G(ext)} = 1.5$ Ω		-	40.4	-	ns
$t_{d(off)}$	turn-off delay time			-	66.6	-	ns
t_f	fall time			-	25.2	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25$ A; $V_{GS} = 0$ V; $T_j = 25$ °C; Fig. 17		-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 25$ A; $dI_S/dt = -100$ A/μs; $V_{GS} = 0$ V; $V_{DS} = 20$ V		-	53.7	-	ns
Q_r	recovered charge	$I_S = 25$ A; $dI_S/dt = -100$ A/μs; $V_{GS} = 0$ V; $V_{DS} = 20$ V; $T_j = 25$ °C		-	80.75	-	nC

[1] Measured 3 mm from package.



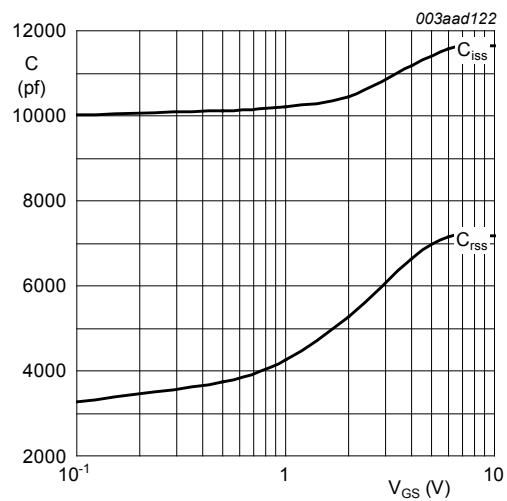


Fig. 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

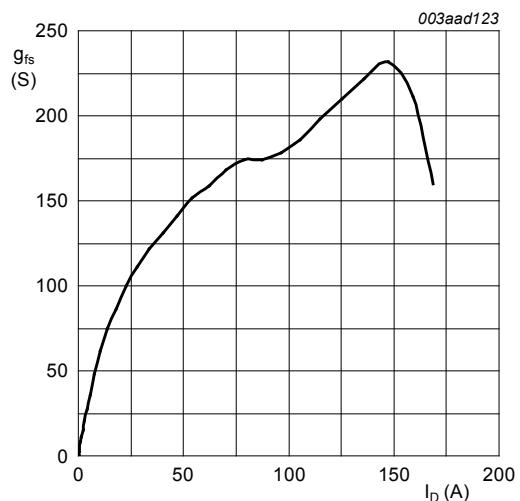


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$; $V_{DS} = 25\text{ V}$

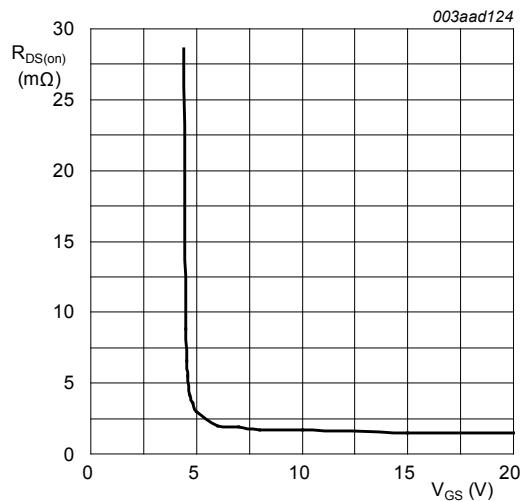


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}$; $I_D = 25\text{ A}$

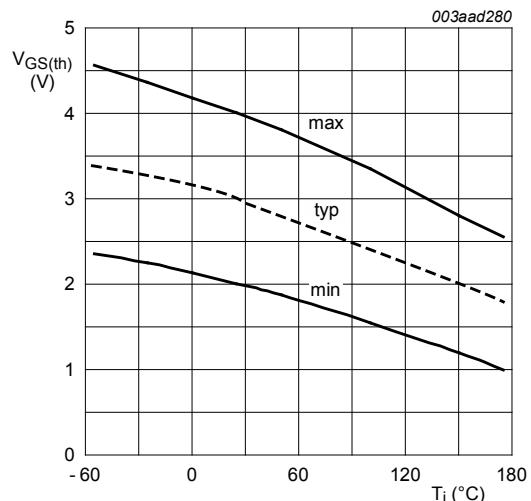


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

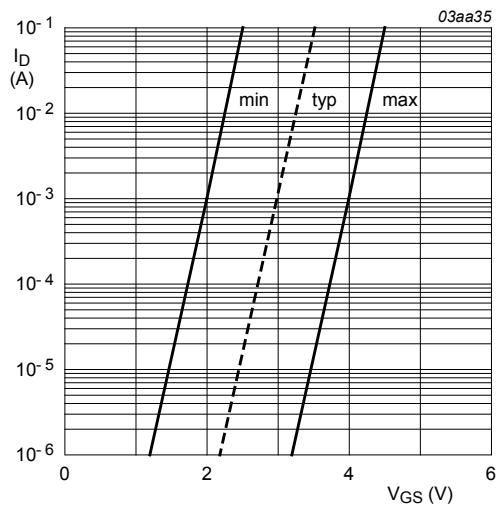


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

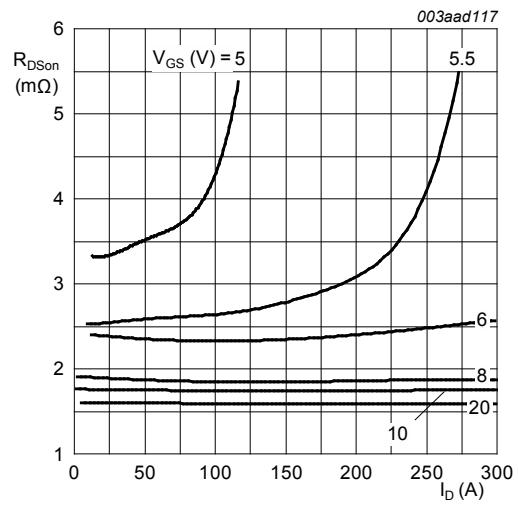


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

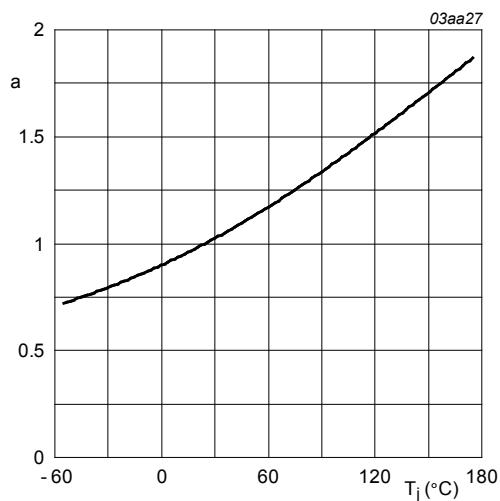


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

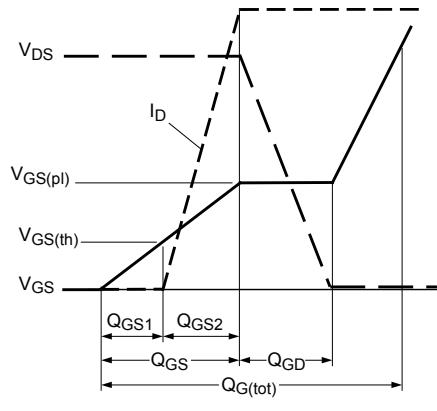


Fig. 14. Gate charge waveform definitions

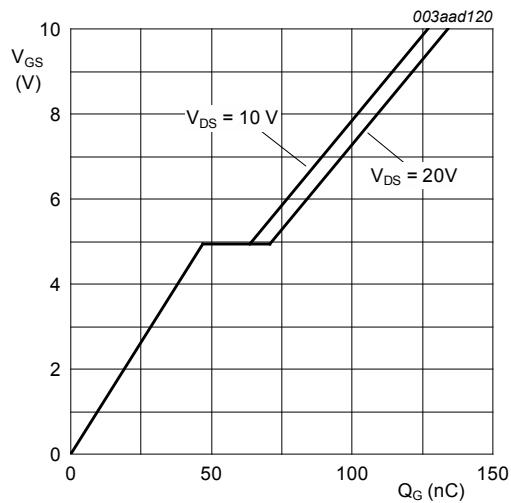


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

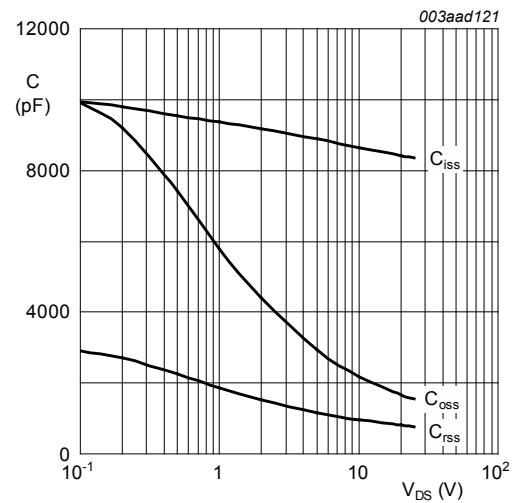


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

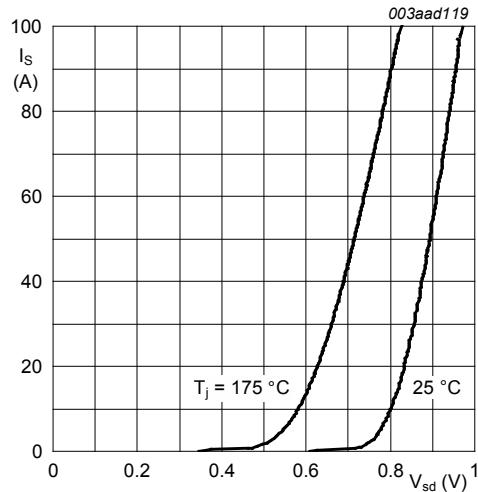


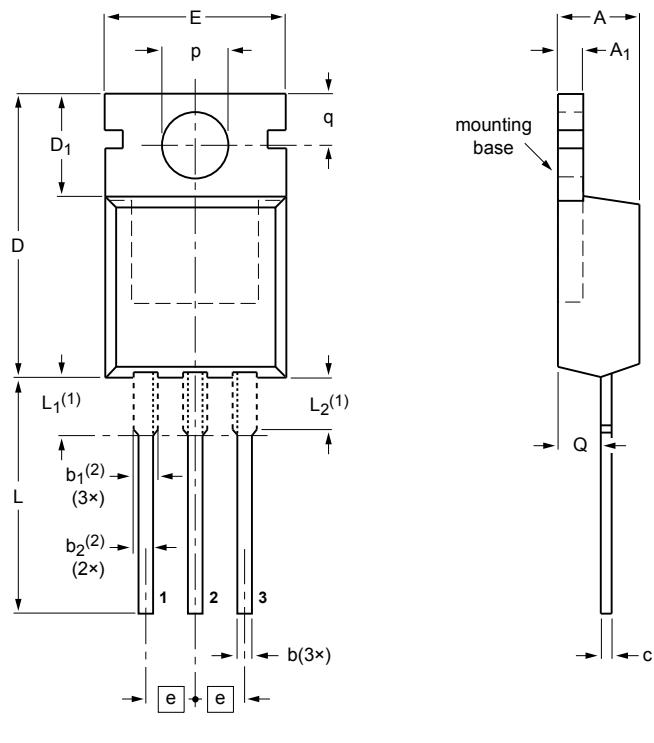
Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁₍₂₎	b ₂₍₂₎	c	D	D ₁	E	e	L	L ₁₍₁₎	L ₂₍₁₎ max.	p	q	Q
mm	4.7	1.40	0.9	1.6	1.3	0.7	16.0	6.6	10.3	2.54	15.0	3.30	3.0	3.8	3.0	2.6
	4.1	1.25	0.6	1.0	1.0	0.4	15.2	5.9	9.7		12.8	2.79	3.0	3.5	2.7	2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			08-04-23 08-06-13

Fig. 18. Package outline TO-220AB (SOT78)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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