

PSMN3R4-30BLE

N-channel 30 V 3.4 mΩ logic level MOSFET in D2PAK

12 October 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low R_{DSon} for low conduction losses

1.3 Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$		-	-	30	V
I_D	drain current	$T_{mb} = 25 \text{ }^\circ\text{C}; V_{GS} = 10 \text{ V}$; Fig. 1	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 2		-	-	178	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$; Fig. 12		-	2.95	3.4	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$; Fig. 12		-	4.25	5	$\text{m}\Omega$
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}$; Fig. 14 ; Fig. 15		-	12.2	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}$; Fig. 14 ; Fig. 15		-	81	-	nC



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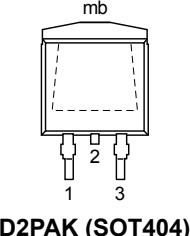
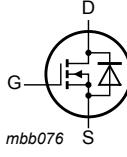


Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 120$ A; $V_{sup} \leq 30$ V; unclamped; $R_{GS} = 50$ Ω; Fig. 3		-	-	246	mJ

[1] Capped at 120A due to package

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain	 D2PAK (SOT404)	 mbb076

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
PSMN3R4-30BLE	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)		SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R4-30BLE	PSMN3R4-30BLE

5. Limiting values

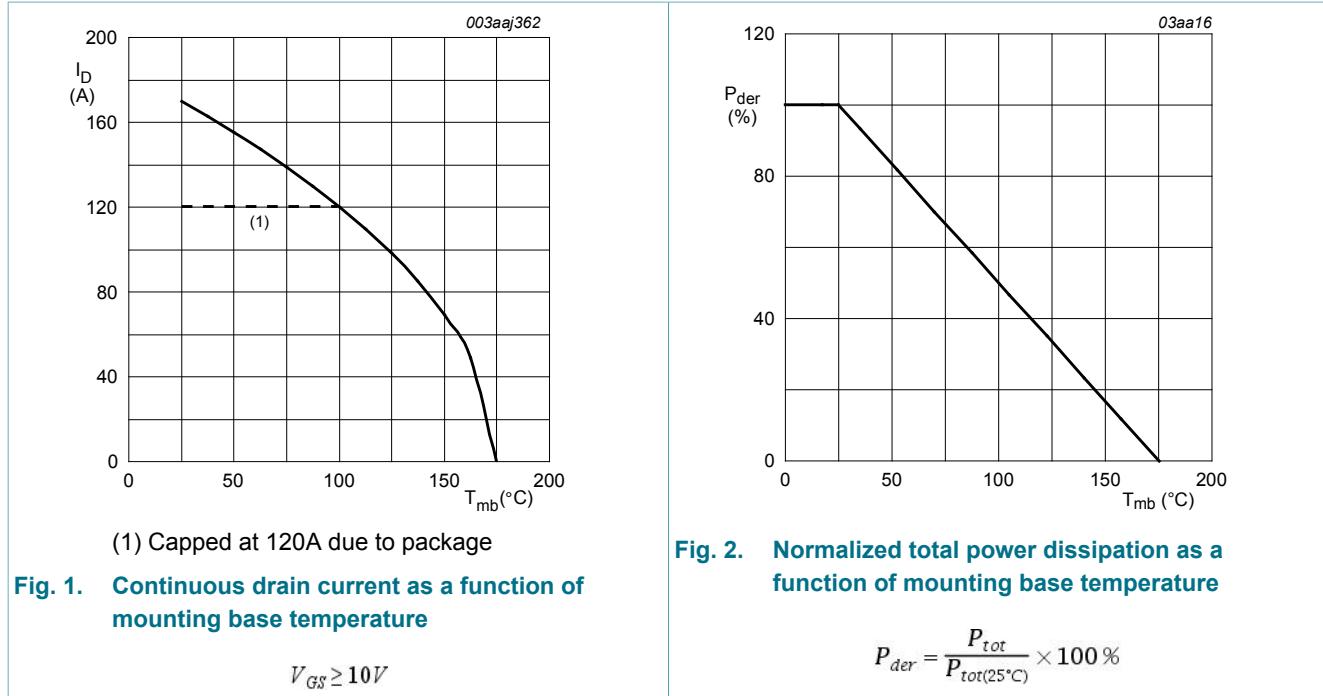
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	30	V
V_{DGR}	drain-gate voltage	$T_j \leq 175$ °C; $T_j \geq 25$ °C; $R_{GS} = 20$ kΩ		-	30	V

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{GS}	gate-source voltage		-20	20	V	
I_D	drain current	$V_{GS} = 10 \text{ V}$; $T_{mb} = 100 \text{ }^\circ\text{C}$; Fig. 1	-	119	A	
		$V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 1	[1]	120	A	
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 4	-	672	A	
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 2	-	178	W	
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$	
T_j	junction temperature		-55	175	$^\circ\text{C}$	
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$	
Source-drain diode						
I_S	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	[1]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	672	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $I_D = 120 \text{ A}$; $V_{sup} \leq 30 \text{ V}$; unclamped; $R_{GS} = 50 \Omega$; Fig. 3	-	246	mJ	

[1] Capped at 120A due to package



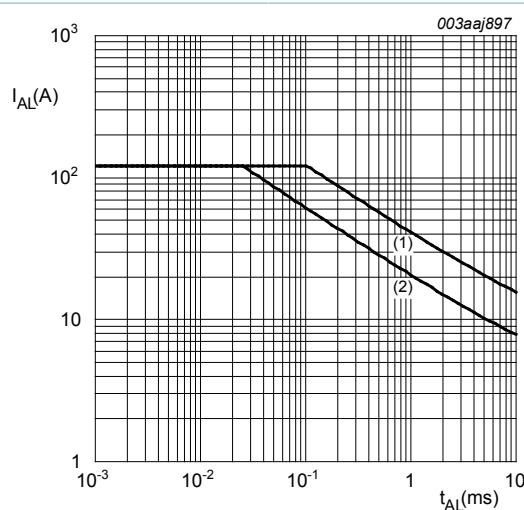


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

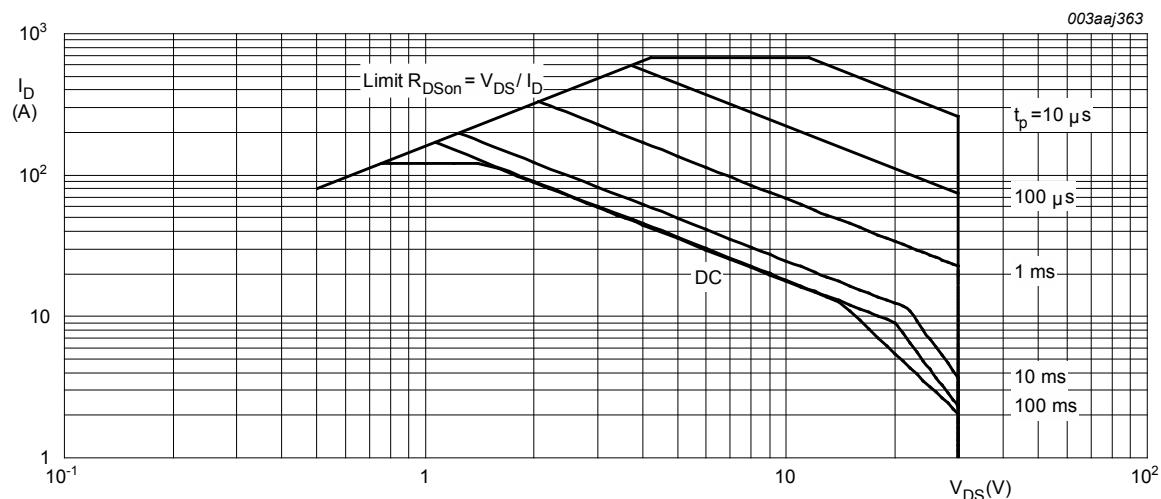
(1) $T_j \text{ (init)} = 25^\circ\text{C}$; (2) $T_j \text{ (init)} = 100^\circ\text{C}$ 

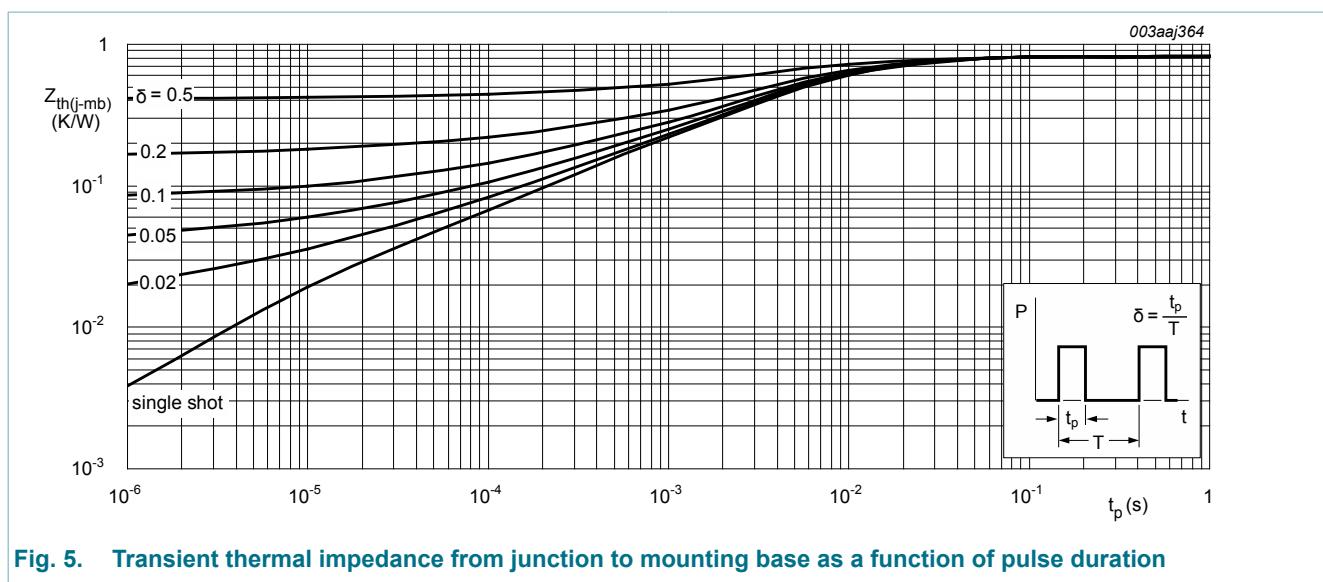
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^\circ\text{C}$; I_{DM} is a single pulse

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.73	0.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board		-	50	-	K/W



7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		27	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10		0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 11; Fig. 10		1.3	1.7	2.15	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 10		-	-	2.45	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C		-	0.2	5	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 100 °C		-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C		-	10	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C		-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	2.95	3.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13; Fig. 12		-	-	5.1	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	4.25	5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 13; Fig. 12		-	-	6.5	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$		0.5	1	2	Ω
Dynamic characteristics							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14 ; Fig. 15		-	81	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 14 ; Fig. 15		-	37	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$		-	79	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 14 ; Fig. 15		-	13.9	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge			-	7.5	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge			-	6.4	-	nC
Q_{GD}	gate-drain charge			-	12.2	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$ Fig. 14 ; Fig. 15		-	3.2	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$		-	4682	-	pF
C_{oss}	output capacitance	$T_j = 25^\circ\text{C};$ Fig. 16		-	909	-	pF
C_{rss}	reverse transfer capacitance			-	438	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.6 \Omega; V_{GS} = 4.5 \text{ V};$		-	35.7	-	ns
t_r	rise time	$R_{G(\text{ext})} = 4.7 \Omega; T_j = 25^\circ\text{C}$		-	101	-	ns
$t_{d(off)}$	turn-off delay time			-	49	-	ns
t_f	fall time			-	51.2	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C};$ Fig. 17		-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = 100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$		-	37	-	ns
Q_r	recovered charge	$V_{DS} = 15 \text{ V}$		-	38	-	nC

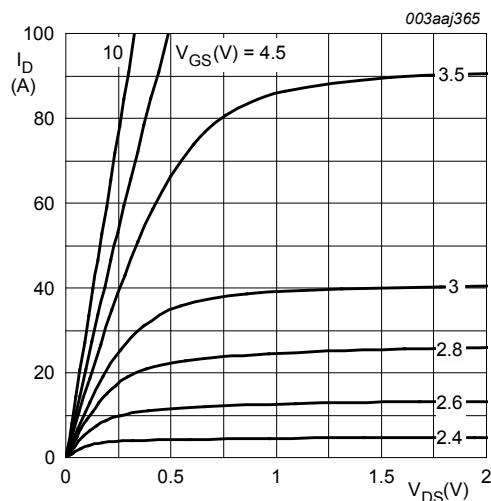


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

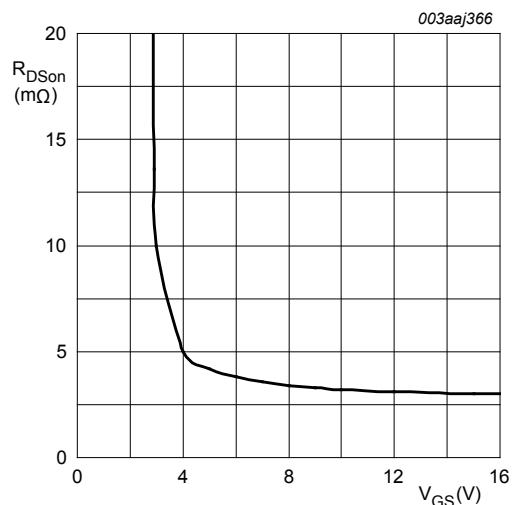


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 25A$

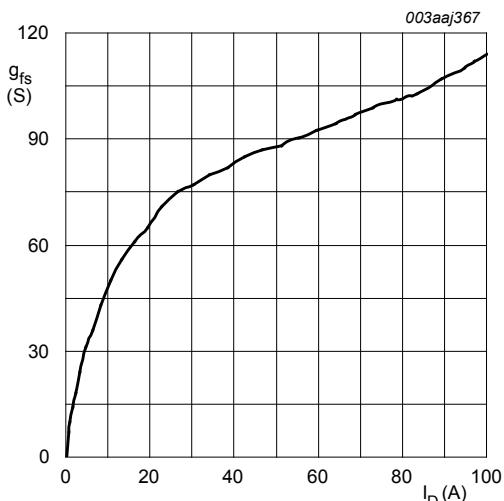


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ C; V_{DS} = 10V$

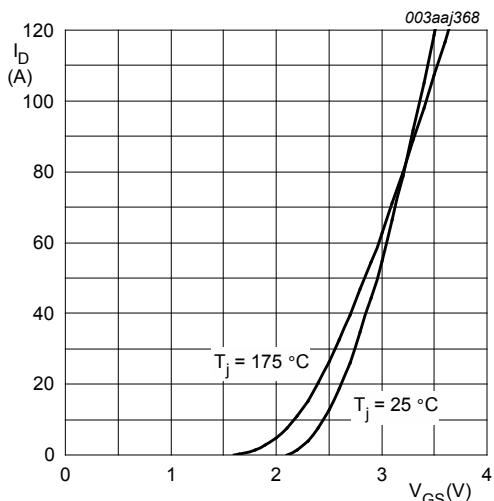


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

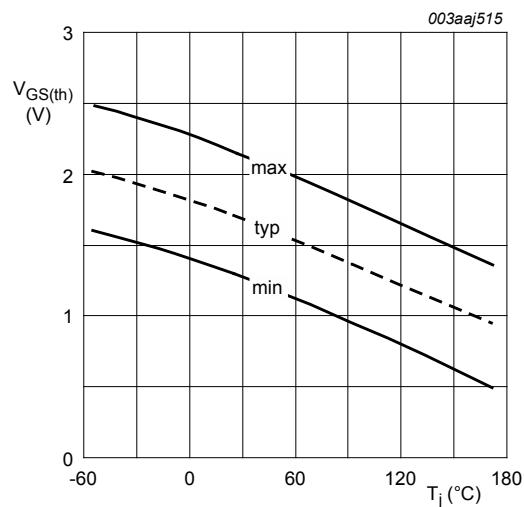


Fig. 10. Gate-source threshold voltage as a function of junction temperature

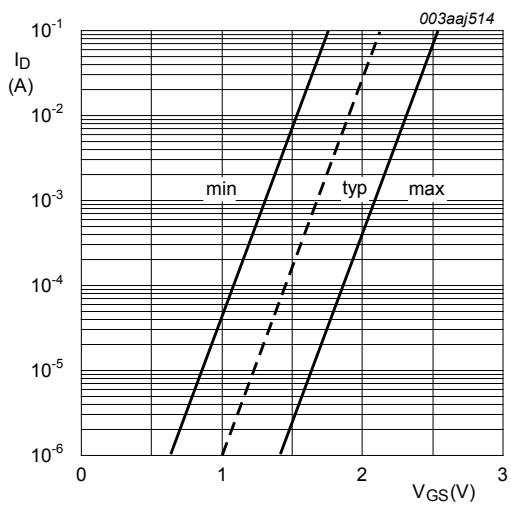


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5V$

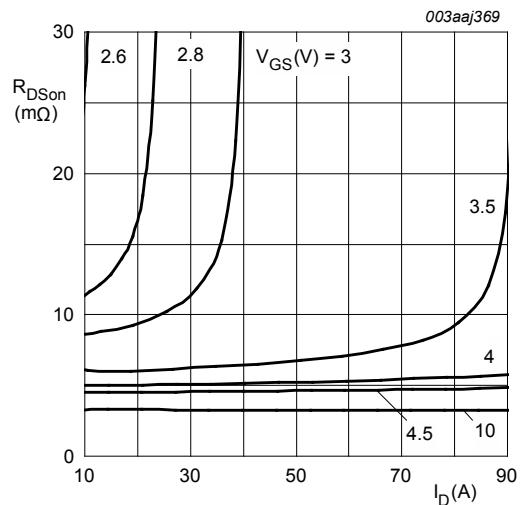


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C$

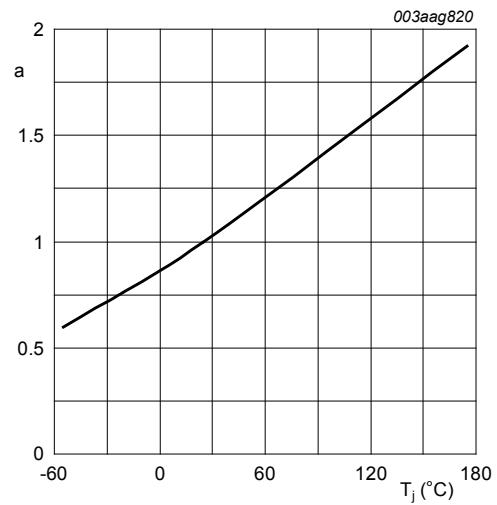


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

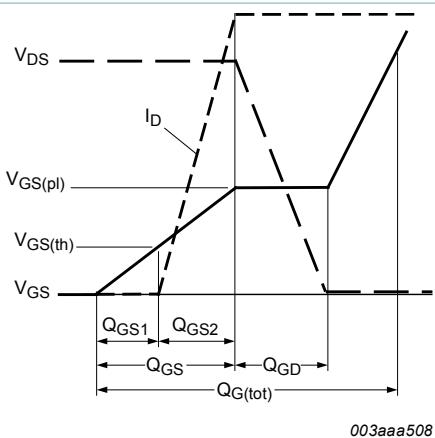


Fig. 14. Gate charge waveform definitions

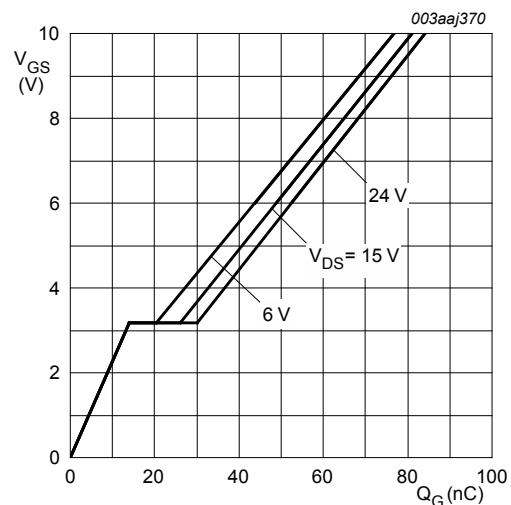


Fig. 15. Gate-source voltage as a function of gate charge; typical values

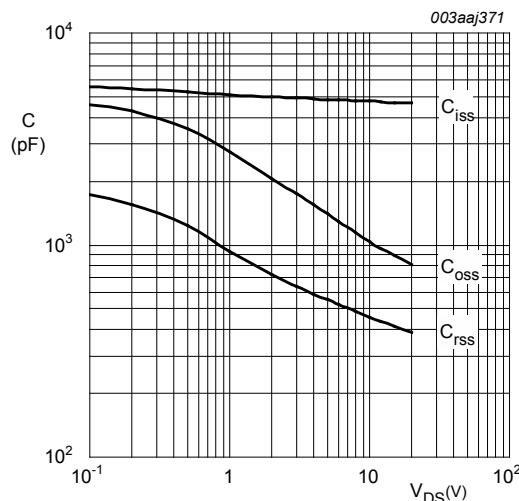
 $T_j = 25^\circ\text{C}$; $I_D = 25\text{A}$ 

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

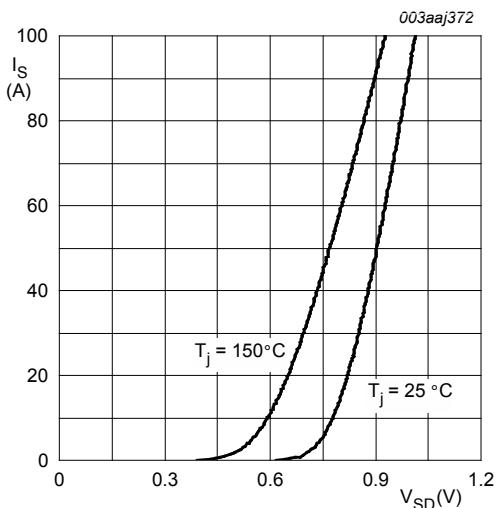
 $V_{GS} = 0\text{V}$; $f = 1\text{MHz}$ 

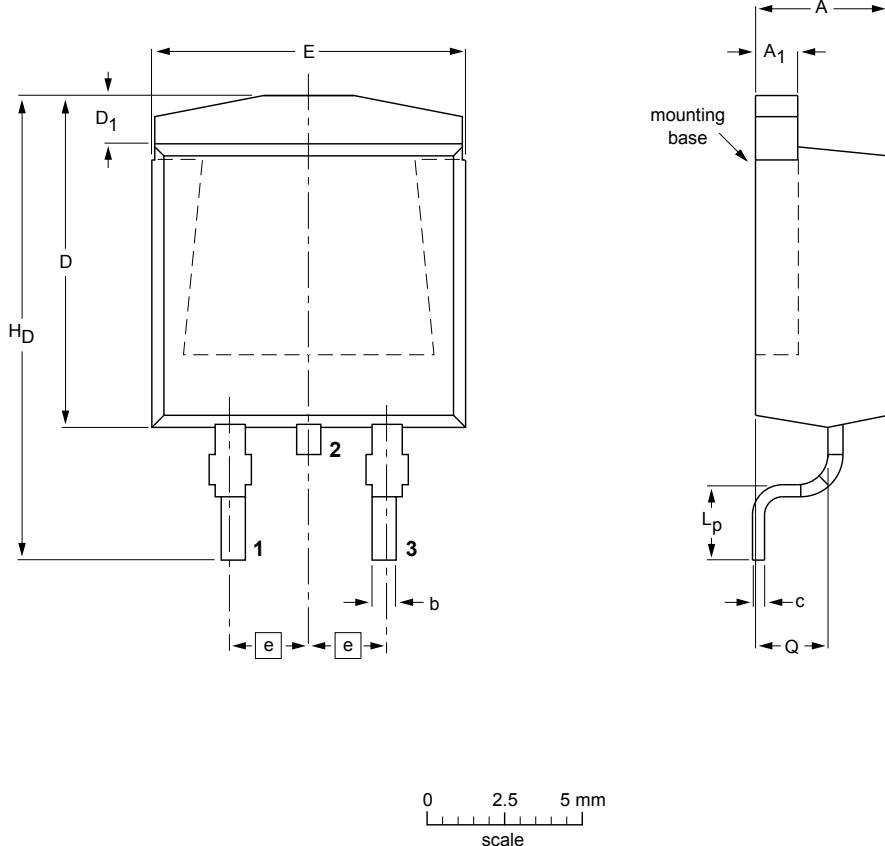
Fig. 17. Source current as a function of source-drain voltage; typical values

 $V_{GS} = 0\text{V}$

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig. 18. Package outline D2PAK (SOT404)

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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