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Kind regards,

Team Nexperia



PSMN4R0-60YS

N-channel LFAK 60 V, 4.0 mΩ standard level FET

14 May 2015

Product data sheet

1. General description

Standard level N-channel MOSFET in LFAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of telecom, industrial and domestic equipment.

2. Features and benefits

- Advanced TrenchMOS provides low R_{DSon} and low gate charge
- High efficiency in switching power converters
- Improved mechanical and thermal characteristics
- LFAK provides maximum power density in a Power SO8 package

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies
- Telecom power

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	130	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 100\text{ °C}$; Fig. 12	-	-	8.3	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C}$; Fig. 13	-	3.6	4	mΩ

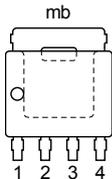
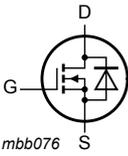


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 75\text{ A}; V_{DS} = 30\text{ V};$	-	11.2	-	nC
$Q_{G(tot)}$	total gate charge	Fig. 14 ; Fig. 15	-	56	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 100\text{ A}; V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ }\Omega;$ unclamped	-	-	170	mJ

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p><i>mbb076</i> S</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R0-60YS	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Limiting values

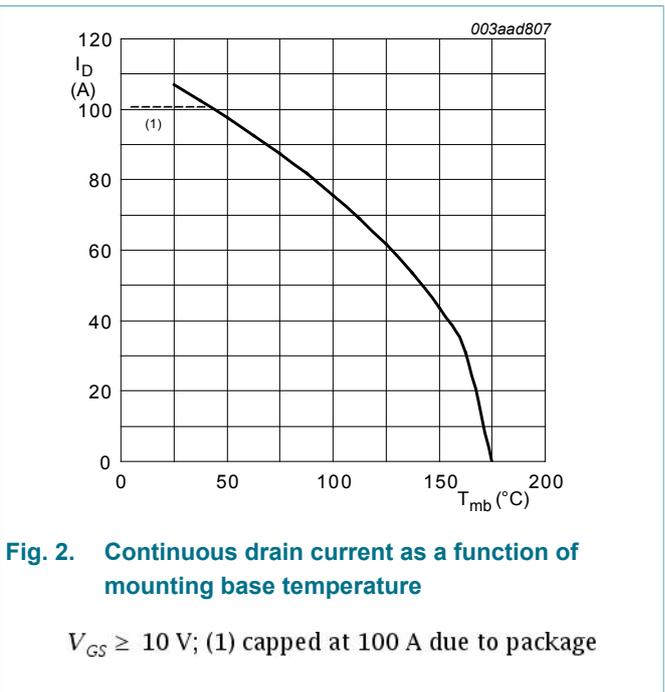
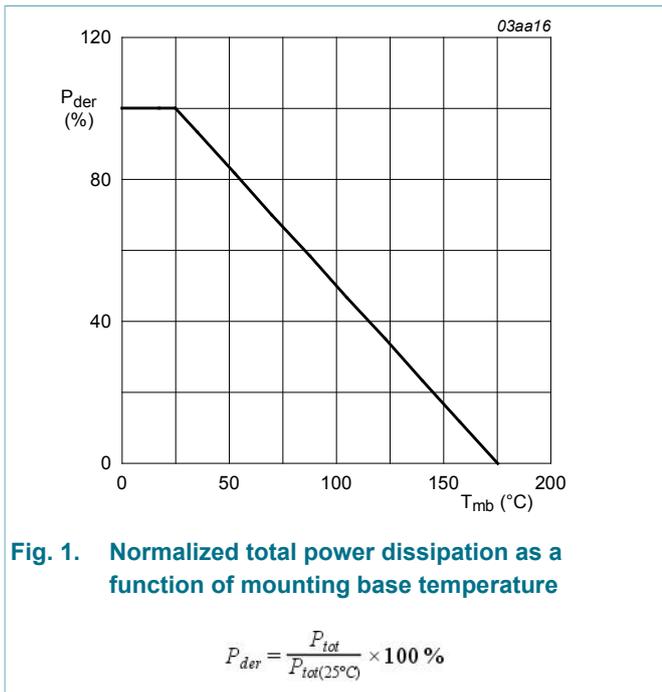
Table 4. Limiting values

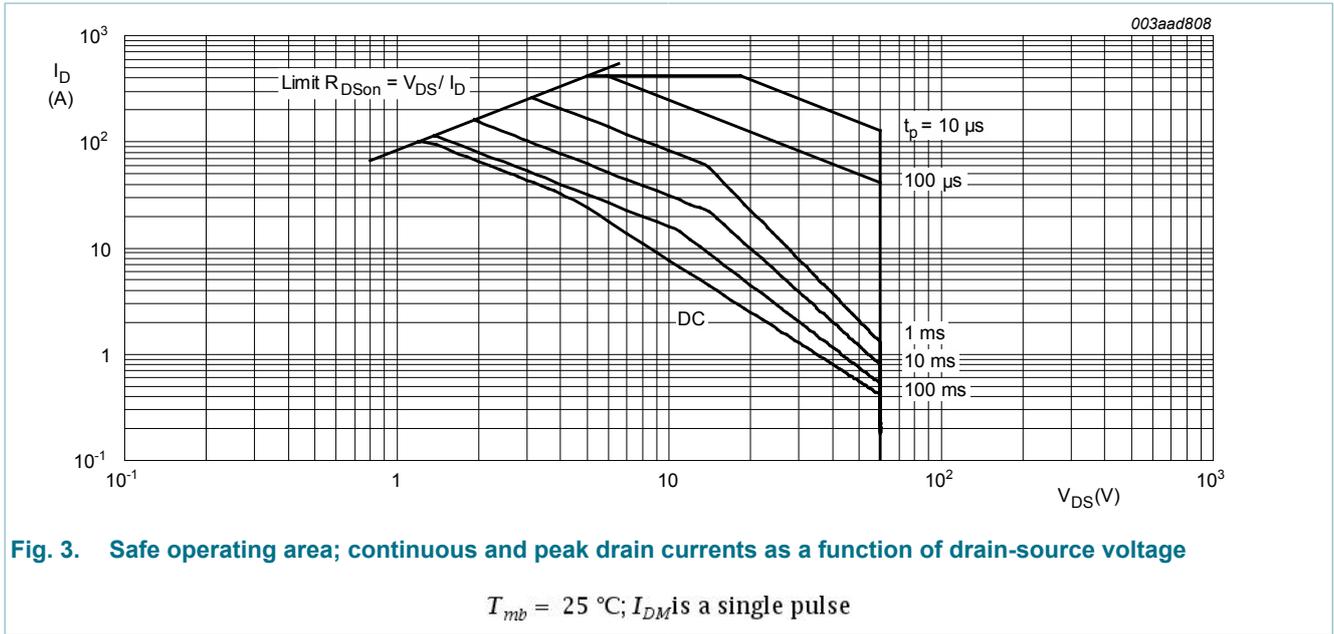
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	130	W
I_D	drain current	$T_{mb} = 100\text{ °C};$ Fig. 2	-	74	A

Symbol	Parameter	Conditions		Min	Max	Unit
		$T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	418	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	418	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 60\text{ V}$; $R_{GS} = 50\ \Omega$; unclamped		-	170	mJ

[1] Continuous current is limited by package.

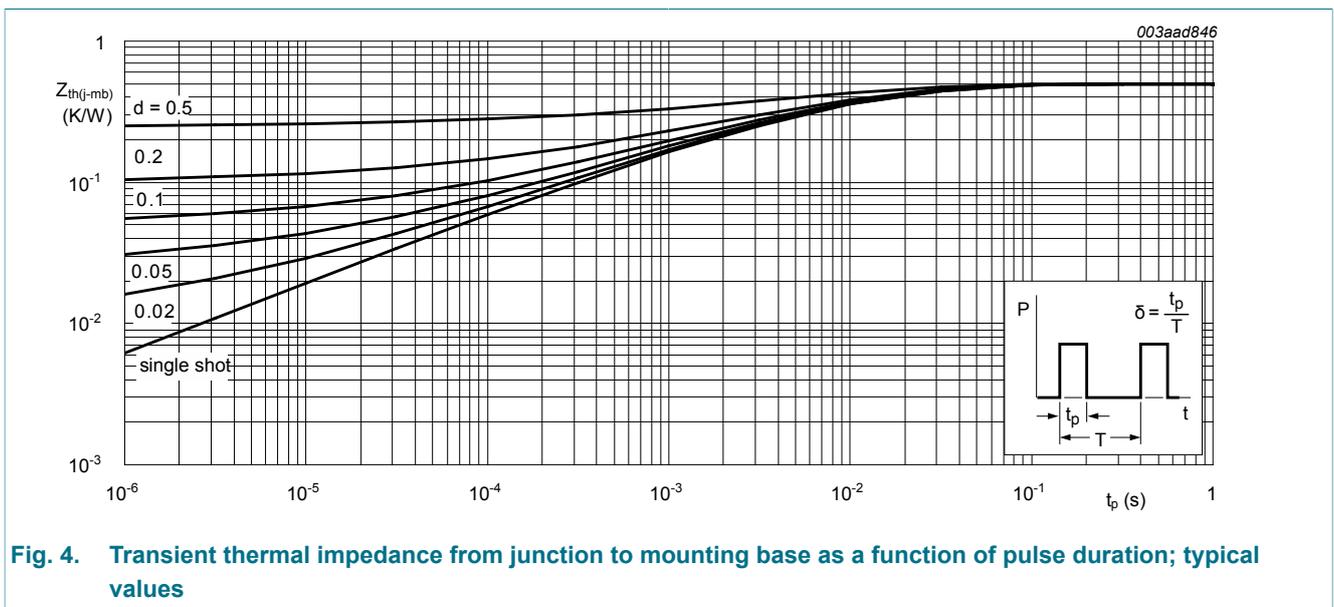




8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.5	1.1	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	54	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	63	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 10 ; Fig. 11	2	3	4	V
V _{GSth}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 11	-	-	4.6	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 11	0.95	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	5	μA
		V _{DS} = 63 V; V _{GS} = 0 V; T _j = 25 °C	-	0.07	7	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 125 °C	-	-	100	μA
		V _{DS} = 63 V; V _{GS} = 0 V; T _j = 125 °C	-	3.25	150	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 175 °C; Fig. 12	-	7.6	12	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; Fig. 12	-	-	8.3	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 13	-	3.6	4	mΩ
R _G	gate resistance	f = 1 MHz	-	0.7	-	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	56	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	47.5	-	nC
Q _{GS}	gate-source charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	18.7	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14	-	10.3	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	8.4	-	nC
Q _{GD}	gate-drain charge	I _D = 75 A; V _{DS} = 30 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15	-	11.2	-	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 30 V; Fig. 14 ; Fig. 15	-	4.9	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$	-	3501	-	pF
C_{oss}	output capacitance	$T_j = 25\text{ °C};$ Fig. 16	-	457	-	pF
C_{rss}	reverse transfer capacitance		-	240	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 0.4\text{ }\Omega; V_{GS} = 10\text{ V};$	-	23	-	ns
t_r	rise time	$R_{G(ext)} = 4.7\text{ }\Omega$	-	24	-	ns
$t_{d(off)}$	turn-off delay time		-	44	-	ns
t_f	fall time		-	14	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ Fig. 17	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	43	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$	-	58	-	nC

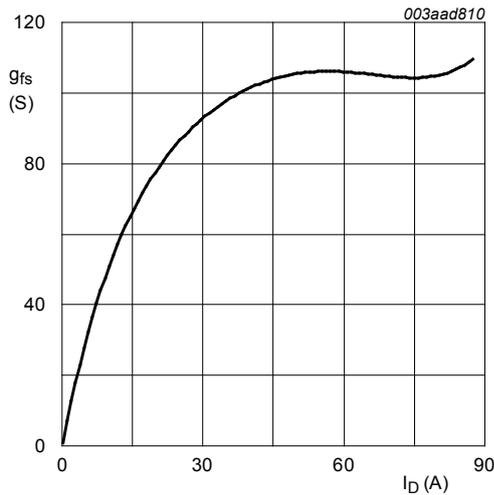


Fig. 5. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ °C}; V_{DS} = 15\text{ V}$

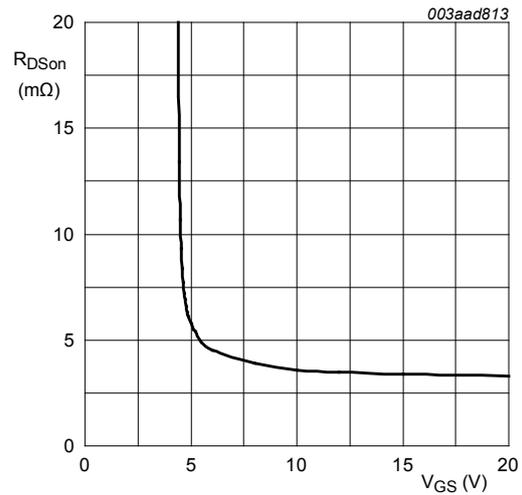


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ °C}; I_D = 25\text{ A}$

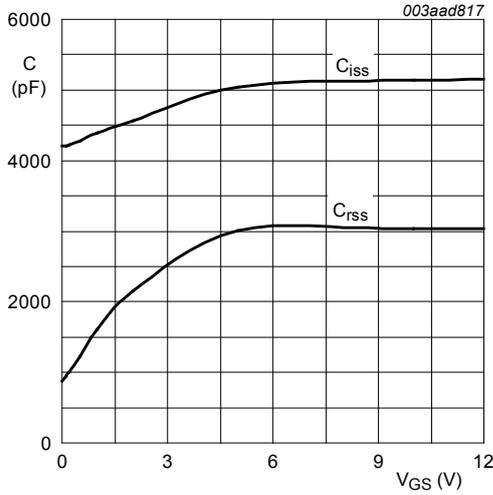


Fig. 7. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$$V_{DS} = 0 \text{ V}; f = 1 \text{ MHz}$$

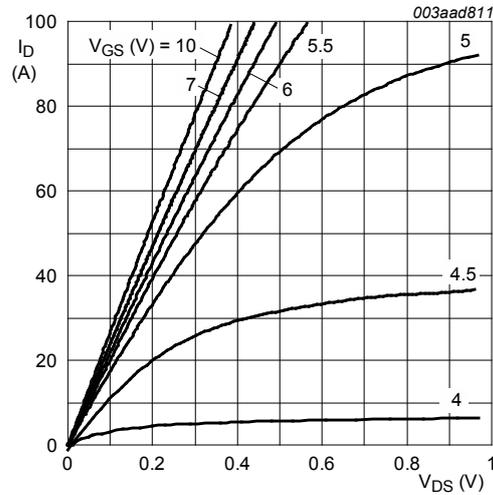


Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$$T_j = 25 \text{ }^\circ\text{C}$$

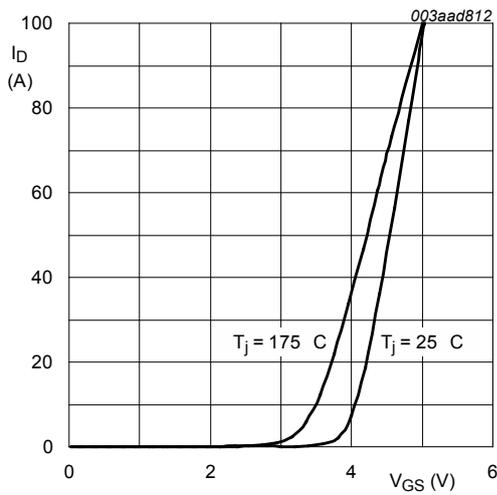


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DSon}$$

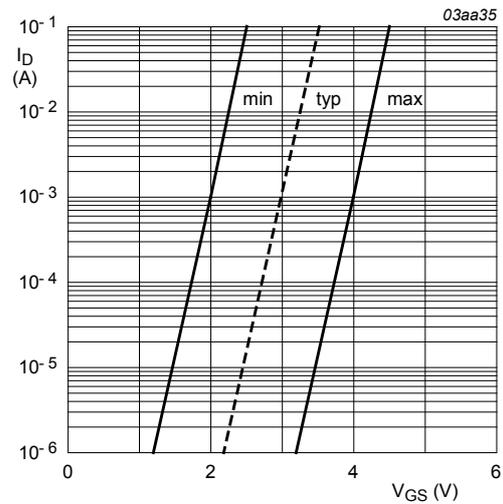


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$$

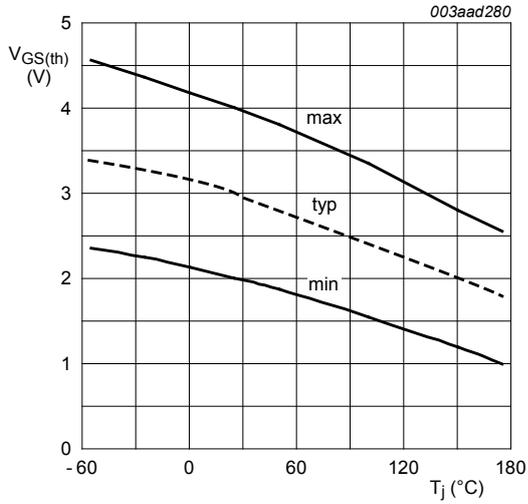


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

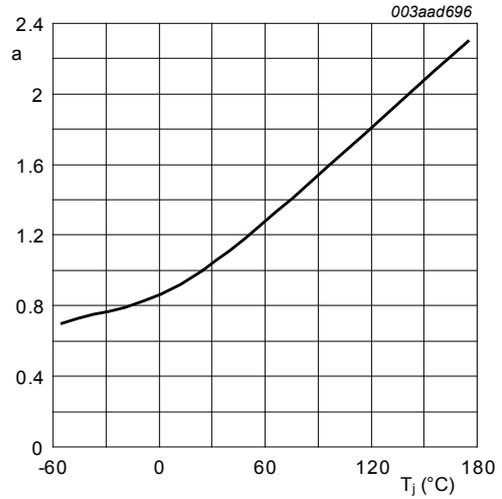


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature.

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

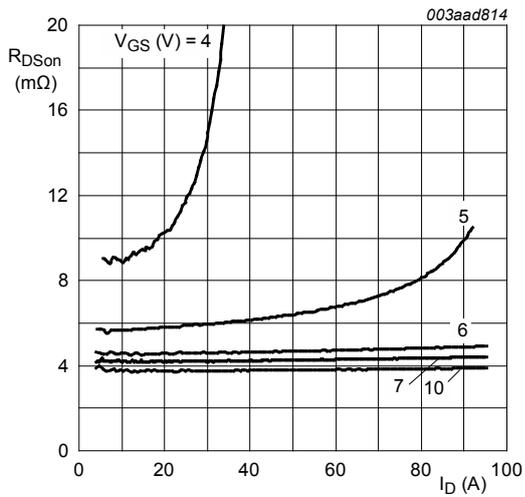


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

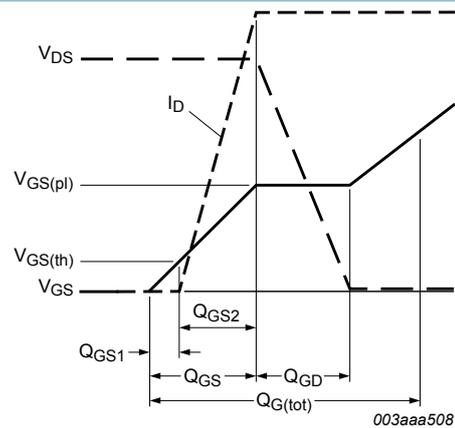


Fig. 14. Gate charge waveform definitions

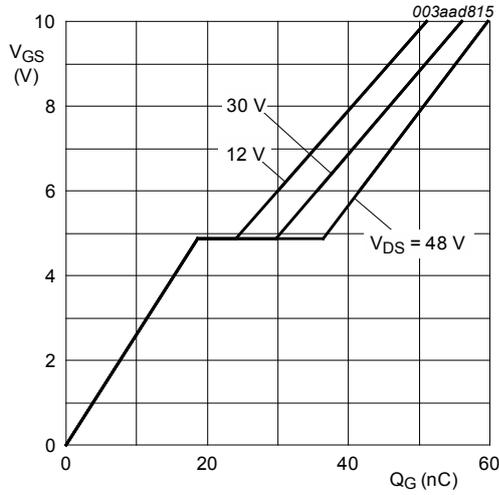


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_J = 25\text{ °C}; I_D = 75\text{ A}$

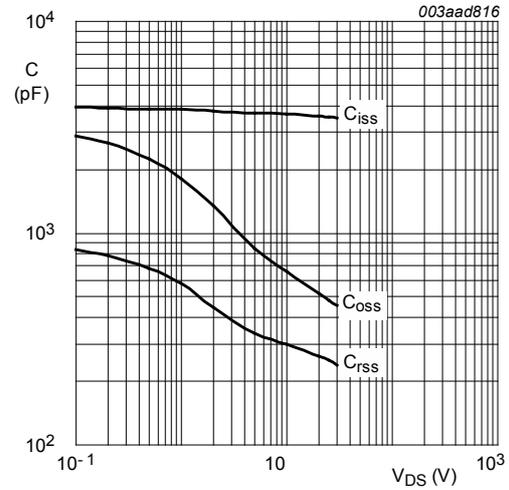


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

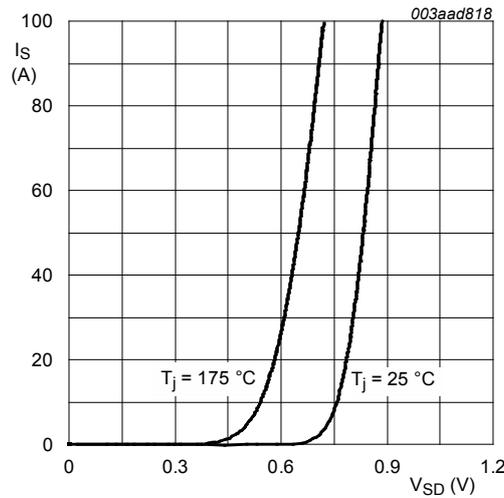
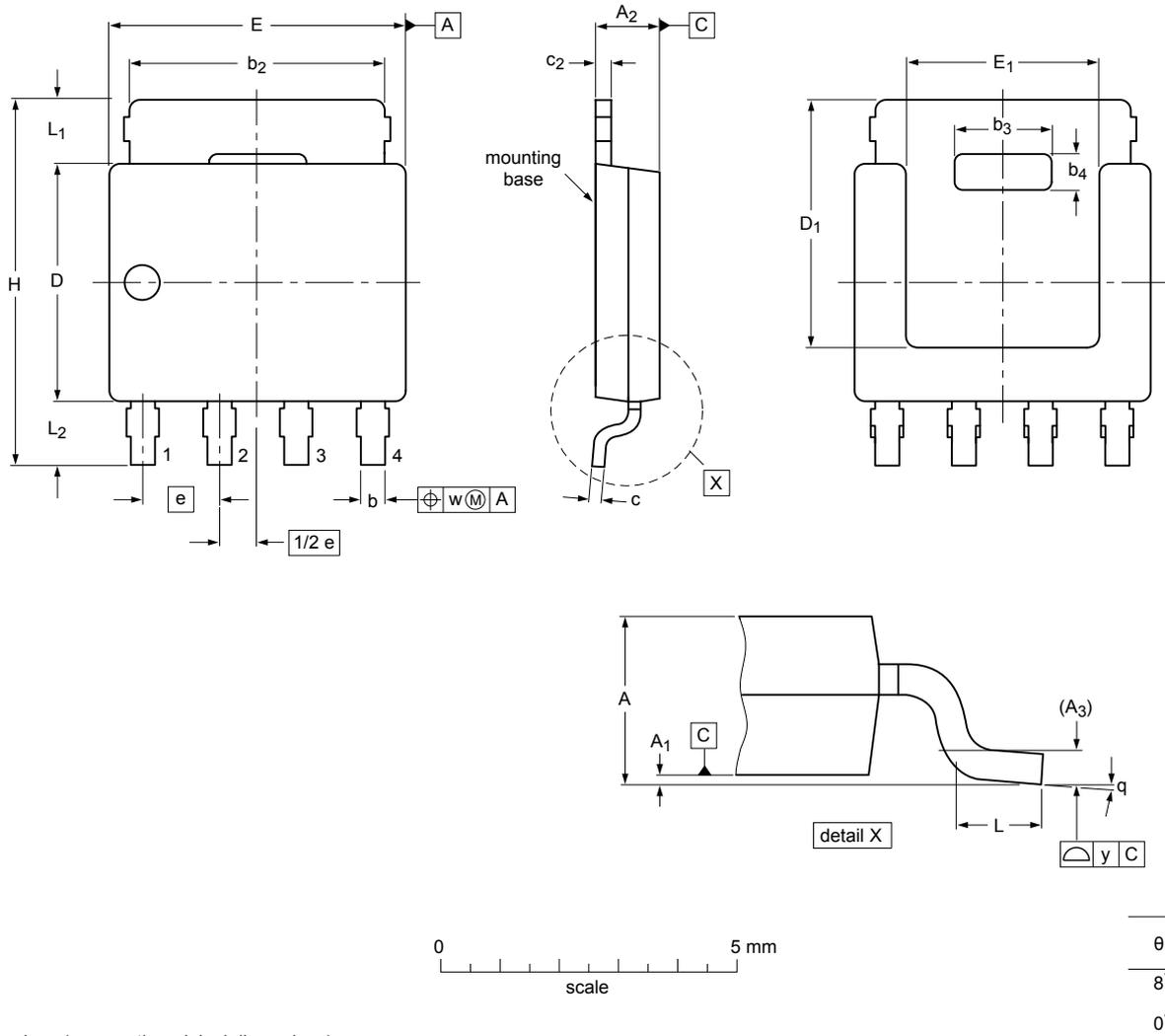


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{ V}$

10. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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