





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

|                                    |                           |                        |
|------------------------------------|---------------------------|------------------------|
| Supply Voltage                     |                           | -0.5V to 3.6V          |
| Input Voltage (all inputs)         |                           | -0.3V to $V_{CC}+0.3V$ |
| Storage Temperature Range          |                           | -65°C to +150°C        |
| Junction Temperature               |                           | +150°C                 |
| Lead Temperature (Soldering 4 Sec) |                           | +260°C                 |
| Package Thermal Resistance         | $\theta_{JA}$ 16-pin WQFN | +43°C/W                |
|                                    | $\theta_{JC}$ 16-pin WQFN | +9°C/W                 |
| ESD Rating (HBM)                   |                           | 8kV                    |
| ESD Rating (MM)                    |                           | 250V                   |

- (1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

## Recommended Operating Conditions

|                                                 |                |
|-------------------------------------------------|----------------|
| Supply Voltage ( $V_{CC} - V_{EE}$ )            | 3.3V $\pm 5\%$ |
| Input Coupling Capacitance                      | 1.0 $\mu F$    |
| AEC Capacitor (Connected between AEC+ and AEC-) | 1.0 $\mu F$    |
| Operating Free Air Temperature ( $T_A$ )        | 0°C to +85°C   |

## DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)(2)</sup>.

| Parameter   |                                           | Test Conditions                    | Reference             | Min | Typ                  | Max | Units             |
|-------------|-------------------------------------------|------------------------------------|-----------------------|-----|----------------------|-----|-------------------|
| $V_{CMIN}$  | Input Common Mode Voltage                 |                                    | SDI, $\overline{SDI}$ |     | 1.9                  |     | V                 |
| $V_{SDI}$   | Input Voltage Swing                       | At LMH0044 input <sup>(3)(4)</sup> |                       | 720 | 800                  | 950 | mV <sub>P-P</sub> |
| $V_{CMOUT}$ | Output Common Mode Voltage                |                                    | SDO, $\overline{SDO}$ |     | $V_{CC} - V_{SDO}/2$ |     | V                 |
| $V_{SDO}$   | Output Voltage Swing                      | 50 $\Omega$ load, differential     |                       |     | 750                  |     | mV <sub>P-P</sub> |
|             | MUTE <sub>REF</sub> DC Voltage (floating) |                                    | MUTE <sub>REF</sub>   |     | 1.3                  |     | V                 |
|             | MUTE <sub>REF</sub> Range                 |                                    |                       |     | 0.7                  |     | V                 |
|             | $\overline{CD}$ Output Voltage            | Carrier not present                | $\overline{CD}$       | 2.6 |                      |     | V                 |
|             |                                           | Carrier present                    |                       |     |                      | 0.4 | V                 |
|             | MUTE Input Voltage                        | Min to mute outputs                | MUTE                  | 3.0 |                      |     | V                 |
|             |                                           | Max to force outputs active        |                       |     |                      | 0.8 | V                 |
| $I_{CC}$    | Supply Current                            | See <sup>(5)</sup>                 |                       |     | 63                   | 77  | mA                |

- (1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to  $V_{EE} = 0$  Volts.
- (2) Typical values are stated for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .
- (3) Specification is ensured by characterization.
- (4) The maximum input voltage swing assumes a nonstressing, DC-balance signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.
- (5) Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Refer to [Figure 2](#) and [Figure 3](#).

## AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)</sup>.

| Parameter                                                         | Test Conditions                                        | Reference                    | Min | Typ   | Max  | Units |
|-------------------------------------------------------------------|--------------------------------------------------------|------------------------------|-----|-------|------|-------|
| BR <sub>MIN</sub>                                                 | Minimum Input Data Rate                                | SDI, $\overline{\text{SDI}}$ |     | 125   |      | Mbps  |
| BR <sub>MAX</sub>                                                 | Maximum Input Data Rate                                |                              |     |       | 1485 | Mbps  |
| Jitter for various Cable Lengths<br>(with equalizer pathological) | 270 Mbps, Belden 1694A,<br>400 meters <sup>(2)</sup>   |                              |     | 0.2   |      | UI    |
|                                                                   | 270 Mbps, Belden 8281,<br>280 meters <sup>(2)</sup>    |                              |     | 0.2   |      | UI    |
|                                                                   | 1.485 Gbps, Belden 1694A,<br>140 meters <sup>(2)</sup> |                              |     | 0.25  |      | UI    |
|                                                                   | 1.485 Gbps, Belden 8281,<br>100 meters <sup>(2)</sup>  |                              |     | 0.25  |      | UI    |
|                                                                   | 1.485 Gbps, Belden 1694A,<br>200 meters <sup>(2)</sup> |                              |     | 0.3   |      | UI    |
| t <sub>r</sub> , t <sub>f</sub>                                   | Output Rise Time, Fall Time                            | SDO, $\overline{\text{SDO}}$ |     | 100   | 220  | ps    |
|                                                                   | Mismatch in Rise/Fall Time                             |                              |     | 2     | 15   | ps    |
| t <sub>OS</sub>                                                   | Output Overshoot                                       |                              |     | 1     | 5    | %     |
| R <sub>OUT</sub>                                                  | Output Resistance                                      |                              |     | 50    |      | Ω     |
| RL <sub>IN</sub>                                                  | Input Return Loss                                      | SDI, $\overline{\text{SDI}}$ | 15  | 18-20 |      | dB    |
| R <sub>IN</sub>                                                   | Input Resistance                                       |                              |     | 1.3   |      | kΩ    |
| C <sub>IN</sub>                                                   | Input Capacitance                                      |                              |     | 1     |      | pF    |

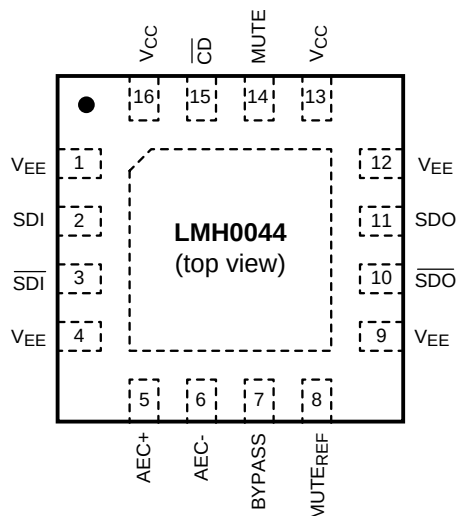
(1) Typical values are stated for V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C.

(2) Specification is ensured by characterization.

(3) Specification is ensured by design.

(4) Input return loss is dependent on board design. The LMH0044 meets this specification on the SD044 evaluation board from 5 MHz to 1.5 GHz.

## Connection Diagram

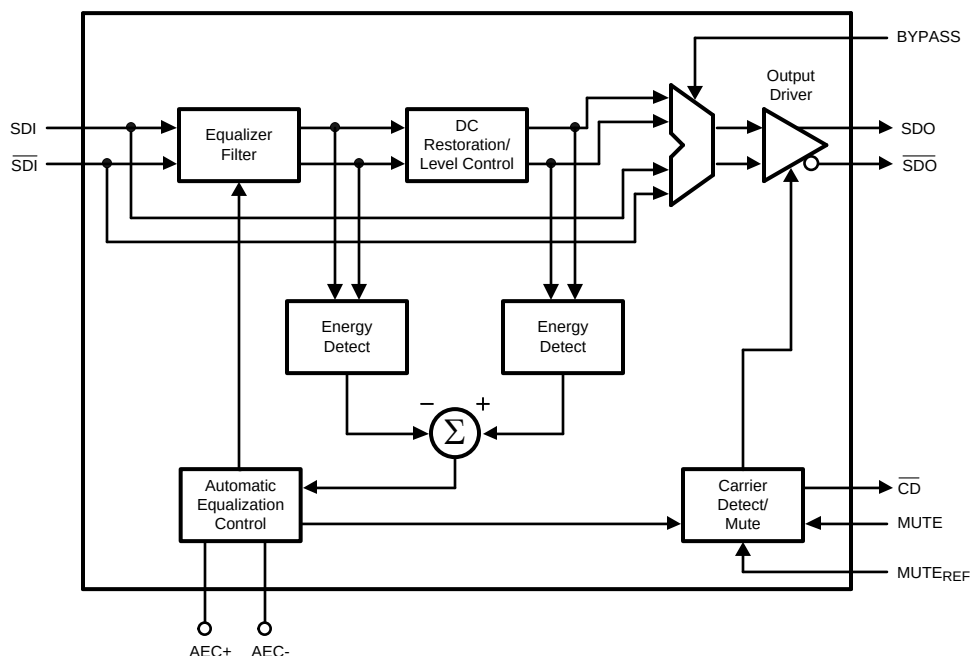


The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

**Figure 1. 16-Pin WQFN Package**  
See Package Number RUM0016A

**Table 1. Pin Descriptions**

| Pin No. | Name                    | Description                                                                                                                                                                                                                                                                                      |
|---------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | $V_{EE}$                | Negative power supply (ground).                                                                                                                                                                                                                                                                  |
| 2       | SDI                     | Serial data true input.                                                                                                                                                                                                                                                                          |
| 3       | $\overline{\text{SDI}}$ | Serial data complement input.                                                                                                                                                                                                                                                                    |
| 4       | $V_{EE}$                | Negative power supply (ground).                                                                                                                                                                                                                                                                  |
| 5       | AEC+                    | AEC loop filter external capacitor (1 $\mu$ F) positive connection.                                                                                                                                                                                                                              |
| 6       | AEC-                    | AEC loop filter external capacitor (1 $\mu$ F) negative connection.                                                                                                                                                                                                                              |
| 7       | BYPASS                  | Bypasses equalization and DC restoration when high. No equalization occurs in this mode.                                                                                                                                                                                                         |
| 8       | MUTE <sub>REF</sub>     | Mute reference. Sets the threshold for $\overline{\text{CD}}$ and (with $\overline{\text{CD}}$ tied to MUTE) determines the maximum cable to be equalized before muting. MUTE <sub>REF</sub> may be unconnected for maximum equalization.                                                        |
| 9       | $V_{EE}$                | Negative power supply (ground).                                                                                                                                                                                                                                                                  |
| 10      | $\overline{\text{SDO}}$ | Serial data complement output.                                                                                                                                                                                                                                                                   |
| 11      | SDO                     | Serial data true output.                                                                                                                                                                                                                                                                         |
| 12      | $V_{EE}$                | Negative power supply (ground).                                                                                                                                                                                                                                                                  |
| 13      | $V_{CC}$                | Positive power supply (+3.3V).                                                                                                                                                                                                                                                                   |
| 14      | MUTE                    | Output mute. To disable the mute function and enable the output, MUTE must be tied to GND or a low level signal. To force the outputs to a muted state, tie to $V_{CC}$ . CD may be tied to this pin to inhibit the output when no input signal is present. MUTE has no function in BYPASS mode. |
| 15      | $\overline{\text{CD}}$  | Carrier detect. $\overline{\text{CD}}$ is high when no signal is present. $\overline{\text{CD}}$ has no function in BYPASS mode.                                                                                                                                                                 |
| 16      | $V_{CC}$                | Positive power supply (+3.3V).                                                                                                                                                                                                                                                                   |
| DAP     | $V_{EE}$                | Connect exposed DAP to negative power supply.                                                                                                                                                                                                                                                    |

**Block Diagram**

## Device Operation

### BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1μF capacitor placed across the AEC+ and AEC- pins.

The **Carrier Detect / Mute** block generates the carrier detect signal and controls the mute function of the output. This block utilizes the  $\overline{\text{CD}}$  and **MUTE** signals along with **Mute Reference (MUTE<sub>REF</sub>)**.

The **Output Driver** produces SDO and  $\overline{\text{SDO}}$ .

### MUTE REFERENCE (MUTE<sub>REF</sub>)

The mute reference sets the threshold for  $\overline{\text{CD}}$  and (with  $\overline{\text{CD}}$  tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. As the applied MUTE<sub>REF</sub> voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE<sub>REF</sub> may be left unconnected for maximum equalization before muting.

### CARRIER DETECT ( $\overline{\text{CD}}$ ) AND MUTE

Carrier detect  $\overline{\text{CD}}$  indicates if a valid signal is present at the LMH0044 input. If MUTE<sub>REF</sub> is used, the carrier detect threshold will be altered accordingly.  $\overline{\text{CD}}$  provides a high voltage when no signal is present at the LMH0044 input.  $\overline{\text{CD}}$  is low when a valid input signal is detected.

MUTE can be used to manually mute or enable SDO and  $\overline{\text{SDO}}$ . Applying a high input to MUTE will mute the LMH0044 outputs. Applying a low input will force the outputs to be active.

$\overline{\text{CD}}$  and MUTE may be tied together to automatically mute the output when no input signal is present.

### INPUT INTERFACING

The LMH0044 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The LMH0044 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

### OUTPUT INTERFACING

The SDO and  $\overline{\text{SDO}}$  outputs are internally loaded with 50Ω. They produce a 750 mV<sub>P-P</sub> differential output, or a 375 mV<sub>P-P</sub> single-ended output.

## APPLICATION INFORMATION

### PCB LAYOUT RECOMMENDATIONS

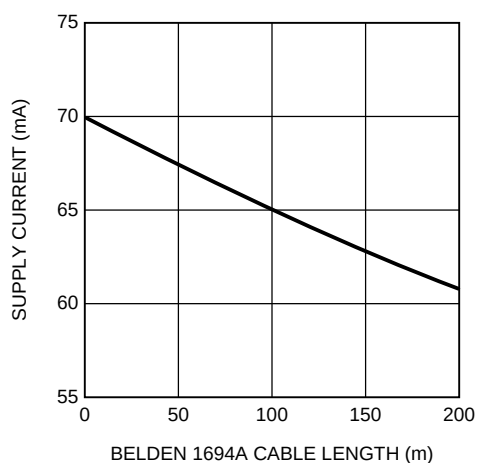
Refer to the following Application Note on TI's website: [AN-1372](#), "LMH0034 PCB Layout Techniques." The PCB layout techniques in the application note apply to the LMH0044 as well.

### REPLACING THE GENNUM GS1574A

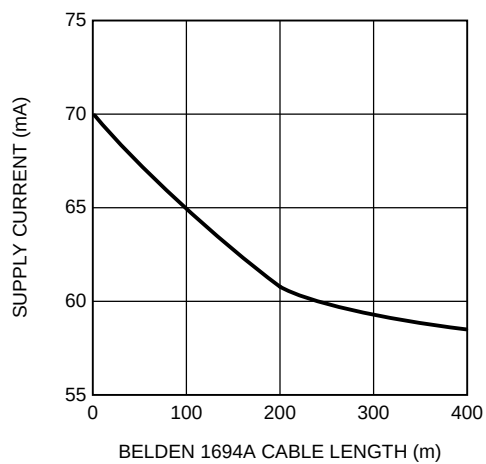
The LMH0044 is footprint compatible with the Gennum GS1574A.

### SUPPLY CURRENT VS. CABLE LENGTH

The supply current ( $I_{CC}$ ) depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. [Figure 2](#) shows supply current vs. Belden 1694A cable length for 1.485 Gbps data and [Figure 3](#) shows supply current vs. Belden 1694A cable length for 270 Mbps data.



**Figure 2. Supply Current vs. Belden 1694A Cable Length, 1.485 Gbps**



**Figure 3. Supply Current vs. Belden 1694A Cable Length, 270 Mbps**

## REVISION HISTORY

| Changes from Revision D (April 2013) to Revision E         | Page              |
|------------------------------------------------------------|-------------------|
| • Changed layout of National Data Sheet to TI format ..... | <a href="#">7</a> |



## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMH0044SQ/NOPB   | ACTIVE        | WQFN         | RUM                | 16   | 1000           | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | 0 to 85      | L044                    | <a href="#">Samples</a> |
| LMH0044SQE/NOPB  | ACTIVE        | WQFN         | RUM                | 16   | 250            | Green (RoHS<br>& no Sb/Br) | CU SN                   | Level-1-260C-UNLIM   | 0 to 85      | L044                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

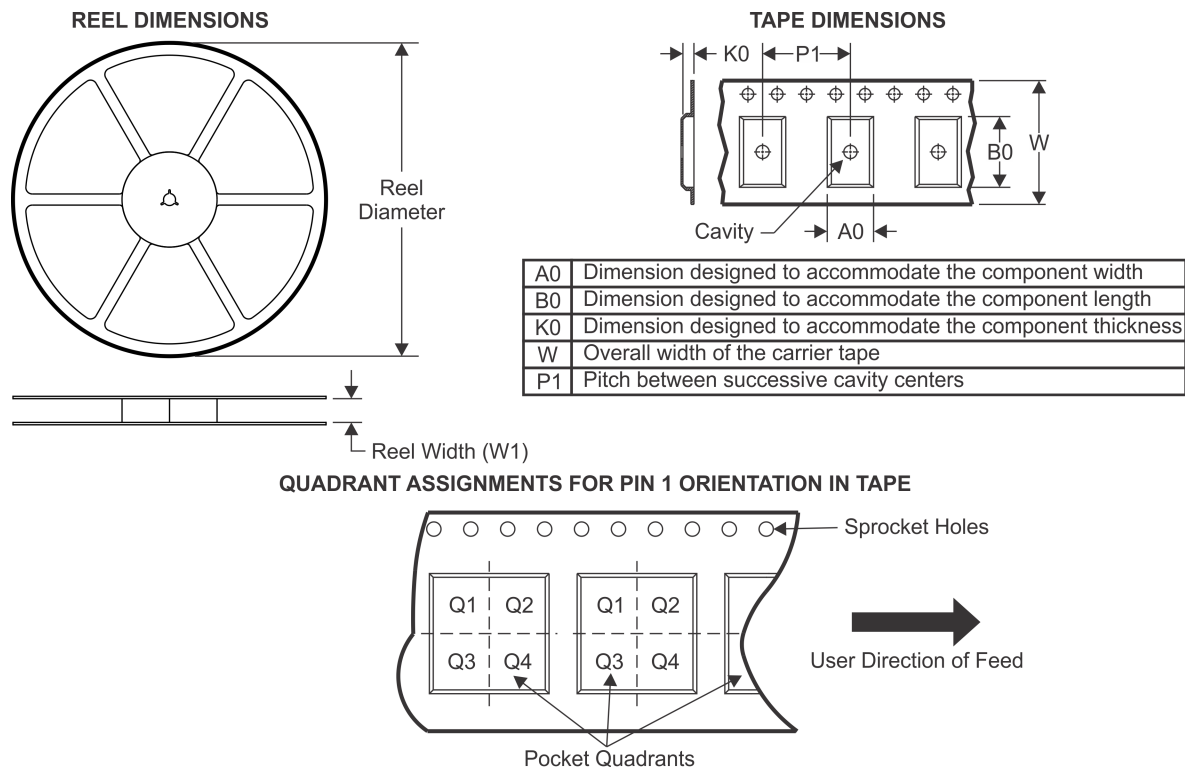
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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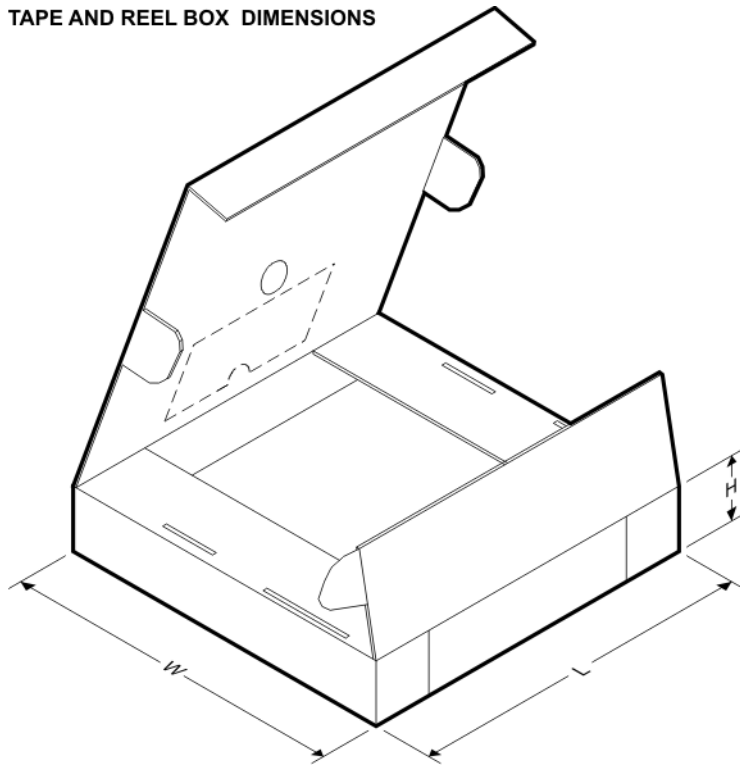
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH0044SQ/NOPB  | WQFN         | RUM             | 16   | 1000 | 178.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |
| LMH0044SQE/NOPB | WQFN         | RUM             | 16   | 250  | 178.0              | 12.4               | 4.3     | 4.3     | 1.3     | 8.0     | 12.0   | Q1            |

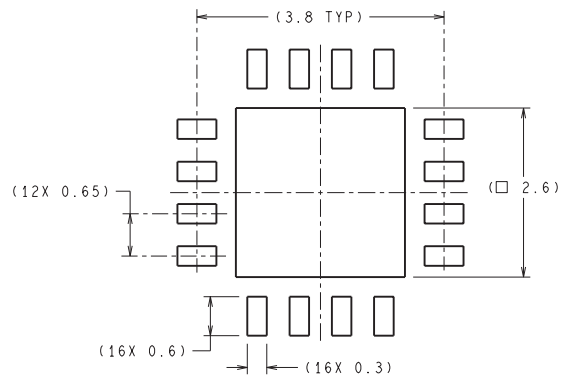
## TAPE AND REEL BOX DIMENSIONS



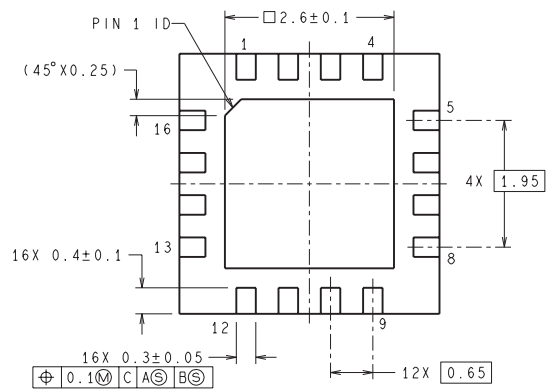
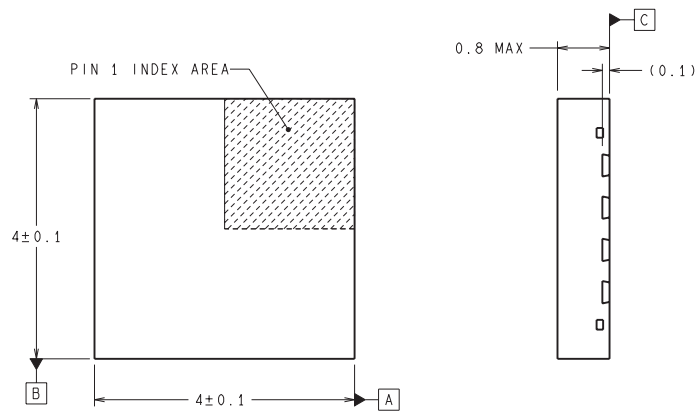
\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH0044SQ/NOPB  | WQFN         | RUM             | 16   | 1000 | 210.0       | 185.0      | 35.0        |
| LMH0044SQE/NOPB | WQFN         | RUM             | 16   | 250  | 210.0       | 185.0      | 35.0        |

RUM0016A



## RECOMMENDED LAND PATTERN



SQB16A (Rev A)

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