Reset Timer IC for Mobile Equipments

NO.EA-280-140604

OUTLINE

The R3200x is a reset timer IC with two input signals for mobile equipment which require long interval for reset sequence. The long interval prevents unexpected resets caused by accidental key operations. Internally, the R3200x consists of a delay generator circuit and output driver transistors.
The R3200x has two active-low input pins ($\overline{SR0}$ and $\overline{SR1}$) which generate reset signals after output delay time when both active-low input pins are activated at the same time.
The R3200x has two versions that are different in output delay time settings and output release method.

R3200x001x:
Output delay time is selectable from 7.5 s or 11.25 s typ. by connecting the DSR pin to either GND or V_{DD}. A reset signal can be released by making one of the active-low input pins high.

R3200xxx2x, R3200L053B or R3200L064A:
Output delay time is fixed. A reset signal will be released automatically after output release time. Or, by making one of the active-low input pins high, a reset signal can be released before output release time.

The R3200x provides ultra-low supply current while a reset signal is remaining active or after being sent out.
The R3200x is offered in a 8-pin DFN(PLP)2020-8B package or a 8-pin DFN1216-8 package.

FEATURES

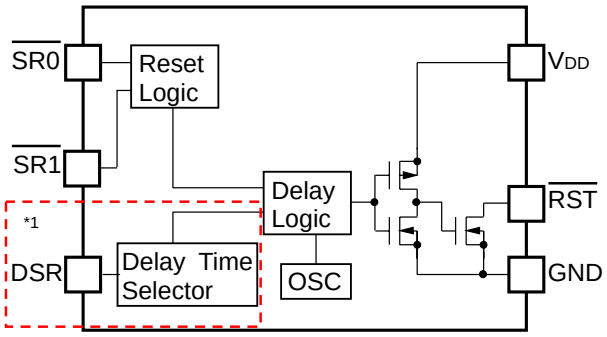
- Operating Voltage Range (Maximum Rating)..... 1.65 V to 5.5 V (6 V)
- Supply Current 1 (at standby) ..... Typ. 0.28 µA (V_{DD} = 5.5 V)
- Supply Current 2 (at active before reset signal output)..... Typ. 3 µA (V_{DD} = 5.5 V)*1
- Supply Current 3 (at active after reset signal output)..... Typ. 0.45 µA (V_{DD} = 5.5 V)
- Operating Temperature Range..... −40 to +85°C
- Output Delay Time (R3200x001x)..... Typ. 7.5 s or 11.25 s
  (R3200x002x) ..... Typ. 7.5 s
  (R3200L052B)..... Typ. 10 s
  (R3200L053B) ..... Typ. 10 s
  (R3200L064A)..... Typ. 3.0 s
- Output Delay Time Accuracy .....±10%
- Output Release Time (R3200x002x) .....Typ. 0.234 s
  (R3200L052B).....Typ. 0.313 s
  (R3200L053B).....Typ. 0.078 s
  (R3200L064A)..... Typ. 0.1875 s
- Output Release Time Accuracy..... ±10%
- Output Type (R3200xxxxA)..... Nch Open Drain
  (R3200xxxxB)..... Nch Open Drain and CMOS
- Packages ..... DFN(PLP)2020-8B, DFN1216-8

*1 Guaranteed by design engineering

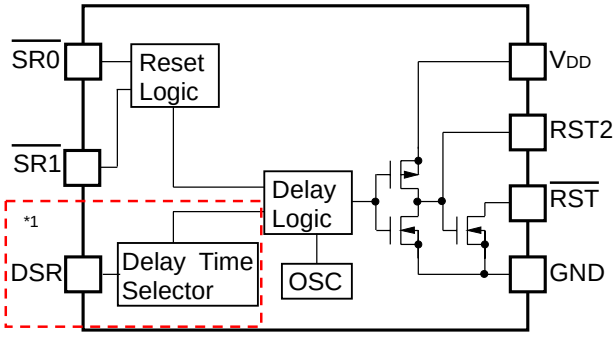
APPLICATIONS

- Mobile phone, Smartphone
- Tablet devices such as E-book etc.
- Portable Games
- Personal Navigation Devices

BLOCK DIAGRAMS



R3200xxxxA



R3200xxxxB

*1 The parts surrounded by red dotted lines are for the R3200x001x only.

SELECTION GUIDE

The package type, the combination of output delay time and output release time, the output type for the device are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3200Kxxx∗-TR	DFN(PLP)2020-8B	5,000 pcs	Yes	Yes
R3200Lxxx∗-E2	DFN1216-8	5,000 pcs	Yes	Yes

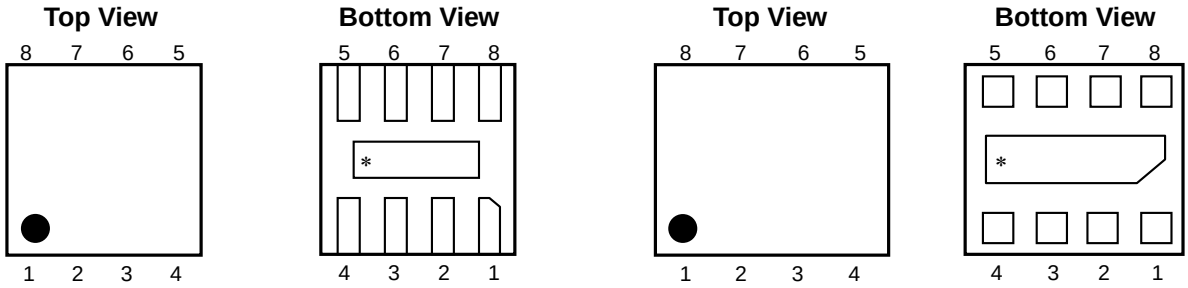
xxx: Specify the combination of output delay time and output release method.
(001) Select the output delay time from 7.5 s or 11.25 s typ.
A reset signal can be released by making one of the active-low input pins high.

(xx2) / (053) / (064)
A reset signal will be released automatically after output release time.
A reset signal can be released before output release time by making one of the active-low input pins high.
Refer to the table below for the output delay time and the output release time for each device.

	Output Delay Time	Output Release Time
002	7.5 s	0.234 s
052 (R3200L052B only)	10 s	0.313 s
053 (R3200L053B only)	10 s	0.078 s
064 (R3200L064A only)	3.0 s	0.1875 s

∗: Specify the output type.
(A) Nch Open Drain
(B) Nch Open Drain and CMOS

PIN DESCRIPTIONS



DFN(PLP)2020-8B **DFN1216-8**

∗ The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

DFN(PLP)2020-8B Pin Description/ DFN1216-8 Pin Description

Pin No.	Symbol	Description
1	NC	No Connection (R3200xxxxA)
	RST2	CMOS Output Pin, Active-high (R3200xxxxB)
2	GND	Ground Pin
3	$\overline{SR1}$	Input Pin2, Active-low*1
4	$\overline{RST}$	Nch Open Drain Output Pin, Active-low*2
5	DSR	Output Delay Time Selection Pin (R3200x001x) (GND: 7.5 s, V_{DD}: 11.25 s)*3
	TEST2	Test Pin 2*4 (R3200xxx2x/ R3200L053B/ R3200L064A)
6	TEST	Test Pin*4
7	$\overline{SR0}$	Input Pin1, Active-low*1
8	V_{DD}	Power Supply Input Pin

*1 When only one active-low input pin is used, connect the unused one to GND.
*2 The $\overline{RST}$ pin must be connected to GND or left floating if it is not used (Ex.R3200xxxxB).
*3 The DSR pin must be connected to GND or V_{DD}.
*4 The TEST pin and the TEST2 pin must be connected to GND when they are used.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item	Rating		Unit
V_{DD}	Supply Voltage	GND −0.3 to 6		V
V_{SR0}	Input Voltage (Input Pin1)	GND −0.3 to 6		V
V_{SR1}	Input Voltage (Input Pin2)	GND −0.3 to 6		V
V_{RST}	Output Voltage (Reset Signal Output Pin1)	GND −0.3 to 6		V
V_{RST2}	Output Voltage (Reset Signal Output Pin2)	GND −0.3 to V_{DD} +0.3		V
V_{DSR}	Input Voltage (Output Delay Time Selection Pin) (R3200x001x)	GND −0.3 to 6		V
I_{OUT}	Output Current	20		mA
P_D	Power Dissipation (Standard Land Pattern)*1	DFN(PLP)2020-8B	880	mW
		DFN1216-8	625	
Ta	Operating Temperature Range	−40 to +85		°C
Tstg	Storage Temperature Range	−55 to +125		°C

*1 Refer to *PACKAGE INFORMATION* for detailed information.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

The specifications surrounded by ▭ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

R3200x001x Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage			1.65		5.5	V
I_{SS1}	Supply Current 1*1	V_{DD} = 5.5 V (at standby)			0.28	1.35	µA
I_{SS2}	Supply Current 2*2	V_{DD} = 5.5 V (at active before reset signal output)			3.0	6.5	µA
I_{SS3}	Supply Current 3*3	V_{DD} = 5.5 V (at active after reset signal output)			0.45	1.7	µA
V_{OL}	"L" Output Voltage	V_{DD} ≥ 4.5 V	I_{OL} = 8 mA			0.3	V
		V_{DD} ≥ 3.3 V	I_{OL} = 5 mA				
		V_{DD} ≥ 1.65 V	I_{OL} = 3 mA				
V_{OH}	"H" Output Voltage*4	V_{DD} ≥ 4.5 V	I_{OH} = 5 mA	V_{DD} x 0.85			V
		V_{DD} ≥ 3.3 V	I_{OH} = 2.5 mA				
		V_{DD} ≥ 1.65 V	I_{OH} = 0.8 mA				
I_{LEAKI}	$\overline{SR0}$, $\overline{SR1}$ Input Leakage Current	V_{DD} = 5.5 V				0.1	µA
I_{LEAKO}	Output Leakage Current	V_{DD} = 5.5 V				0.1	µA
tdelay	Output Delay Time	DSR = GND		6.75	7.5	8.25	s
		DSR = V_{DD}		10.125	11.25	12.375	s
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ "L" Input Voltaget					0.3	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ "H" Input Voltaget			0.85			V

All test items listed under *ELECTRICAL CHARACTERISTICS* are done under the pulse load condition (Tj ≈ Ta = 25°C) except Supply Current 2.

*1 Supply current when the device is active and waiting for the reset input.

*2 Supply current when both active-low input pins are low and the timer operation is running.

*3 Supply current after the completion of timer operation and the output of reset signal.

*4 For the R3200xxxxB only (CMOS output).

ELECTRICAL CHARACTERISTICS (continued)

The specifications surrounded by ▭ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

R3200xxx2x, R3200L053B, R3200L064A Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage			1.65		5.5	V
I_{SS1}	Supply Current 1*1	V_{DD} = 5.5 V (at standby)			0.28	1.35	µA
I_{SS2}	Supply Current 2*2	V_{DD} = 5.5 V (at active before reset signal output)			3.0	6.5	µA
I_{SS3}	Supply Current 3*3	V_{DD} = 5.5 V (at active after reset signal output)			0.45	1.7	µA
V_{OL}	"L" Output Voltage	V_{DD} ≥ 4.5 V	I_{OL} = 8 mA			0.3	V
		V_{DD} ≥ 3.3 V	I_{OL} = 5 mA				
		V_{DD} ≥ 1.65 V	I_{OL} = 3 mA				
V_{OH}	"H" Output Voltage*4	V_{DD} ≥ 4.5 V	I_{OH} = 5 mA	V_{DD} x 0.85			V
		V_{DD} ≥ 3.3 V	I_{OH} = 2.5 mA				
		V_{DD} ≥ 1.65 V	I_{OH} = 0.8 mA				
I_{LEAKI}	$\overline{SR0}$, $\overline{SR1}$ Input Leakage Current	V_{DD} = 5.5 V				0.1	µA
I_{LEAKO}	Output Leakage Current	V_{DD} = 5.5 V				0.1	µA
tdelay	Output Delay Time*5			tdelay_s x 0.9	tdelay_s	tdelay_s x 1.1	sec
trec	Output Release Time*5			trec_s x 0.9	trec_s	trec_s x 1.1	sec
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ "L" Input Voltage					0.3	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ "H" Input Voltage			0.85			V

All test items listed under *ELECTRICAL CHARACTERISTICS* are done under the pulse load condition (Tj ≈ Ta = 25°C) except Supply Current 2.

*1 Supply current when the device is active and waiting for the reset input.

*2 Supply current when both active-low input pins are low and the timer operation is running.

*3 Supply current after the automatic cancellation of reset signal following the completion of timer operation and the output of rest signal.

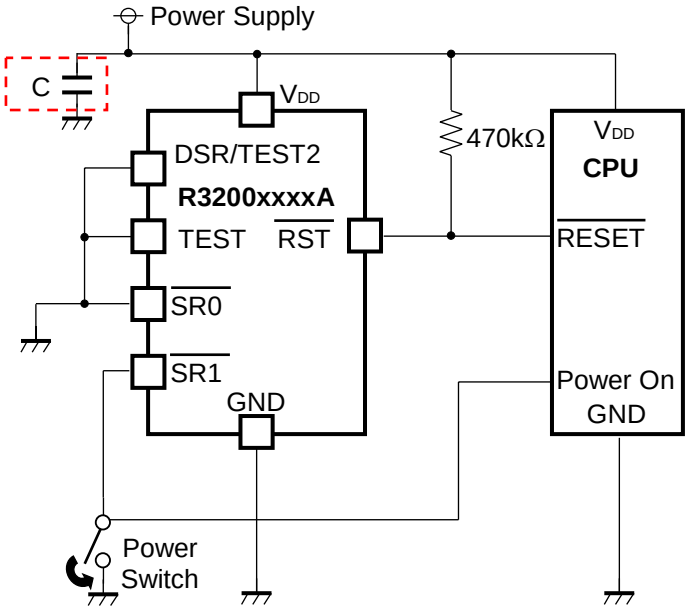
*4 For the R3200xxxxB only (CMOS output).

*5 Refer to *Output Delay Time and Output Release Time of R3200x*.

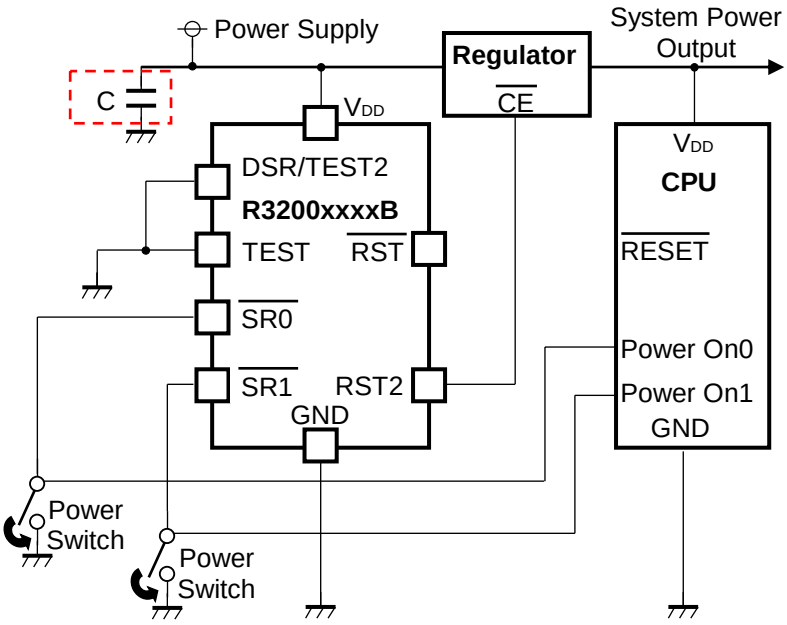
Output Delay Time and Output Release Time of R3200x

Product Name	tdelay_s	trec_s
R3200x002x	7.5 s	0.234 s
R3200L052B	10 s	0.313 s
R3200L053B	10 s	0.078 s
R3200L064A	3.0 s	0.1875 s

TYPICAL APPLICATIONS



R3200xxxxA Typical Application



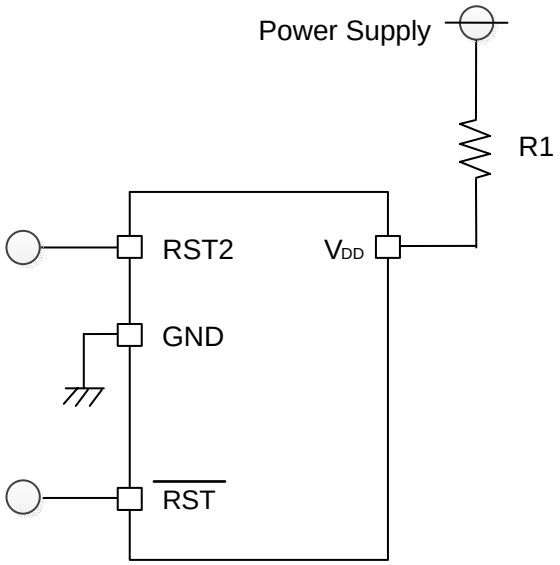
R3200xxxxB Typical Application

A bypass capacitor between the power supply line and the GND line is not necessarily required. If the device operation is affected by power supply noise, connect an appropriately selected bypass capacitor.

TECHNICAL NOTES

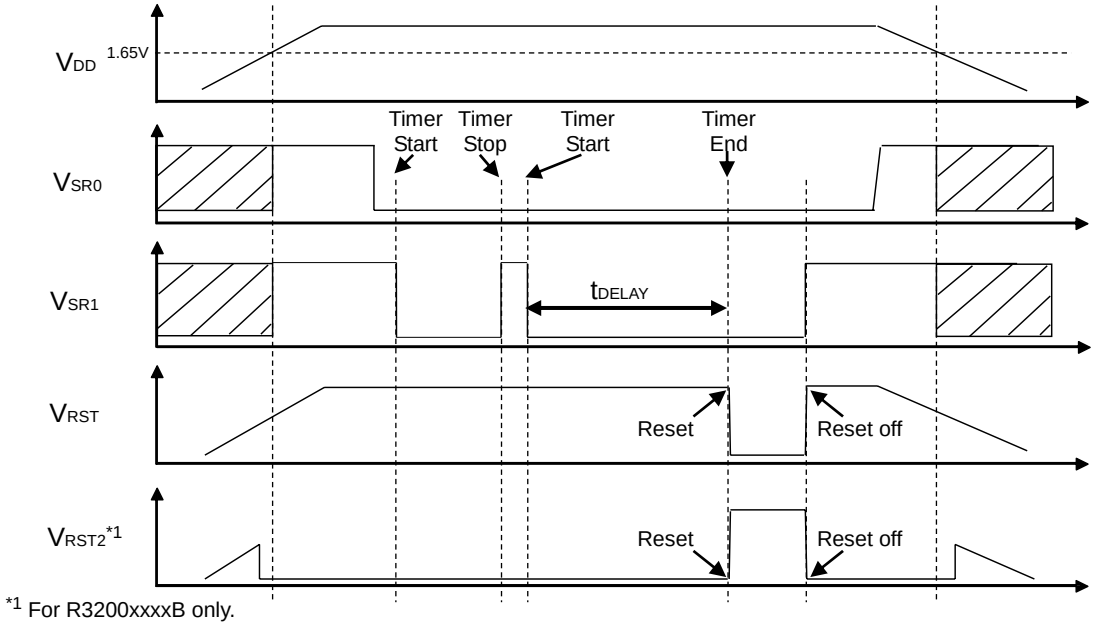
The performance of power source circuits using this device largely depends on the peripheral circuits. When selecting the peripheral components, consider the conditions of use. Do not allow each component, PCB pattern and the device to exceed their respected rated values (voltage, current and power) when designing the peripheral circuits.

- When only one active-low input pins is used (refer to *R3200xxxxA Typical Application*) connect the unused one to GND.
- In the case of applying the following circuit configuration to the R3200x, the supply current of the device itself may cause significant voltage drop on the V_{DD} pin if the R1 value is high. As a result, the V_{DD} voltage may fall below the minimum operating voltage.



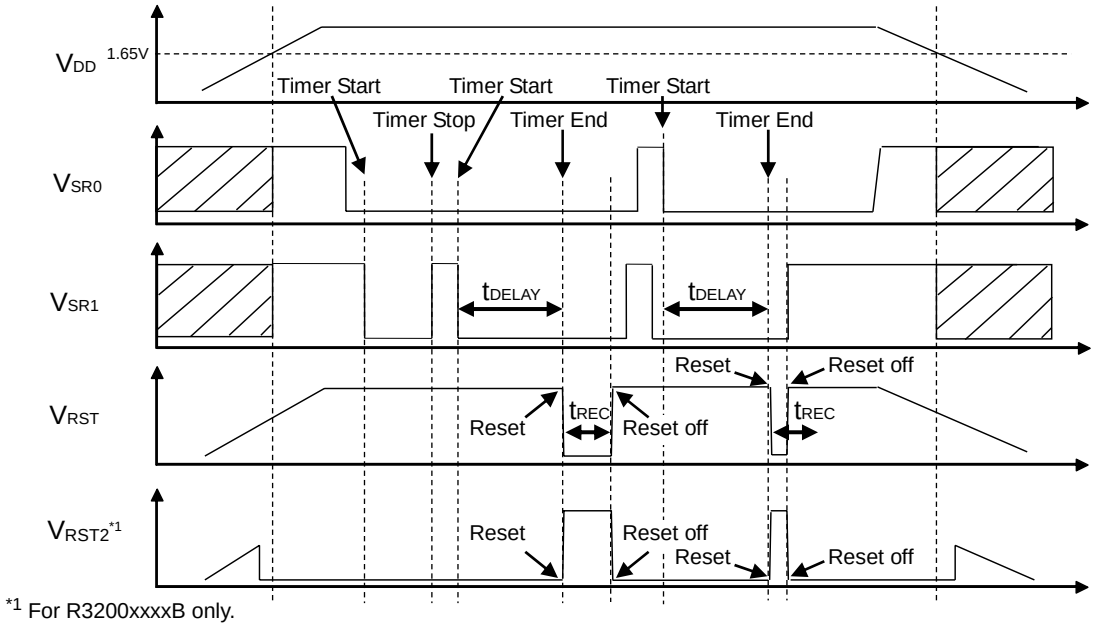
Circuit Configuration Example

THEORY OF OPERATION



R3200x001x Timing Chart

- When both active-low input pins become the low voltage level, the timer operation starts. After the output delay time (tdelay), a reset signal will be sent out. When one of the active-low input pins becomes the high voltage level, the timer operation stops.
- During tdealy, if one of the active-low input pins becomes the high voltage level, the timer operation stops. If both active-low input pins become the low voltage level again, a reset signal will be sent out after tdelay.
- A reset signal will be released if one of the active-low input pins becomes the high voltage level. Until one of the active-low input pins becomes the high voltage level, a reset signal will be continually sent out.
- tdelay can be selected from 7.5 s or 11.25 s typ. by connecting the DSR pin to either GND or V_{DD}. However, if the DSR pin is switched during the operations, the output would become unstable and may cause false operations. Switching of the DSR pin must be done during power-off.
  Also, the DSR pin must be connected to either GND or V_{DD}, otherwise the output would become unstable and may cause false operations.

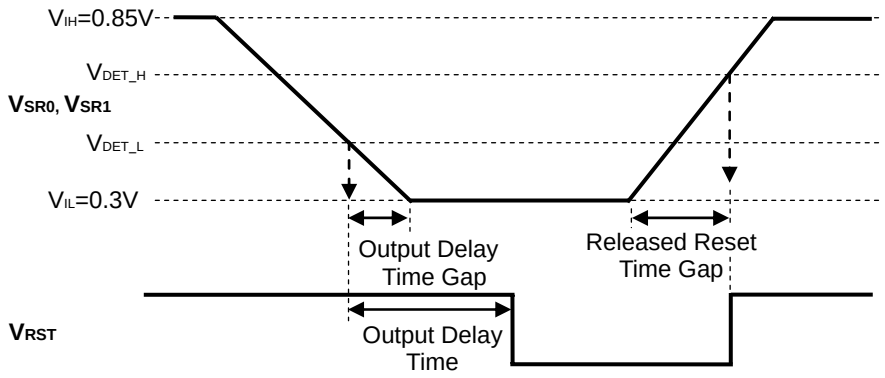


R3200xxx2x, R3200L053B, R3200L064A Timing Chart

- When both active-low input pins become the low voltage level, the timer operation starts. After the output delay time (tdelay), a reset signal will be sent out. If one of the active-low input pins becomes the high voltage level, the timer operation stops.
- During tdelay, if one of the active-low input pins becomes the high voltage level, the timer operation stops. If both active-low input pins become the low voltage level again, a reset signal will be sent out after tdelay.
- A reset signal will be released automatically after the reset delay time (trec), or it will be released if one of the active-low input pins becomes the high voltage level.

OUTPUT DELAY TIME GAP

The threshold voltages of the active-low input pins are between V_{IL} and V_{IH}. Therefore, if the rising or falling slew rate is very slow, the timer will start at the point of crossing the threshold voltage and may cause errors in the output delay time (tdelay) and the output release time (trec).



Relation between the Rising and Falling Slew Rate and the Time Gap

V_{DD} START-UP DURING LOW INPUT

When starting up V_{DD} at slow slew rate of 0.001 V/µs or less while the active-low input pins are the low voltage level, the device may start the operation at lower than the minimum operating voltage, thus tdelay may exceed the guaranteed time.

PACKAGE INFORMATION

POWER DISSIPATION (DFN(PLP)2020-8B)

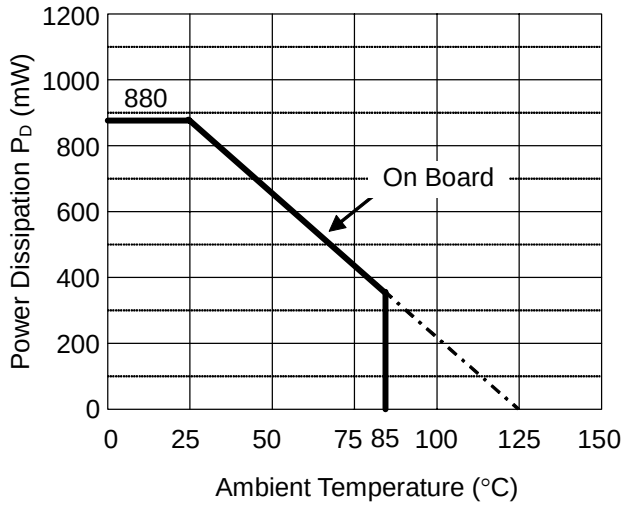
Power Dissipation (P_D) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

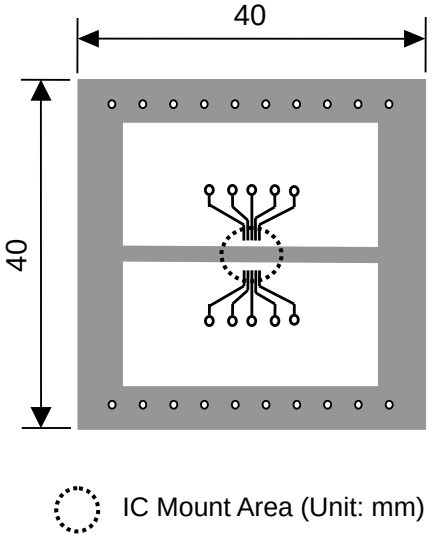
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.54 mm x 30 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern
Power Dissipation	880 mW
Thermal Resistance	θja = (125 − 25°C) / 0.88 W = 114°C/W
	θjc = 22.8°C/W

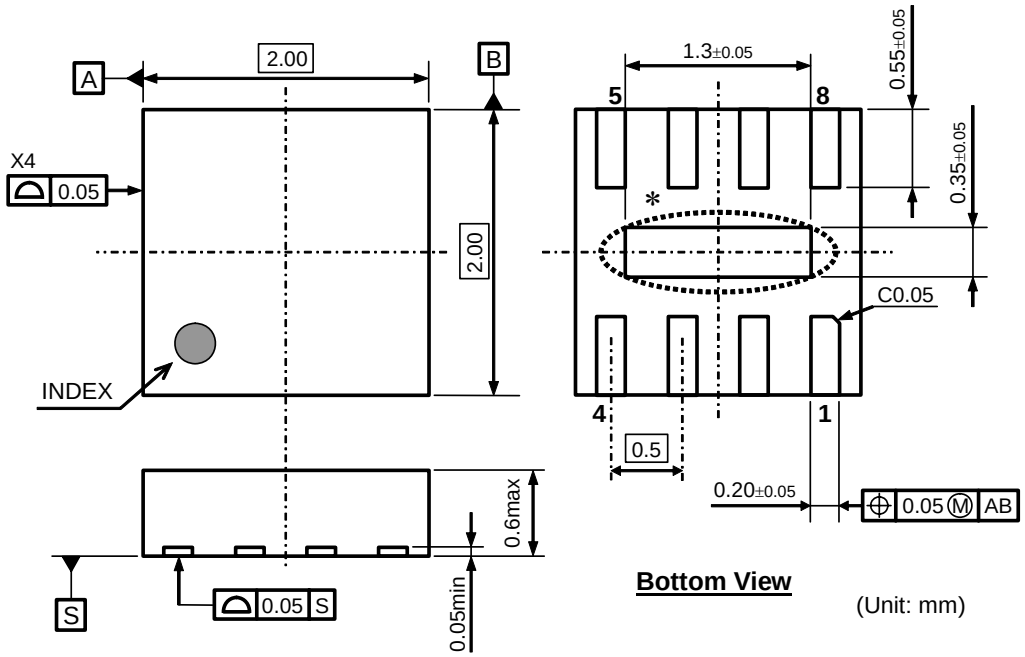


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

PACKAGE DIMENSIONS (DFN(PLP)2020-8B)



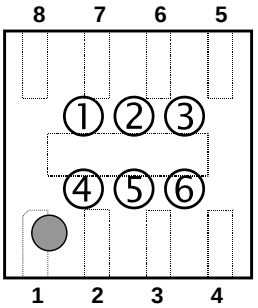
* The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level).
It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

DFN(PLP)2020-8B Package Dimensions

MARK SPECIFICATION (DFN(PLP)2020-8B)

①②③④: Product Code … **Refer to *MARK SPECIFICATION TABLE (DFN(PLP)2020-8B).***

⑤⑥: Lot Number … Alphanumeric Serial Number



DFN(PLP)2020-8B Mark Specification

MARK SPECIFICATION TABLE (DFN(PLP)2020-8B)

R3200K Mark Specification Table

Product Name	①②③④
R3200K001A	D 0 0 1
R3200K001B	D D 0 2
R3200K002A	D D 0 3
R3200K002B	D D 0 4

POWER DISSIPATION (DFN1216-8)

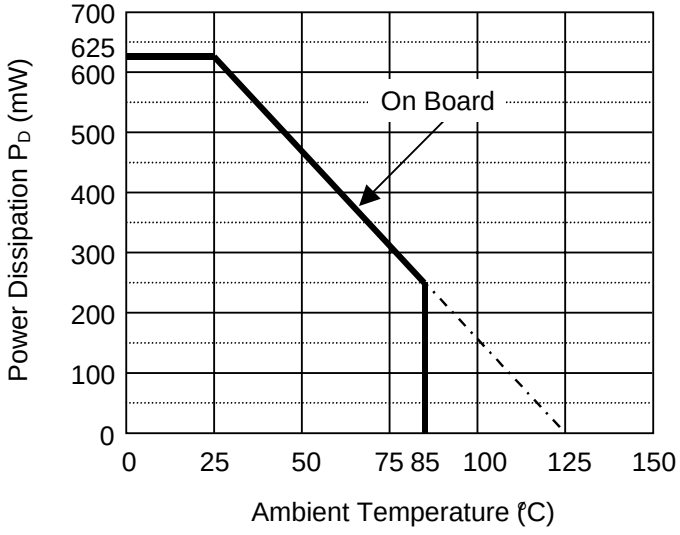
Power Dissipation (P_D) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

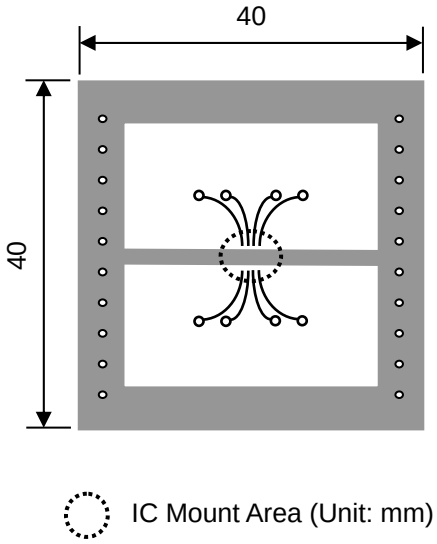
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.5 mm x 28 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern
Power Dissipation	625 mW
Thermal Resistance	θja = (125 − 25°C) / 0.625 W = 160°C/W
	θjc = 26°C/W

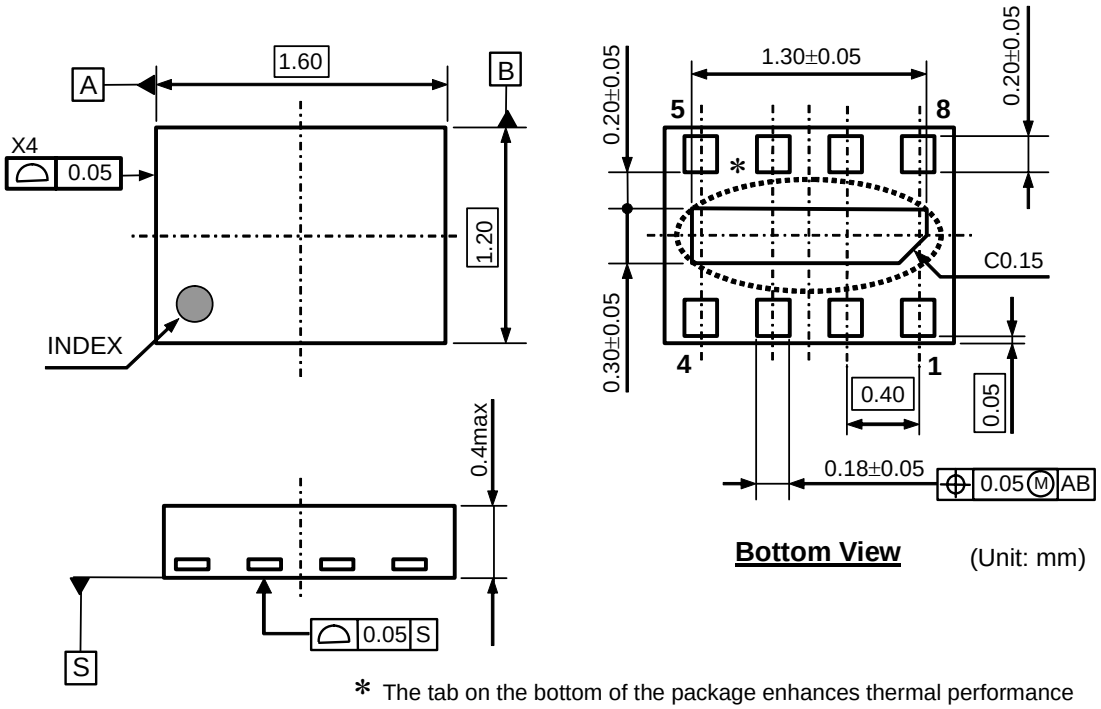


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

PACKAGE DIMENSIONS (DFN1216-8)



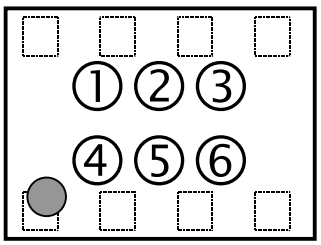
* The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level).
It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

DFN1216-8 Package Dimensions

MARK SPECIFICATION (DFN1216-8)

①②③④: Product Code … **Refer to *MARK SPECIFICATION TABLE (DFN1216-8).***

⑤⑥: Lot Number … Alphanumeric Serial Number



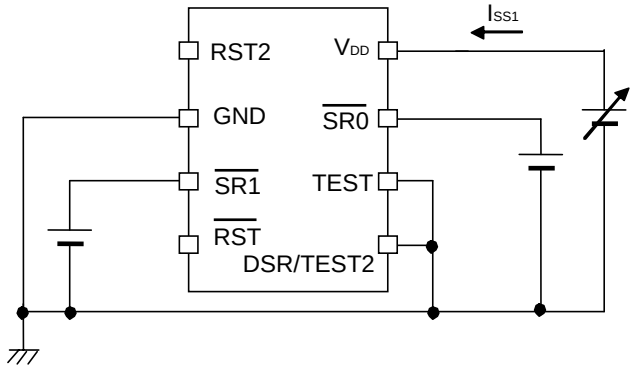
DFN1216-8 Mark Specification

MARK SPECIFICATION TABLE (DFN1216-8)

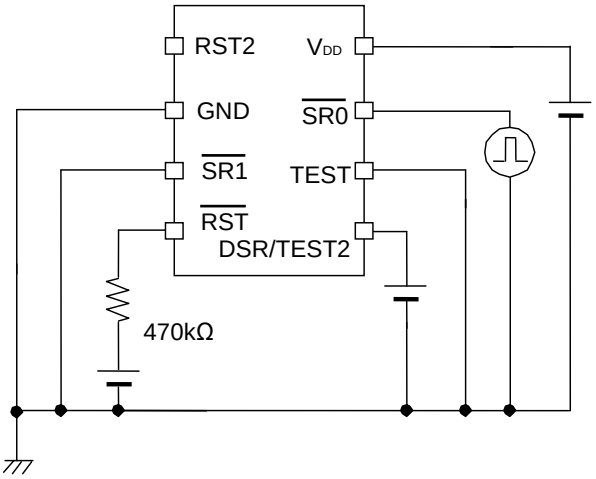
R3200L Mark Specification Table

Product Name	①②③④
R3200L001A	D E 0 1
R3200L001B	D F 0 2
R3200L002A	D E 0 3
R3200L002B	D E 0 4
R3200L052B	D E 0 5
R3200L053B	D E 0 6
R3200L064A	D E 0 7

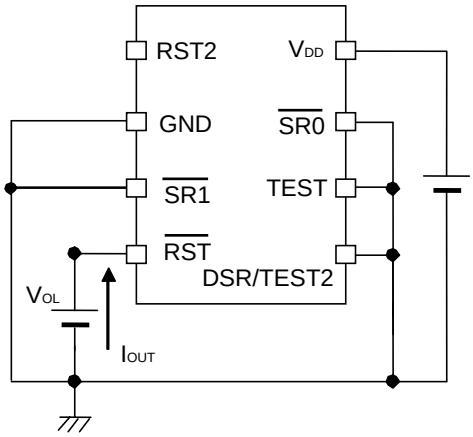
TEST CIRCUITS



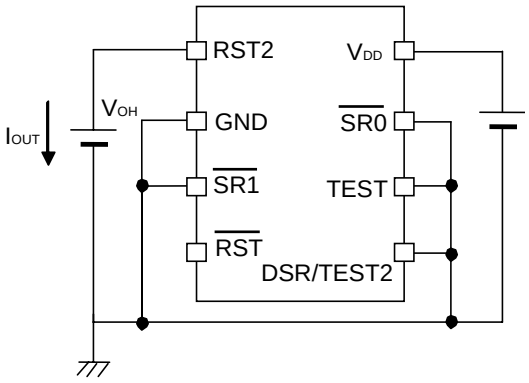
Supply Current Test Circuit



Output Delay Time Test Circuit



Nch Driver Output Voltage Test Circuit

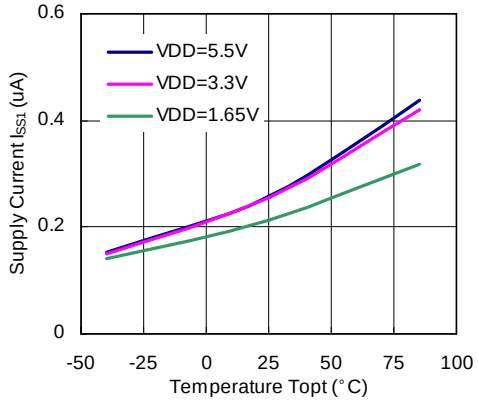


CMOS Driver Output Voltage Test Circuit
(For the R3200xxxxB only.)

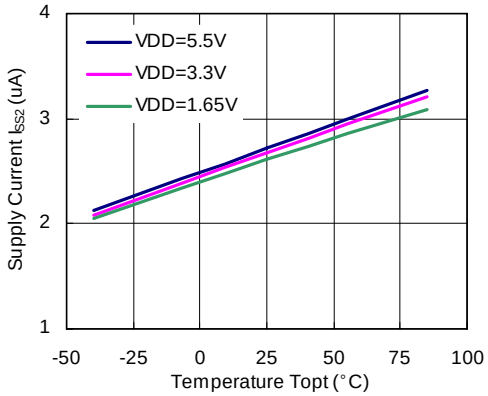
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

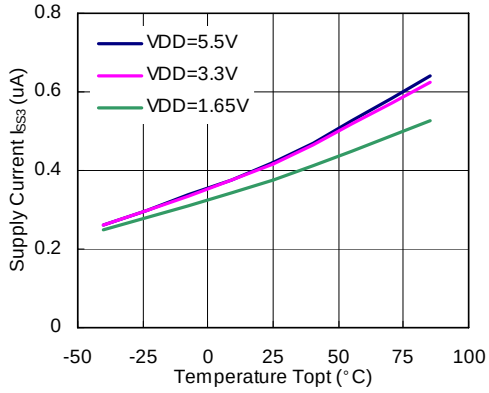
1) Supply Current 1 vs. Temperature
R3200x (at standby)



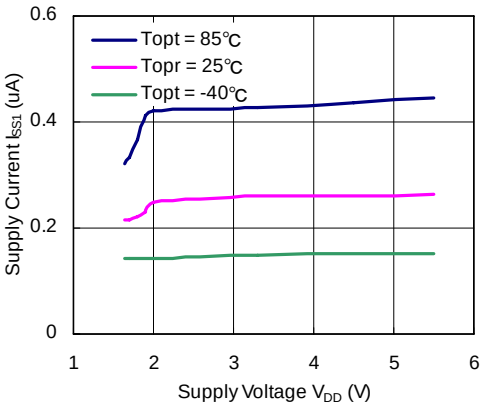
2) Supply Current 2 vs. Temperature
R3200x (before the reset signal output)



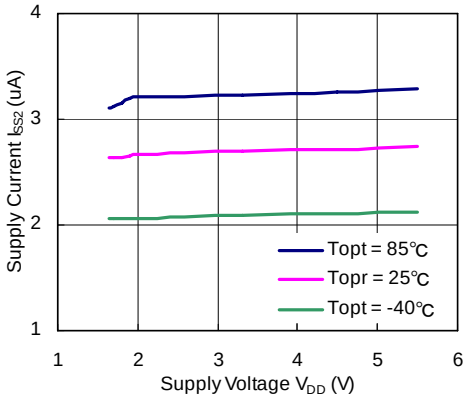
3) Supply Current 3 vs. Temperature
R3200x (after the reset signal output)



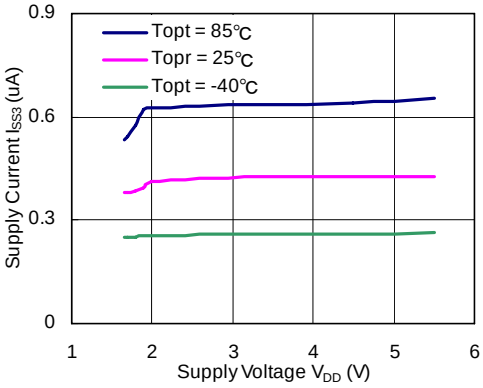
4) Supply Current 1 vs. Supply Voltage
R3200x (at standby)



5) Supply Current 2 vs. Supply Voltage
R3200x (before the reset signal output)

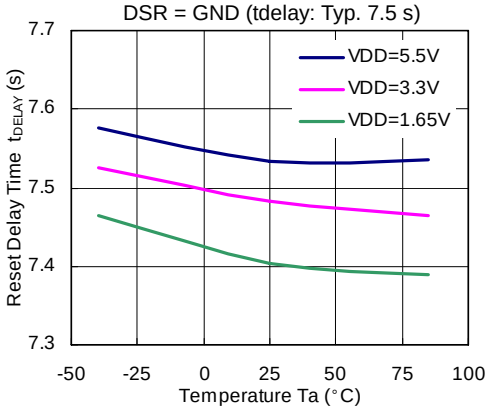


6) Supply Current 2 vs. Supply Voltage
R3200x (after the reset signal output)

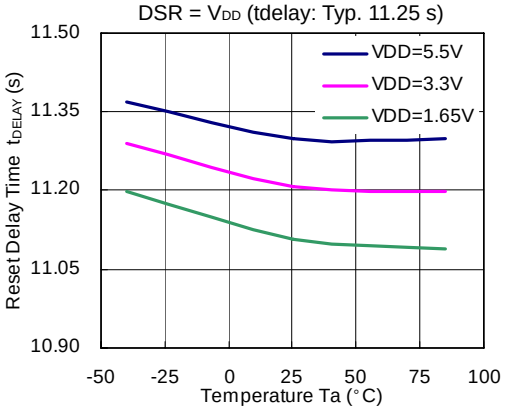


7) Output Delay Time vs. Temperature

R3200x001x

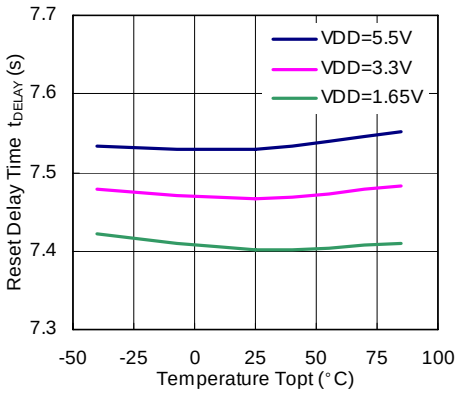


R3200x001x

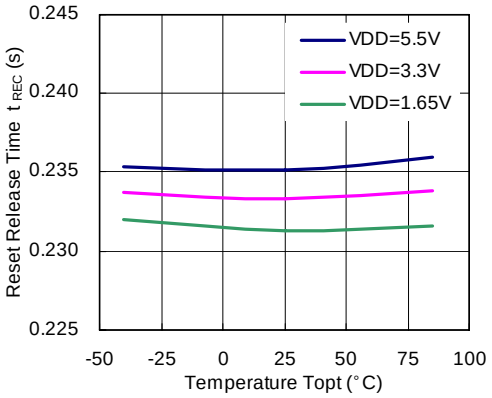


8) Output Release Time vs. Temperature

R3200x002x

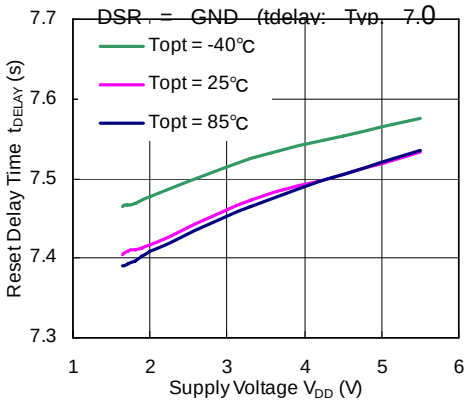


R3200x002x

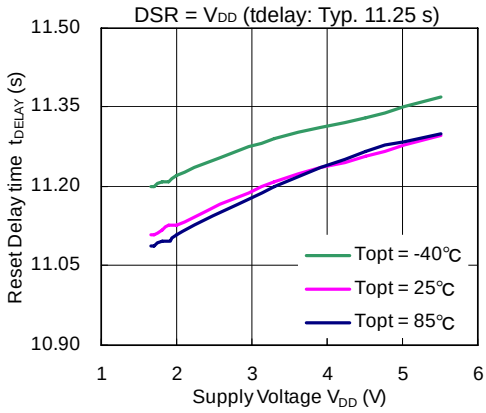


9) Output Delay Time vs. Supply Voltage

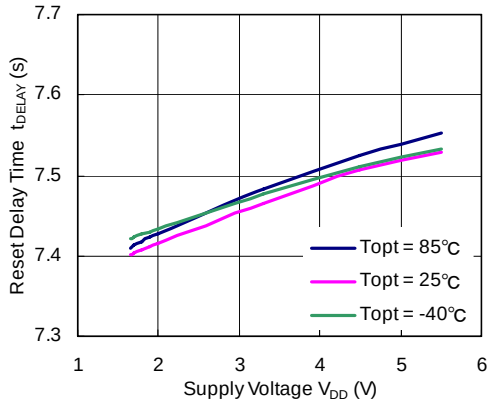
R3200x001x



R3200x001x

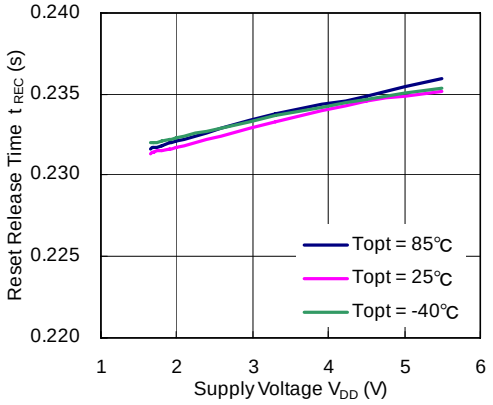


R3200x002x



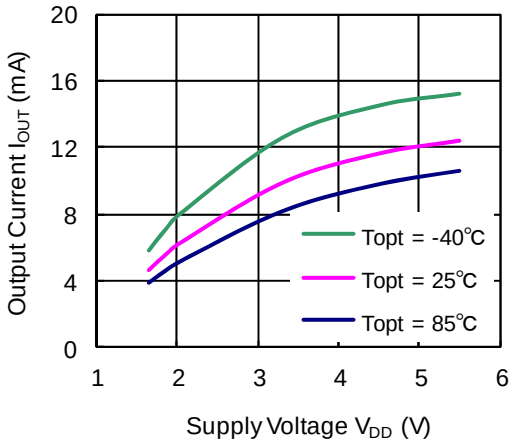
10) Output Release Time vs. Supply Voltage

R3200x002x

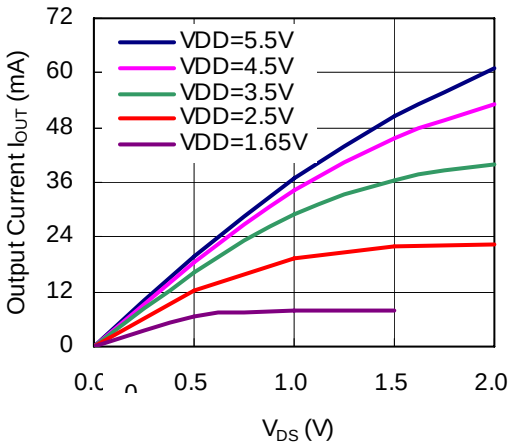


11) Nch Driver Output Current vs. Supply Voltage

V_{DS} = 0.3 V

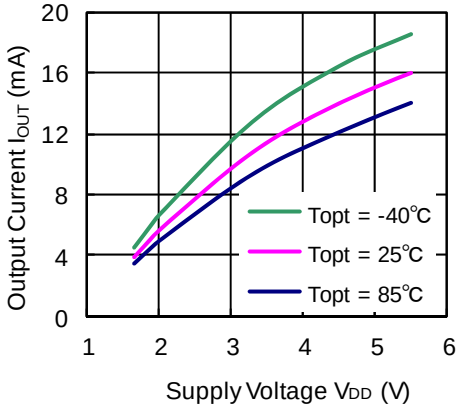


12) Nch Driver Output Current vs. V_{DS}

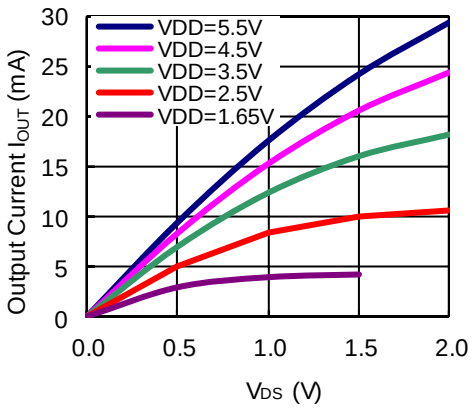


13) Pch Driver Output Current vs. Supply Voltage

V_{DS} = 0.9 V



14) Pch Driver Output Current vs. V_{DS}



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