Dual 1A 1.5MHz Synchronous Step-Down Converters

General Description

The RT8056 is a high efficiency synchronous dual step-down converter. Capable of delivering two independent 1A output current over a wide input voltage range from 2.8V to 5.5V. The RT8056 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as cellular phones, PDAs and hand-held devices. The RT8056 provides two operation modes including PWM/Low-Dropout auto switch and shutdown modes. The internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical applications. The RT8056 enters Low-Dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8056 enters shut-down mode and consumes less than 0.1μA when EN pin is pulled low. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operating frequency of 1.5MHz.

Ordering Information

RT8056□□

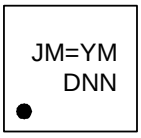
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



JM= : Product Code

YMDNN : Date Code

Features

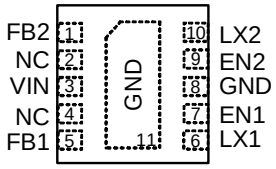
- **2.8V to 5.5V Input Voltage Range**
- **1.5MHz Fixed Frequency PWM Operation**
- **2 x 1A Output Current**
- **Up to 95% Efficiency**
- **No Schottky Diode Required**
- **0.6V Reference Allows for Low Output Voltage**
- **Low Dropout Operation : 100% Duty Cycle**
- **Small 10-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Portable Instruments
- Microprocessors and DSP Core Supplies
- Cellular Phones
- Wireless and DSL Modems
- PC Cards
- Set Top Box

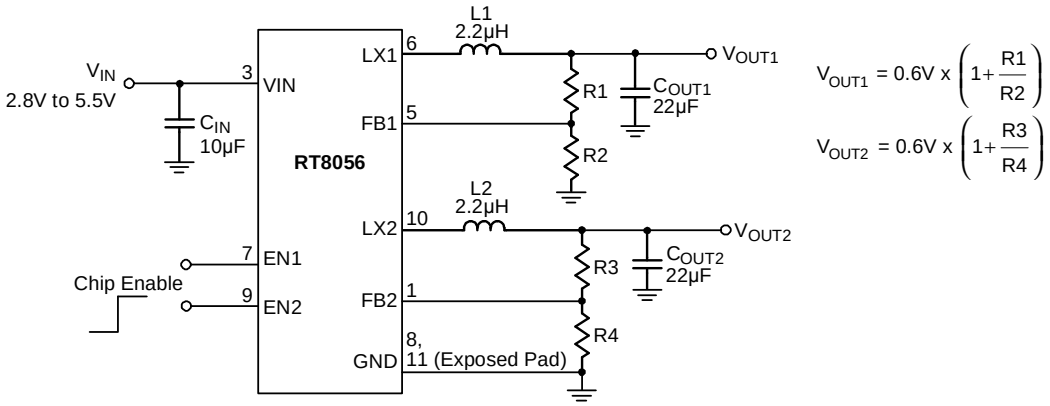
Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

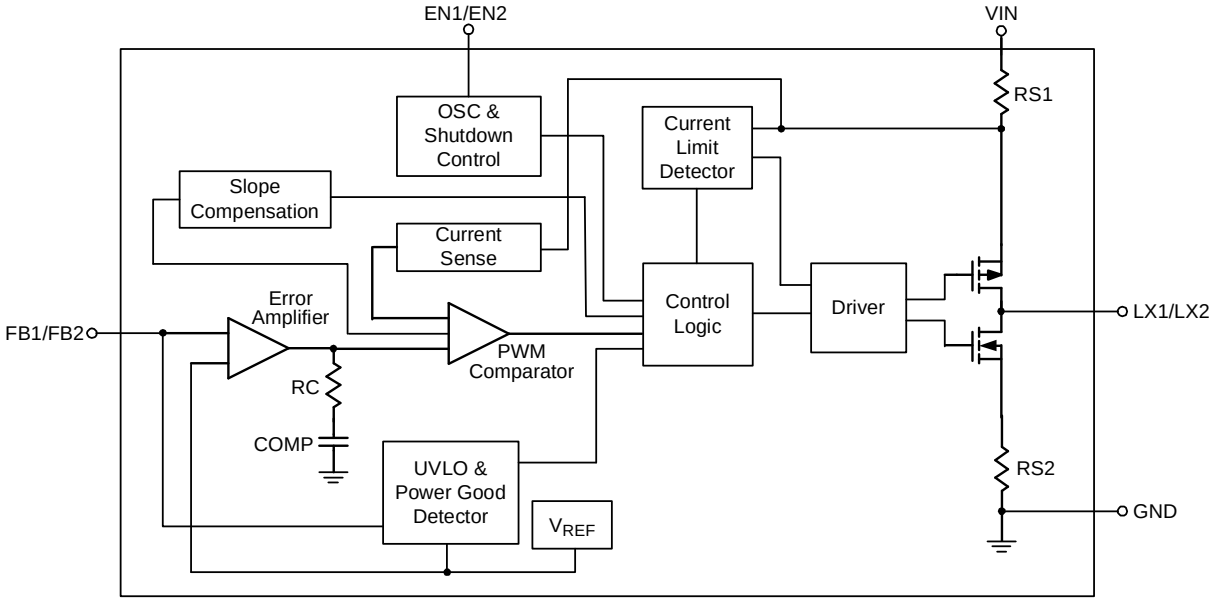
Typical Application Circuit



Function Pin Description

Pin No.	Pin Name	Pin Function
1	FB2	Feedback Input of Channel 2.
2, 4	NC	No Internal Connection.
3	VIN	Power Supply Input of Channel 1 & Channel 2.
5	FB1	Feedback Input of Channel 1.
6	LX1	Switching Node of Channel 1.
7	EN1	Chip Enable of Channel 1 (Active High).
8, 11 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
9	EN2	Chip Enable of Channel 2 (Active High).
10	LX2	Switching Node of Channel 2.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 6.5V
- LX1, LX2 Pin Voltages ---------- –0.3V to (V_{IN}+0.3V)
- Other I/O Pin Voltages ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM ---------- 2kV
  MM ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{IN} ---------- 2.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current		I_Q		--	300	--	μA
Feedback Reference Voltage		V_{REF}		0.588	0.6	0.612	V
Under Voltage Lockout Threshold		V_{UVLOH}	V_{IN} Rising	--	2.1	--	V
			Hysteresis	--	0.18	--	V
Shutdown Current		I_{SHDN}		--	0.1	1	μA
Switching Frequency				1.2	1.5	1.8	MHz
ENx Threshold Voltage	Logic High	V_{IH}		1.5	--	V_{IN}	V
	Logic Low	V_{IL}		--	--	0.4	V
Peak Current Limit		I_{LIM}	V_{IN} = 2.8V to 5.5V	1.1	1.5	--	A
Output Voltage Line Regulation			V_{IN} = 2.8V to 5.5V	--	0.04	0.4	%V
Output Voltage Load Regulation			0mA < I_{LOAD} < 1A (Note5)	--	1	--	%
Switch On-Resistance, High		$R_{DS(ON)\_H}$	I_{SW} = 0.2A	--	280	--	mΩ
Switch On Resistance, Low		$R_{DS(ON)\_L}$	I_{SW} = 0.2A	--	290	--	mΩ
Thermal Shutdown Temperature		T_{SD}		--	138	--	°C
Thermal Shutdown Hysteresis				--	18	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

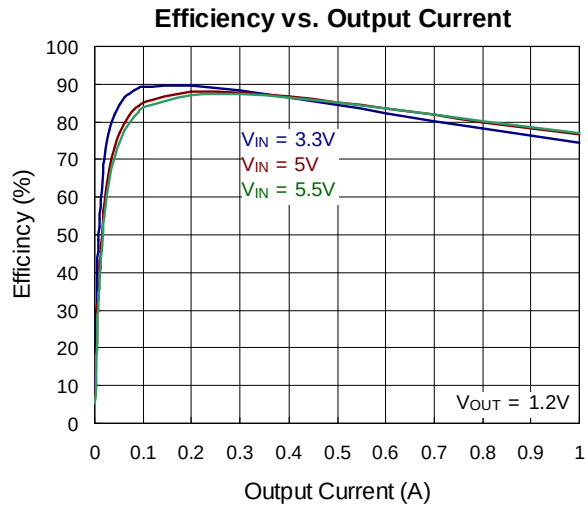
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

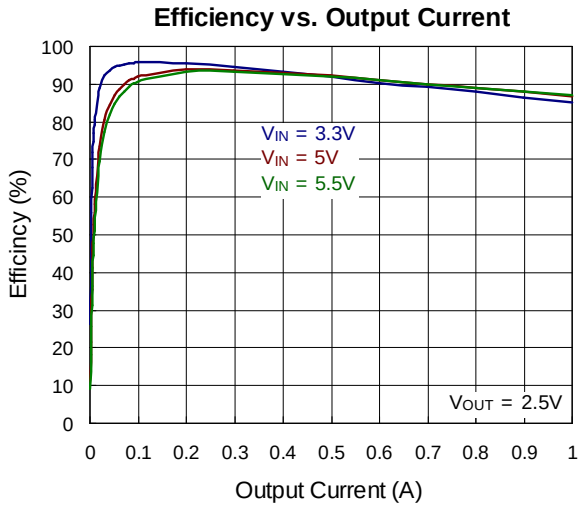
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

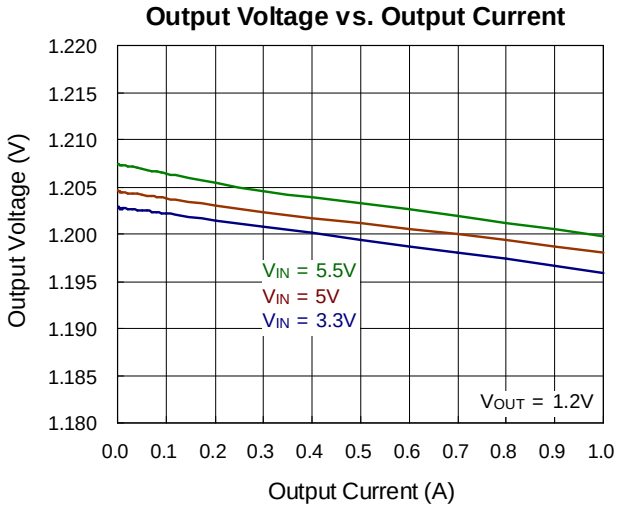
Note 4. The device is not guaranteed to function outside its operating conditions.

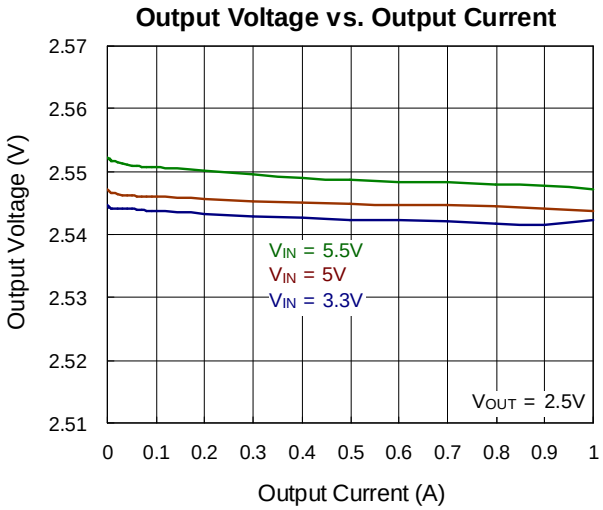
Note 5. Guaranteed by Design.

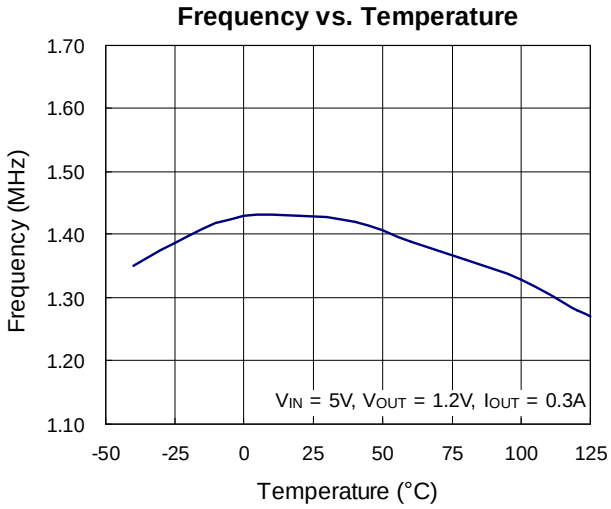
Typical Operating Characteristics

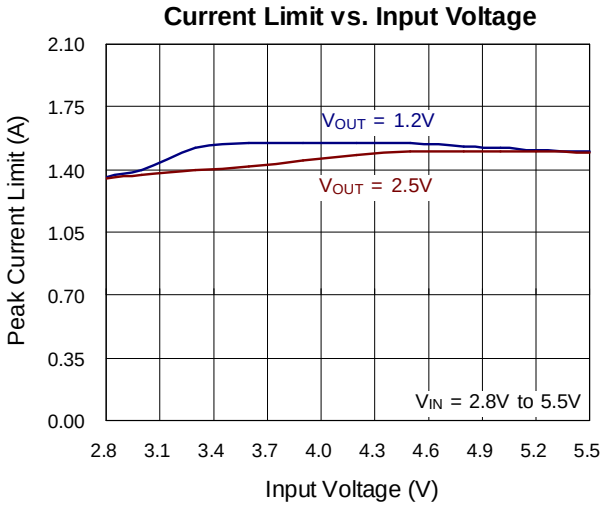




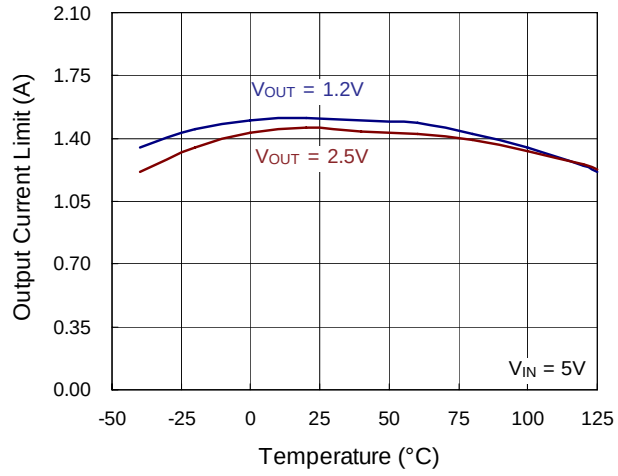




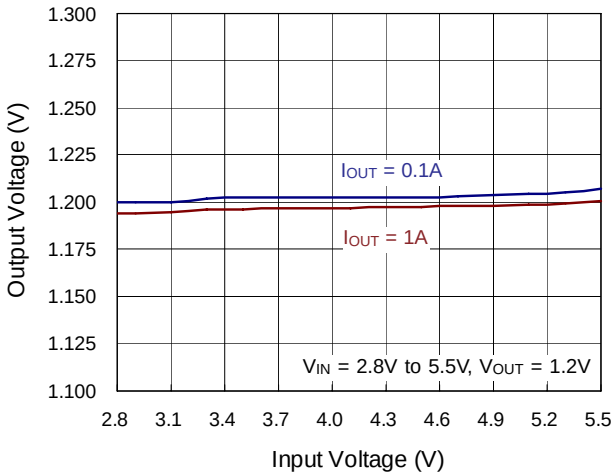




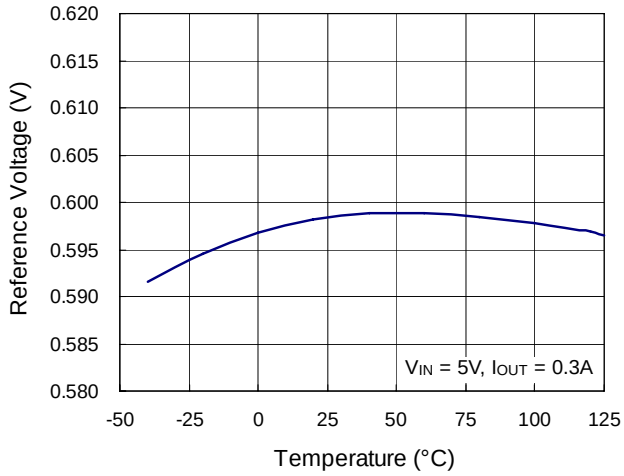
Current Limit vs. Temperature



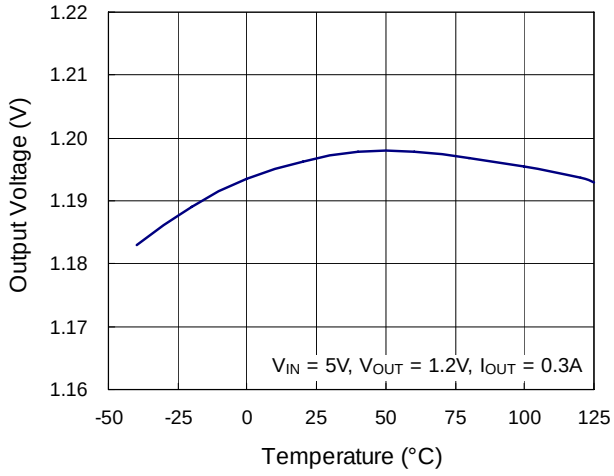
Output Voltage vs. Input Voltage



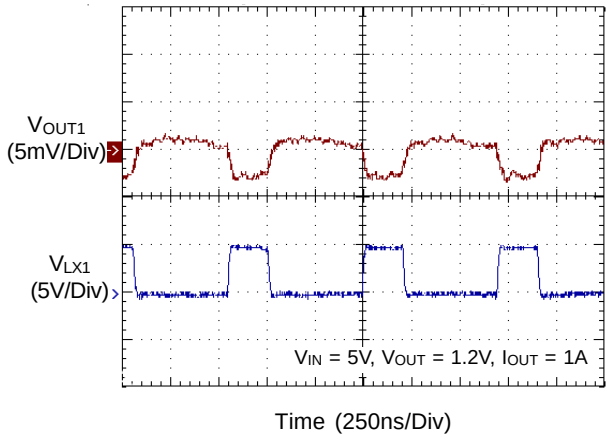
Reference Voltage vs. Temperature



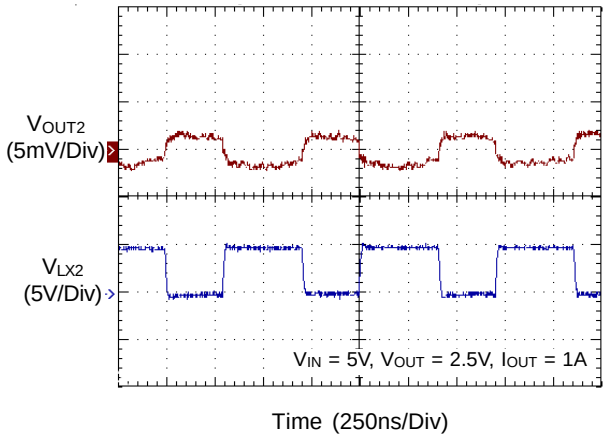
Output Voltage vs. Temperature



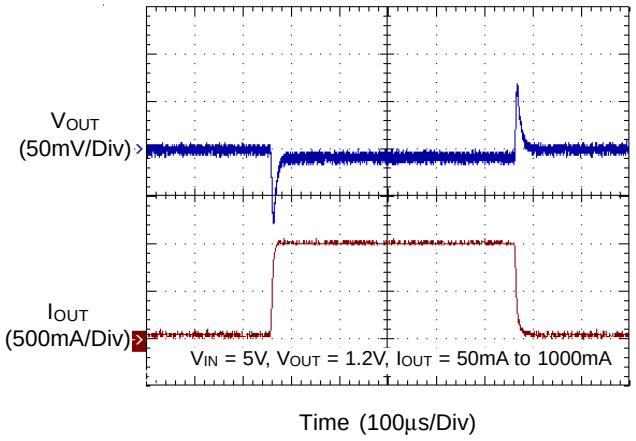
Output Ripple



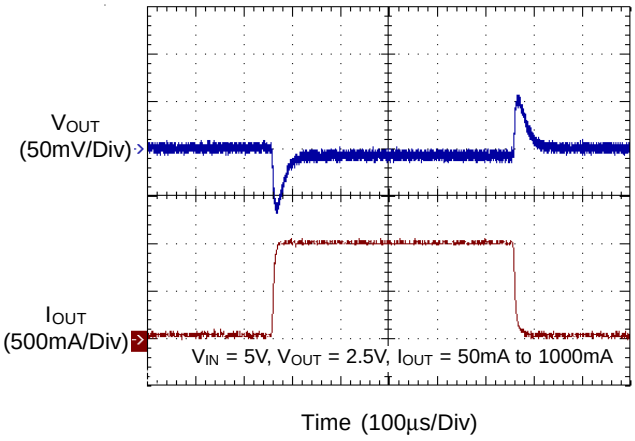
Output Ripple



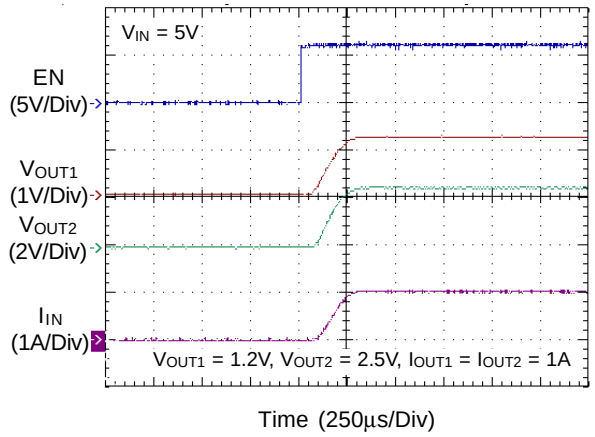
Load Transient Response



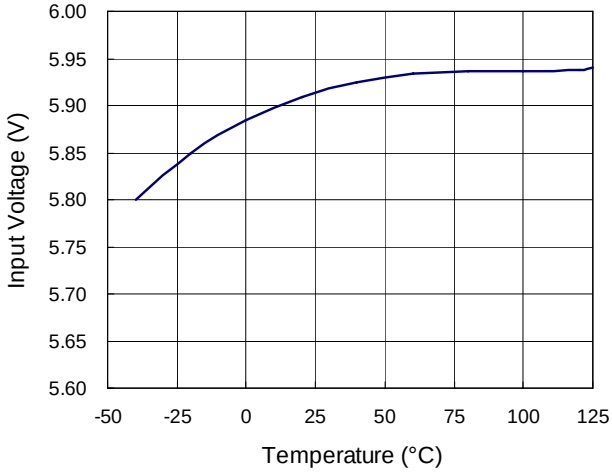
Load Transient Response



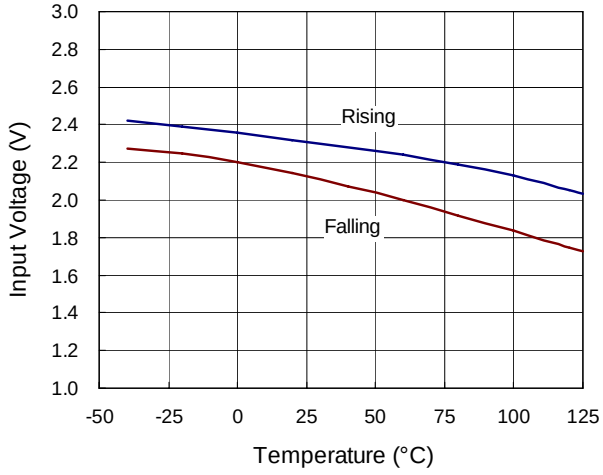
Power On from EN



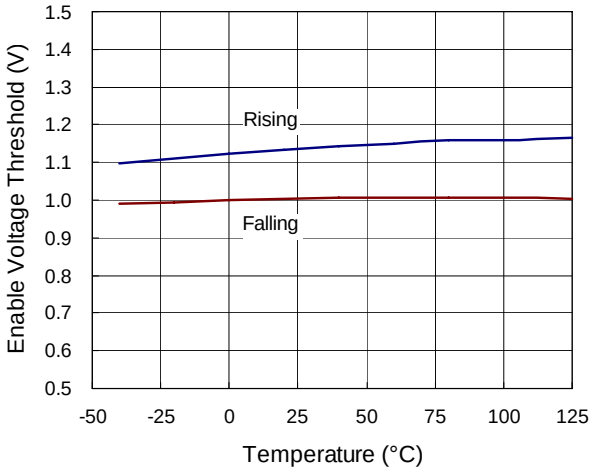
VIN OVP Threshold vs. Temperature



VIN UVLO Threshold vs. Temperature



EN Threshold vs. Temperature



Applications Information

The basic RT8056 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency, followed by C_{IN} and C_{OUT}.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low-cost powdered iron cores, thus forcing the use of more expensive ferrite or permalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. However, increased inductance requires more turns of wire and therefore, results in higher copper losses.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and saturation prevention. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded.

This results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which kind of inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often only based on 2000 hours of life-time which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special

polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR, but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications, provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

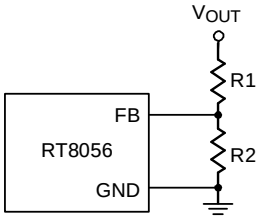


Figure 1. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation :

$V_{OUT} = V_{REF} \times (1+ R1/R2)$

where V_{REF} is the internal reference voltage (0.6V typical)

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of RT8056, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For RT8056 package, the derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

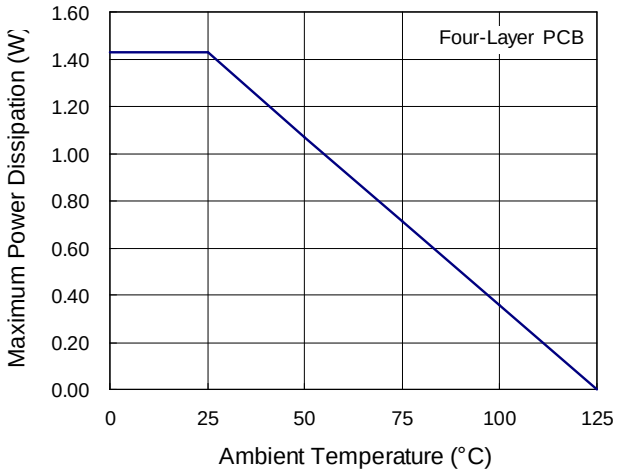


Figure 2. Derating Curve for RT8056 Package

Layout Consideration

Follow the PCB layout guidelines for optimal performance of RT8056.

- For the main current path, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8056.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

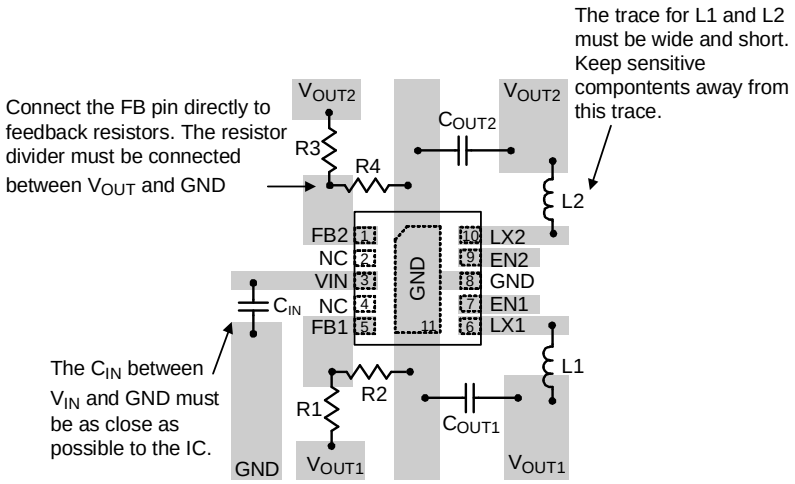
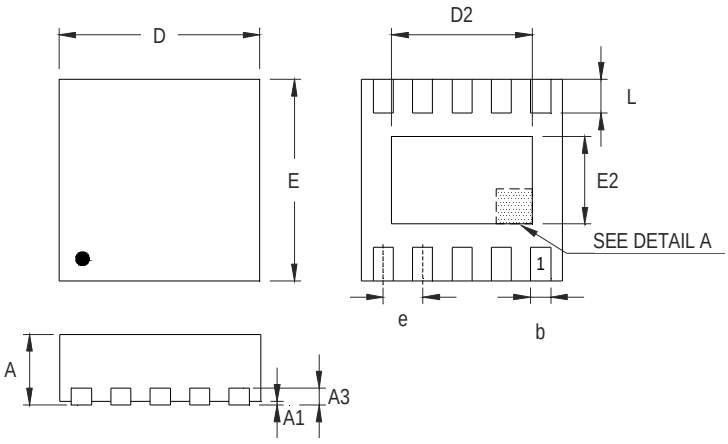
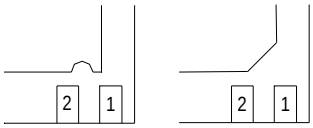


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com