

APPLICATION MANUAL

RV-3029-C2

DTCXO Temperature Compensated

Real Time Clock / Calendar Module

with I2C Interface

| | | |
|-------|------------|-------------------|
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RV-3029-C2

Highly accurate, DTCXO Temperature Compensated Real Time Clock / Calendar Module with I²C Interface.

1.0 OVERVIEW

- RTC module with built-in “Tuning Fork” crystal oscillating at 32.768 kHz
- Factory calibrated, all built-in Temperature Compensation circuitry.

| Time accuracy: | Temperature Range | Opt: A | Opt: B |
|----------------|-------------------|-----------|------------|
| | 25°C | +/- 3 ppm | +/- 3 ppm |
| | 0°C to + 50°C | +/- 4 ppm | +/- 5 ppm |
| | -10°C to + 60°C | +/- 5 ppm | +/- 10 ppm |
| | -40°C to + 85°C | +/- 6 ppm | +/- 25 ppm |
| | -40°C to +125°C | +/- 8 ppm | +/- 30 ppm |

- Ultra low power consumption: 850nA typ @ V_{DD} = 3.0V / T_{amb} = 25°C
- Wide clock operating voltage: 1.3 – 5.5V
- Wide Interface operating voltage: 1.4 – 5.5V
- Extended Operating Temperature Range: -40°C to +125°C
- I²C Serial Interface with fast mode SCL clock frequency of 400 kHz.
- Provides year, month, day, weekday, hours, minutes and seconds.
- Highly versatile Alarm and Timer functions
- Integrated Low-Voltage Detector, Power-On Reset and Self-Recovery System.
- Main Power Supply to Backup Battery switchover circuitry with Trickle Charger.
- Programmable CLKOUT pins for peripheral devices (32.768 kHz / 1024 Hz / 32 Hz / 1 Hz)
- Small and compact package-size of 5.0 x 3.2 x 1.2mm, RoHS-compliant and 100% lead-free.

1.1 GENERAL DESCRIPTION

The RV-3029-C2 is a CMOS low power, real-time clock/calendar module with built-in Thermometer and Digital Temperature Compensation circuitry (DTCXO). The temperature compensation circuitry is factory-calibrated and greatly improves the time accuracy by compensating the frequency-deviation @ 25°C and the anticipated frequency-drift over the temperature of the embedded 32.768 kHz “Tuning-Fork” crystal, even over the extended Temperature Range -40°C to +125°C. Data is transferred serially via an I²C-Interface with a maximum SCL clock frequency in fast mode of 400 kHz, the built-in word address register is incremented automatically after each written or read data byte. Beyond standard RTC-functions like year, month, day, weekday, hours, minutes, seconds information, the RV-3029-C2 offers highly versatile Alarm and Timer-Interrupt function, programmable Clock-Output and Low-Voltage Detector.

1.2 APPLICATIONS

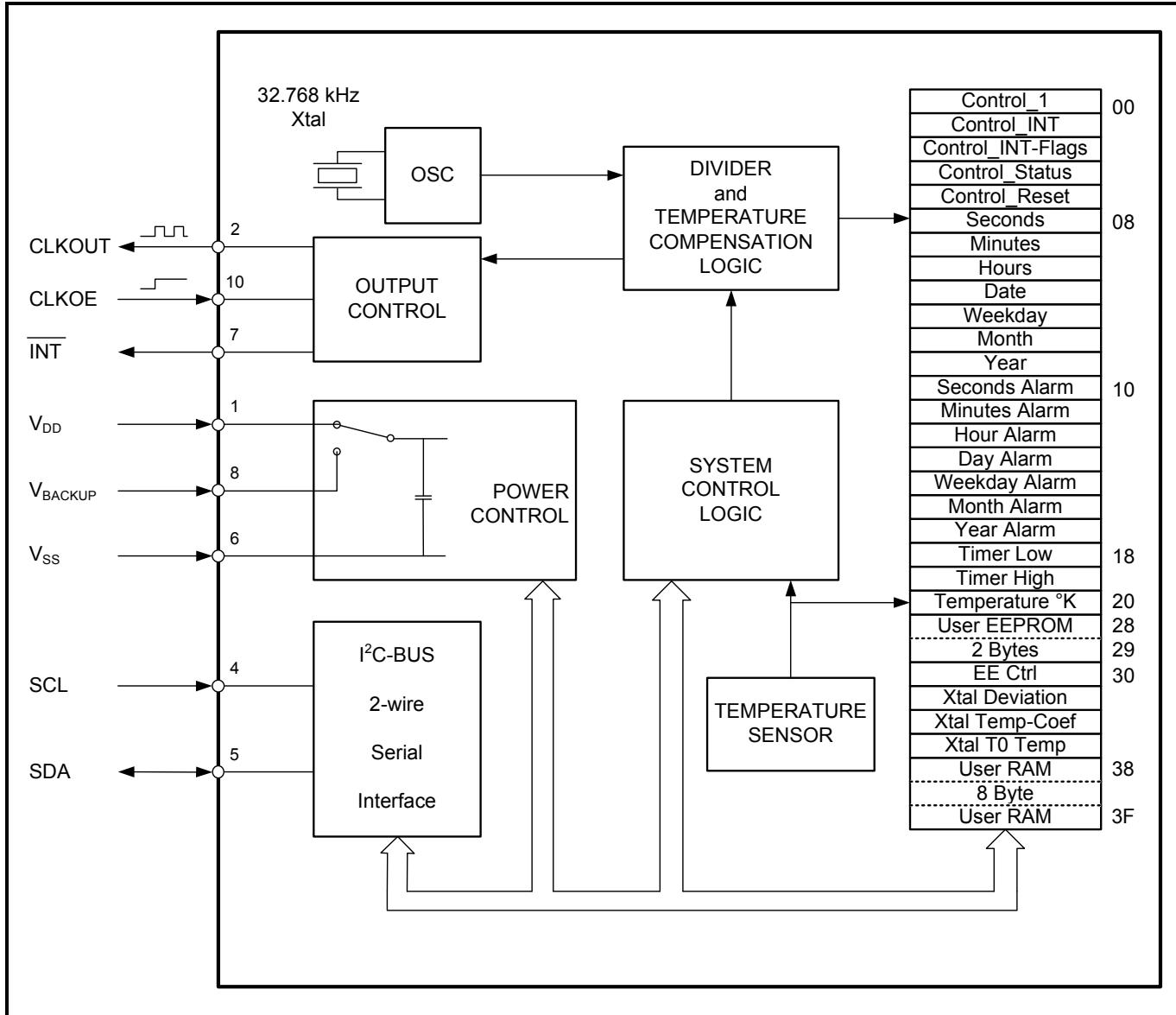
The RV-3029-C2 RTC module combines key functions with outstanding performance in a small ceramic package:

- Factory calibrated Temperature Compensation
- Extended Temperature Range up to +125°C
- Low Power consumption.
- Smallest temperature compensated RTC module with embedded Xtal.

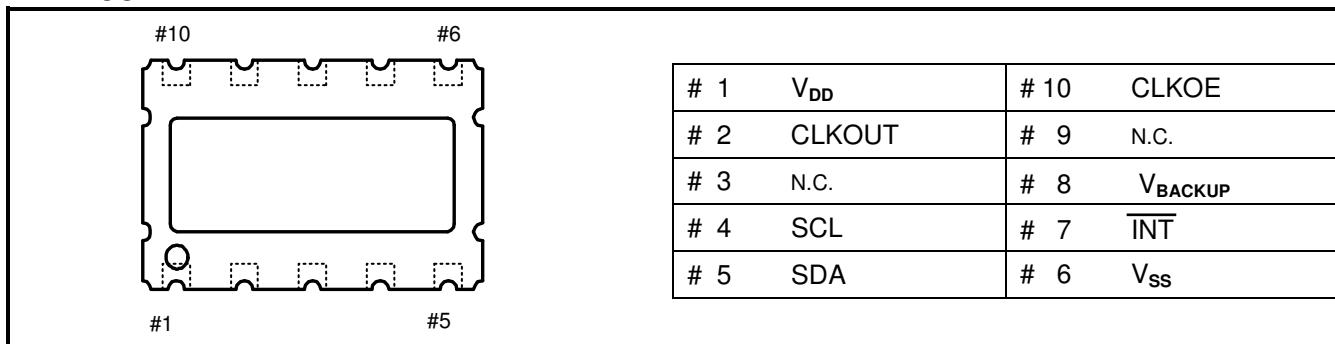
These unique features make this product perfectly suitable for many applications:

- Automotive : Car Radio / GPS and Tracking Systems / Dashboard / Engine Controller / Car Mobile & Entertainment Systems / Tachometers
- Metering : E-meter / Heating Counter
- Outdoor : ATM & POS systems / Surveillance & Safety systems / Ticketing systems
- All kind of portable and battery operated devices.
- Industrial and consumer electronics
- White goods

2.0 BLOCK DIAGRAM



2.1 PINOUT



2.2 PIN DESCRIPTION

| Symbol | Pin # | Description |
|--------------|-------|---|
| V_{DD} | 1 | Positive supply voltage; positive or negative steps in supply voltage may affect oscillator performance, recommend 10 nF decoupling capacitor close to device |
| CLKOUT | 2 | Clock Output pin. CLKOUT or INT function can be selected.(Control_1; bit7; CLK/INT) CLKOUT output push-pull / INT function open-drain requiring pull-up resistor |
| NC | 3 | Not Connected |
| SCL | 4 | Serial Clock Input pin; requires pull-up resistor |
| SDA | 5 | Serial Data Input-Output pin; open-drain; requires pull-up resistor |
| V_{SS} | 6 | Ground |
| INT | 7 | Interrupt Output pin; open-drain; active LOW |
| V_{BACKUP} | 8 | Backup Supply Voltage; tie to GND when not using backup supply voltage. |
| NC | 9 | Not Connected |
| CLKOE | 10 | CLKOUT enable/disable pin; enable is active HIGH |

2.3 FUNCTIONAL DESCRIPTION

The RV-3029-C2 is a highly accurate real-time clock/calendar module due to integrated temperature compensation circuitry. The built-in Thermometer and Digital Temperature Compensation circuitry (DTCXO) provides improved time-accuracy; achieved by measuring the temperature and calculating an expected correction value based on precise, factory-calibrated Crystal parameters. The compensation of the frequency deviation @ 25 °C and the Crystal's frequency-drift over the temperature range are obtained by adding or subtracting 32.768 kHz oscillator clock-pulses. Beyond standard RTC-functions like year, month, day, weekday, hours, minutes, seconds information, the RV-3029-C2 offers highly versatile Alarm and Timer-Interrupt function, programmable Clock-Output and Voltage-Low-Detector and a Main-Supply to Backup-Battery Switchover Circuitry and a 400 kHz I²C-Interface.

The CMOS IC contains thirty 8-bit RAM registers organized in 6 memory pages; the address counter is automatically incremented within the same memory page.

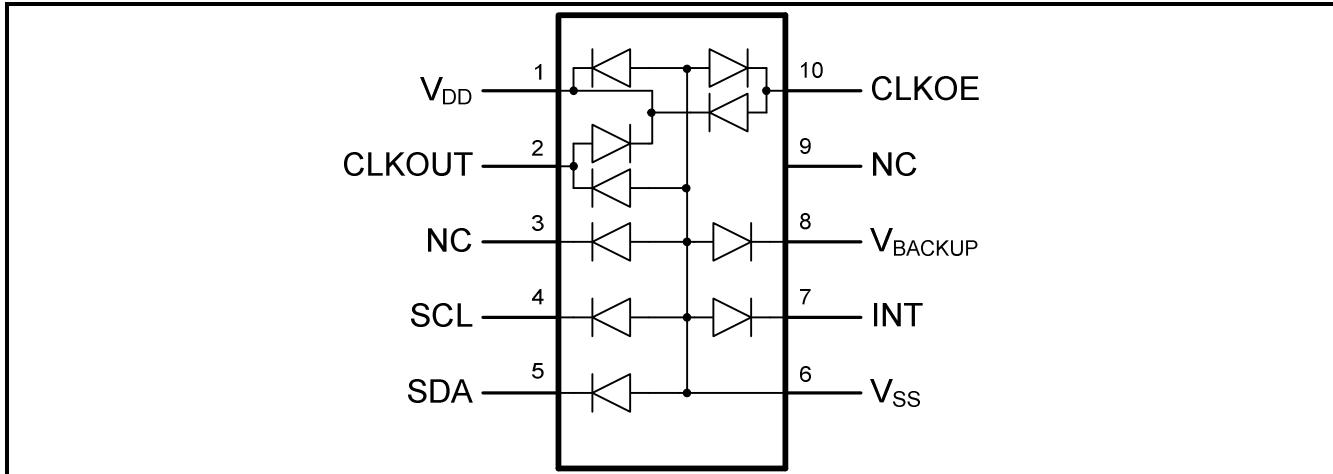
All sixteen registers are designed as addressable 8-bit parallel registers, although, not all bits are implemented.

- **Memory page #00** contains of five registers (memory address 00h and 04h) used as control registers.
- **Memory page #01** addresses 08h through 0Eh are used as counters for the clock function (seconds up to years). The Seconds, Minutes, Hours, Days, Weekdays, Months and Years registers are all coded in Binary-Coded-Decimal (BCD) format. When one of the RTC registers is read, the content of all counters is frozen to prevent faulty reading of the clock/calendar registers during a carry condition.
- **Memory page #02** addresses 10h through 16h define the alarm condition
- **Memory page #03** addresses 18h and 19h are used for Timer function
- **Memory page #04** address 20h provides the thermometer reading value.
- **Memory page #07** addresses 38h through 3Fh are available for user data

Additionally, the CMOS-IC contains six non-volatile 8-bit EEPROM registers organized in 2 memory pages; the address counter is automatically incremented within the same memory page.

- **EEPROM page #05** addresses 28h and 29h are available for EEPROM user data.
- **EEPROM page #06** contains of four registers (memory address 30h through 33h) used as non-volatile control registers. These registers contain the factory programmed parameters of the Crystal's thermal characteristics, the frequency-deviation @ ambient temperature and the Thermometer's calibration values. In favour for the best time-accuracy, the factory programmed registers (memory address 31h through 33h) shall not be changed by the user without carefully studying its function.

2.4 DEVICE PROTECTION DIAGRAM



3.0 REGISTER ORGANIZATION

The registers are grouped into memory pages.

The pages are addressed by the 5 most-significant-bits (MSB's bits 7 – 3), the 3 least-significant-bits (LSB's 2 – 0) select the registers within the addressed page.

30 RAM registers organized in 6 memory pages and 6 EEPROM registers organized in 2 memory pages are available. During Interface access, the page address (MSB's 7 - 3) is fixed while the register address (LSB's 2 - 0) are automatically incremented. The content of all counters and registers are frozen to prevent faulty reading of the clock/calendar registers during carry condition.

The time registers in the Clock and Alarm pages are encoded in the Binary Coded Decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary format.

3.1 REGISTER OVERVIEW

| Address | | | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | | |
|---------------------|-----------|-----|----------------|---------------------------------|--------|-----------|---------|-------|-------|-------|-------|-----|----|----|
| Page | Address | Hex | | | | | | | | | | | | |
| Bit 7 - 3 | Bit 2 - 0 | | Control page | 000 | 00h | Control_1 | Clk/Int | TD1 | TD0 | SROn | EERE | TAR | TE | WE |
| 00000 | 001 | 01h | | Control_INT | X | X | X | SRIE | V2IE | V1IE | TIE | AIE | | |
| | 010 | 02h | | Control_INT Flag | X | X | X | SRF | V2IF | V1IF | TF | AF | | |
| | 011 | 03h | | Control_Status | EEbusy | X | PON | SR | V2F | V1F | X | X | | |
| | 100 | 04h | | Control_Reset | X | X | X | SysR | X | X | X | X | | |
| | 101 | 05h | | Control_Disable | X | X | X | SROff | X | X | X | X | | |
| Clock page | 000 | 08h | Seconds | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| | 001 | 09h | Minutes | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| | 010 | 0Ah | Hours | X | 12-24 | 20-PM | 10 | 8 | 4 | 2 | 1 | | | |
| | 011 | 0Bh | Days | X | X | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| | 100 | 0Ch | Weekdays | X | X | X | X | X | 4 | 2 | 1 | | | |
| | 101 | 0Dh | Months | X | X | X | 10 | 8 | 4 | 2 | 1 | | | |
| | 110 | 0Eh | Years | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| Alarm page | 000 | 10h | Second Alarm | AE_S | 40 | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| | 001 | 11h | Minute Alarm | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| | 010 | 12h | Hour Alarm | AE_H | X | 20-PM | 10 | 8 | 4 | 2 | 1 | | | |
| | 011 | 13h | Days Alarm | AE_D | X | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| | 100 | 14h | Weekday Alarm | AE_W | X | X | X | X | 4 | 2 | 1 | | | |
| | 101 | 15h | Months Alarm | AE_M | X | X | 10 | 8 | 4 | 2 | 1 | | | |
| | 110 | 16h | Year Alarm | AE_Y | 40 | 20 | 10 | 8 | 4 | 2 | 1 | | | |
| Timer page | 000 | 18h | Timer Low | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | | | |
| | 001 | 19h | Timer High | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | | | |
| Temperature page | 000 | 20h | Temperature | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | | | |
| EEPROM User | 000 | 28h | EEPROM User | 2 bytes of EEPROM for user data | | | | | | | | | | |
| | 001 | 29h | EEPROM User | | | | | | | | | | | |
| EEPROM Control page | 000 | 30h | EEPROM Control | R80k | R20k | R5k | R1k | FD1 | FD0 | ThE | ThP | | | |
| | 001 | 31h | Xtal Offset | sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | | | |
| | 010 | 32h | Xtal Coef | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | | | |
| | 011 | 33h | Xtal T0 | X | X | 32 | 16 | 8 | 4 | 2 | 1 | | | |
| RAM page | 000 | 38h | User RAM | 8 bytes of RAM for user data | | | | | | | | | | |
| | : | : | | | | | | | | | | | | |
| | 111 | 3Fh | | | | | | | | | | | | |

Bit positions labelled as "X" are not implemented and will return a "0" when read.

3.2 CONTROL PAGE REGISTER FUNCTION

3.2.1 CONTROL_1 (address 00h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|---------|--|-------|-------|-------|-------|-----------------|-------|
| 00h | Control_1 | Clk/Int | TD1 | TD0 | SROn | EERE | TAR | TE | WE |
| Bit | Symbol | Value | Description | | | | | Reference | |
| 7 | Clk/Int | 0 | CLKOUT pin 2; applies INT function on pin 2 | | | | | see section 4.9 | |
| | | 1 | CLKOUT pin 2; applies CLKOUT function on pin 2 | | | | | | |
| 6 | TD1 | 00 | Select Source Clock for internal Countdown Timer | | | | | see section 4.4 | |
| 5 | TD0 | 01 | | | | | | | |
| 4 | SROn | 10 | Disables Self Recovery function | | | | | see section 4.8 | |
| | | 11 | | | | | | | |
| 3 | EERE | 0 | Disables automatic EEPROM refresh every hour | | | | | see section 4.3 | |
| | | 1 | Enables automatic EEPROM refresh every hour | | | | | | |
| 2 | TAR | 0 | Disables Countdown Timer auto-reload mode | | | | | see section 4.4 | |
| | | 1 | Enables Countdown Timer auto-reload mode | | | | | | |
| 1 | TE | 0 | Disables Countdown Timer | | | | | see section 4.4 | |
| | | 1 | Enables Countdown Timer | | | | | | |
| 0 | WE | 0 | Disables 1Hz Clock Source for Watch | | | | | see section 4.7 | |
| | | 1 | Enables 1Hz Clock Source for Watch | | | | | | |

3.2.2 CONTROL_INT (address 01h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
|---------|-------------|-------|---|-------|-------|-------|-------|-------------------|-------|--|--|
| 01h | Control_INT | X | X | X | SRIE | V2IE | V1IE | TIE | AIE | | |
| Bit | Symbol | Value | Description | | | | | Reference | | | |
| 7 to 5 | unused | X | unused | | | | | see section 4.8 | | | |
| | SRIE | 0 | Disables Self-Recovery INT | | | | | | | | |
| | | 1 | Enables Self-Recovery INT | | | | | | | | |
| 3 | V2IE | 0 | Disables VLOW2 INT; "Low Voltage 2 detection" | | | | | see section 4.1.2 | | | |
| | | 1 | Enables VLOW2 INT; "Low Voltage 2 detection" | | | | | | | | |
| 2 | V1IE | 0 | Disables VLOW1 INT; "Low Voltage 1 detection" | | | | | see section 4.1.2 | | | |
| | | 1 | Enables VLOW1 INT; "Low Voltage 1 detection" | | | | | | | | |
| 1 | TIE | 0 | Disables Countdown Timer INT | | | | | see section 4.4.1 | | | |
| | | 1 | Enables Countdown Timer INT | | | | | | | | |
| 0 | AIE | 0 | Disables Alarm INT | | | | | see section 4.5.1 | | | |
| | | 1 | Enables Alarm INT | | | | | | | | |

Bit positions labelled as "X" are not implemented and will return a "0" when read.

3.2.3 CONTROL_INT_FLAG (address 02h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------------|-------|---|-------|-------|-------|-------|-------|-----------------|
| 02h | Control_INT Flag | X | X | X | SRF | V2IF | V1IF | TF | AF |
| Bit | Symbol | Value | Description | | | | | | Reference |
| 7 to 5 | unused | X | unused | | | | | | |
| | SRF | 0 | No Self-Recovery Interrupt generated | | | | | | see section 4.6 |
| | | 1 | Self-Recovery Interrupt generated if possible deadlock is detected; clear flag to clear interrupt | | | | | | |
| 3 | V2IF | 0 | No VLOW2 Interrupt generated | | | | | | see section 4.6 |
| | | 1 | VLOW2 Interrupt generated when supply voltage drops below VLOW2 threshold | | | | | | |
| 2 | V1IF | 0 | No VLOW1 Interrupt generated | | | | | | see section 4.6 |
| | | 1 | VLOW1 Interrupt generated when supply voltage drops below VLOW1 threshold | | | | | | |
| 1 | TF | 0 | No Timer Interrupt generated | | | | | | see section 4.6 |
| | | 1 | Timer Interrupt generated when Countdown Timer value reaches zero | | | | | | |
| 0 | AF | 0 | No Alarm Interrupt generated | | | | | | see section 4.6 |
| | | 1 | Alarm Interrupt generated when Time & Date matches Alarm setting | | | | | | |

Bit positions labelled as "X" are not implemented and will return a "0" when read.

3.2.4 CONTROL_STATUS (address 03h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|--------|---|-------|-------|-------|-------|-------|-------------------|
| 03h | Control_Status | EEbusy | X | PON | SR | V2F | V1F | X | X |
| Bit | Symbol | Value | Description | | | | | | Reference |
| 7 | EEbusy | 0 | EEPROM is not busy | | | | | | see section 4.3 |
| | | 1 | Flag is set when EEPROM page is busy due to "write" or automatic EEPROM refresh in progress | | | | | | |
| 6 | unused | X | unused | | | | | | |
| 5 | PON | 0 | No Power-On Reset executed | | | | | | see section 4.1 |
| | | 1 | Flag is set at Power-On, flag must be cleared by writing "0" | | | | | | |
| 4 | SR | 0 | No Self-Recovery Reset or System Reset has been generated. | | | | | | see section 4.2.1 |
| | | 1 | Flag is set when Self-Recovery Reset or System Reset has been generated. | | | | | | |
| 3 | V2F | 0 | No VLOW2 Interrupt generated | | | | | | see section 4.6 |
| | | 1 | VLOW2 Interrupt generated when supply voltage drops below VLOW1 threshold | | | | | | |
| 2 | V1F | 0 | No VLOW1 Interrupt generated | | | | | | see section 4.6 |
| | | 1 | VLOW1 Interrupt generated when supply voltage drops below VLOW1 threshold | | | | | | |
| 1 to 0 | unused | X | unused | | | | | | |

Bit positions labelled as "X" are not implemented and will return a "0" when read.

3.2.5 CONTROL_RESET (address 04h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|-------|---|-------|-------|-------|-------|-------------------|-------|
| 04h | Control_Reset | X | X | X | SysR | X | X | X | X |
| Bit | Symbol | Value | Description | | | | | Reference | |
| 7 to 5 | unused | X | unused | | | | | | |
| 4 | SysR | 0 | No System Reset will be executed | | | | | see section 4.2.1 | |
| | | 1 | Set bit = "1" triggers a System Reset. After the restart of the logic, the SysR will be cleared and in bit 4 "SR" in the register Control_Status will be set. | | | | | | |
| 3 to 0 | unused | X | unused | | | | | | |

Bit positions labelled as "X" are not implemented and will return a "0" when read.

3.3 WATCH PAGE REGISTER FUNCTION

Watch Page registers are coded in the Binary Coded Decimal (BCD) format; BCD format is used to simplify application use.

3.3.1 SECONDS, MINUTES, HOURS, DAYS, WEEKDAYS, MONTHS, YEARS REGISTER**Seconds** (address 08h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|---|-------|-------|-------|-------|-------|-------|
| 08h | Seconds | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | X | - | unused | | | | | | |
| 6 to 0 | Seconds | 0 to 59 | This register holds the current seconds coded in BCD format | | | | | | |

Minutes (address 09h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|---|-------|-------|-------|-------|-------|-------|
| 09h | Minutes | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | X | - | unused | | | | | | |
| 6 to 0 | Minutes | 0 to 59 | This register holds the current seconds coded in BCD format | | | | | | |

Hours (address 0Ah...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------------------|----------|---------------|------------------------------|---|-------|-------|-------|-------|-------|
| 0Ah | Hours | X | 12-24 | 20-PM | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | X | - | unused | | | | | | |
| 12 hour mode (AM/PM) | | | | | | | | | |
| 6 | 12-24 | 0 | Selects 24-hour mode | | | | | | |
| | | 1 | Selects 12-hour (AM/PM) mode | | | | | | |
| 5 | 20-PM | 0 | Indicates AM | | | | | | |
| | | 1 | Indicates PM | | | | | | |
| 4 to 0 | Hours | ¹⁾ | 1 to 12 | This register holds the current hours coded in BCD format | | | | | |
| 24 hour mode | | | | | | | | | |
| 6 | 12-24 | 0 | Selects 24-hour mode | | | | | | |
| | | 1 | Selects 12-hour AM/PM mode | | | | | | |
| 5 to 0 | Hours | ¹⁾ | 0 to 23 | This register holds the current hours coded in BCD format | | | | | |

¹⁾ User is requested to pay attention setting valid data only.

Days (address 0Bh...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|--|-------|-------|-------|-------|-------|-------|
| 0Bh | Days | X | X | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 to 6 | X | - | unused | | | | | | |
| 5 to 0 | Days | 1 to 31 | This register holds the current days coded in BCD format ¹⁾ | | | | | | |

¹⁾ The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4; including the year 00.

Weekdays (address 0Ch...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|-----------|----------|--------|--|-------|-------|-------|-------|-------|-------|-------|
| 0Ch | Weekdays | X | X | X | X | X | 4 | 2 | 1 | |
| Bit | Symbol | Value | Description | | | | | | | |
| 7 to 3 | X | - | unused | | | | | | | |
| 2 to 0 | Weekdays | 1 to 7 | This register holds the current weekdays coded in BCD format ¹⁾ | | | | | | | |
| Weekdays | | 1) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Sunday | | X | X | X | X | X | 0 | 0 | 1 | |
| Monday | | X | X | X | X | X | 0 | 1 | 0 | |
| Tuesday | | X | X | X | X | X | 0 | 1 | 1 | |
| Wednesday | | X | X | X | X | X | 1 | 0 | 0 | |
| Thursday | | X | X | X | X | X | 1 | 0 | 1 | |
| Friday | | X | X | X | X | X | 1 | 1 | 0 | |
| Saturday | | X | X | X | X | X | 1 | 1 | 1 | |

¹⁾ These bits may be re-assigned by the user.

Months (address 0Dh...bits description)

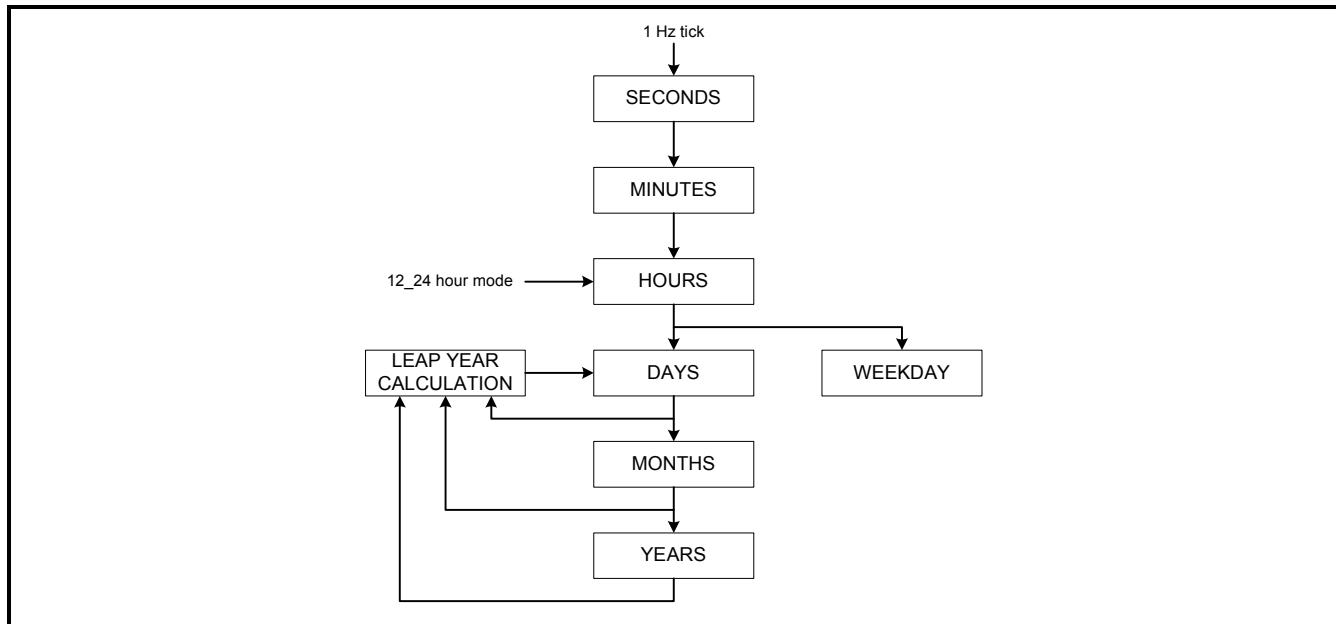
| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|----------|---------|--|-------|-------|-------|-------|-------|-------|
| 0Dh | Months | X | X | X | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 to 5 | X | - | unused | | | | | | |
| 4 to 0 | Months | 1 to 12 | This register holds the current months coded in BCD format ¹⁾ | | | | | | |
| Months | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| January | | X | X | X | 0 | 0 | 0 | 0 | 1 |
| February | | X | X | X | 0 | 0 | 0 | 1 | 0 |
| March | | X | X | X | 0 | 0 | 0 | 1 | 1 |
| April | | X | X | X | 0 | 0 | 1 | 0 | 0 |
| May | | X | X | X | 0 | 0 | 1 | 0 | 1 |
| June | | X | X | X | 0 | 0 | 1 | 1 | 0 |
| July | | X | X | X | 0 | 0 | 1 | 1 | 1 |
| August | | X | X | X | 0 | 1 | 0 | 0 | 0 |
| September | | X | X | X | 0 | 1 | 0 | 0 | 1 |
| October | | X | X | X | 1 | 0 | 0 | 0 | 0 |
| November | | X | X | X | 1 | 0 | 0 | 0 | 1 |
| December | | X | X | X | 1 | 0 | 0 | 1 | 0 |

¹⁾ The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4; including the year 00.

Years (address 0Eh...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|---------|---|-------|-------|-------|-------|-------|-------|
| 0Eh | Years | X | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | X | - | unused | | | | | | |
| 6 to 0 | Years | 0 to 79 | this register holds the current year 20xx coded in BCD format ¹⁾ | | | | | | |

¹⁾ The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4; including the year 00.

3.3.2 DATA FLOW OF TIME AND DATE FUNCTION

3.4 ALARM PAGE REGISTER FUNCTION

The Alarm Page registers contain alarm information. When one or more of these registers are loaded with a valid second, minute, hour, day, weekday, month or year information and its corresponding alarm enable bit (AE_x) is logic “1”, then that information will be compared with the current time / date information in the Watch Page registers.

When all enabled comparisons first match (wired “AND”) and the AIE Flag (bit 0 in register Control_INT) is enabled, then the AF Flag (bit 0 in register Control_INT) is set = “1” and an Interrupt signal becomes available at pin #7.

Disabled Alarm registers which have their corresponding bit AE_X at logic “0” are ignored.

3.4.1 SECONDS, MINUTES, HOURS, DAYS, WEEKDAYS, MONTHS, YEARS ALARM REGISTER

Alarm Seconds (address 10h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|---------|--|-------|-------|-------|-------|-------|-------|
| 10h | Second Alarm | AE_S | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_S | 0 | Second Alarm is disabled | | | | | | |
| | | 1 | Second Alarm is enabled | | | | | | |
| 6 to 0 | Seconds Alarm | 0 to 59 | These bits hold the Second Alarm information coded in BCD format | | | | | | |

Alarm Minutes (address 11h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|---------|--|-------|-------|-------|-------|-------|-------|
| 11h | Minute Alarm | AE_M | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_M | 0 | Minute Alarm is disabled | | | | | | |
| | | 1 | Minute Alarm is enabled | | | | | | |
| 6 to 0 | Minutes Alarm | 0 to 59 | These bits hold the Minute Alarm information coded in BCD format | | | | | | |

Alarm Hours (address 12h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------------|-------------|---------|---|-------|-------|-------|-------|-------|-------|
| 12h | Hours Alarm | AE_H | 12-24 | 20-PM | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_H | 0 | Hour Alarm is disabled | | | | | | |
| | | 1 | Hour Alarm is enabled | | | | | | |
| 6 | X | - | unused | | | | | | |
| 12 hour mode (AM/PM) | | | | | | | | | |
| 5 | 20-PM | 0 | indicates AM | | | | | | |
| | | 1 | indicates PM | | | | | | |
| 4 to 0 | Hours Alarm | 1 to 12 | These registers hold the Hours Alarm information coded in BCD format when in 12 hour mode | | | | | | |
| 24 hour mode | | | | | | | | | |
| 5 to 0 | Hours Alarm | 0 to 23 | These registers hold the Hours Alarm information coded in BCD format when in 24 hour mode | | | | | | |

Alarm Days (address 13h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|---------|---|-------|-------|-------|-------|-------|-------|
| 13h | Days Alarm | AE_D | X | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_D | 0 | Day Alarm is disabled | | | | | | |
| | | 1 | Day Alarm is enabled | | | | | | |
| 6 | X | - | unused | | | | | | |
| 5 to 0 | Days Alarm | 1 to 31 | These registers hold the Day Alarm information coded in BCD | | | | | | |

Alarm Weekdays (address 14h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------------|--------|---|-------|-------|-------|-------|-------|-------|
| 14h | Weekday Alarm | AE_W | X | X | X | X | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_W | 0 | Weekday Alarm is disabled | | | | | | |
| | | 1 | Weekday Alarm is enabled | | | | | | |
| 6 to 3 | X | - | unused | | | | | | |
| 2 to 0 | Weekday Alarm | 1 to 7 | These registers hold the Weekday Alarm information coded in BCD | | | | | | |

Alarm Months (address 15h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|---------|--|-------|-------|-------|-------|-------|-------|
| 15h | Months Alarm | AE_M | X | X | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_M | 0 | Months Alarm is disabled | | | | | | |
| | | 1 | Months Alarm is enabled | | | | | | |
| 6 to 5 | X | - | unused | | | | | | |
| 4 to 0 | Months Alarm | 1 to 12 | These registers hold the Months Alarm information coded in BCD | | | | | | |

Alarm Years (address 16h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|---------|--|-------|-------|-------|-------|-------|-------|
| 16h | Year Alarm | AE_Y | 40 | 20 | 10 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | AE_Y | 0 | Year Alarm is disabled | | | | | | |
| | | 1 | Year Alarm is enabled | | | | | | |
| 6 to 0 | Year Alarm | 0 to 79 | These registers hold the Year Alarm information coded in BCD | | | | | | |

3.5 TIMER PAGE REGISTER FUNCTION

The Timer Page contains 2 registers forming a 16-bit count down timer value.

Countdown Timer Value (address 18h / 19h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|----------|---|-------|-------|-------|-------|-------|-------|
| 18h | Timer Low | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 19h | Timer High | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Address | Symbol | Value | Description | | | | | | |
| 18h | Timer Low | 1 to 255 | These bits hold the Low Countdown Timer Value in binary format | | | | | | |
| 19h | Timer High | 0 to 255 | These bits hold the High Countdown Timer Value in binary format | | | | | | |

3.6 TEMPERATURE PAGE REGISTER FUNCTION

The Temperature Page register contains the result of the measured temperature ranging from -60°C (=0d) to +190°C (=250d) with 0°C corresponding to a content of =60d.

During read / write access, the content of the register Temperature is frozen in a cache memory to prevent faulty reading.

When the Thermometer is disabled by ThE = "0" (bit 1 in register EEPROM_Control), the register Temperature at address 20h can be externally written.

Temperature Value (address 20h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|---------------|--|-------|-------|-------|-------|-------|-------|
| 20h | Temperature | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Address | Symbol | Value | Description | | | | | | |
| 20h | Temperature | -60 to +194°C | These bits hold the Temperature Value coded in binary format | | | | | | |

3.7 EEPROM DATA PAGE REGISTER FUNCTION

The EEPROM Data Page contains 2 non-volatile EEPROM registers for user's application.

Please see section 4.3 EEPROM Memory Access on page 25 for detailed instructions how to handle EEPROM read / write access.

User EEPROM Data Registers (address 28h / 29h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|----------|----------------------------|-------|-------|-------|-------|-------|-------|
| 28h | EEPROM User | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 29h | EEPROM User | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Address | Symbol | Value | Description | | | | | | |
| 28h | EEPROM User | 0 to 255 | EEPROM User Data (2 Bytes) | | | | | | |
| 29h | EEPROM User | 0 to 255 | | | | | | | |

3.8 EEPROM CONTROL PAGE REGISTER FUNCTION

The EEPROM Control Page contains 4 non-volatile EEPROM registers.

With Register EEPROM Control, the settings for Trickle-Charger (bit 7-4), the CLKOUT frequency (bit 3&2) and the Thermometer (bit 1&0) can be controlled.

The registers XTAL Offset, XTAL Coef and XTAL T0 contain the factory calibrated, individual crystal parameters to compensate the frequency deviation over the temperature range.

Please see section 4.3 EEPROM Memory Access on page 25 for detailed instructions how to handle EEPROM read / write access.

3.8.1 EEPROM CONTROL (address 30h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------|----------------|-------|---|-------|-------|-------|-------|-------|-------------------|--|
| 30h | EEPROM Control | R80k | R20k | R5k | R1k | FD1 | FD0 | ThE | ThP | |
| Bit | R80k | 0 | Disables 80 kΩ trickle charge resistor | | | | | | see section 4.1 | |
| | | 1 | Enables 80 kΩ trickle charge resistor | | | | | | | |
| | R20k | 0 | Disables 20 kΩ trickle charge resistor | | | | | | | |
| | | 1 | Enables 20 kΩ trickle charge resistor | | | | | | | |
| | R5k | 0 | Disables 5 kΩ trickle charge resistor | | | | | | | |
| | | 1 | Enables 5 kΩ trickle charge resistor | | | | | | | |
| | R1k | 0 | Disables 1.5 kΩ trickle charge resistor | | | | | | | |
| | | 1 | Enables 1.5 kΩ trickle charge resistor | | | | | | | |
| | FD1 | 00 | Selects Clock Frequency at CLKOUT pin | | | | | | see section 4.9 | |
| | FD0 | 01 | | | | | | | | |
| | ThE | 10 | | | | | | | | |
| | | 11 | | | | | | | | |
| | ThP | 0 | Disables Thermometer | | | | | | see section 5.2.1 | |
| | | 1 | Enables Thermometer | | | | | | | |
| | ThP | 0 | set Temperature Scanning Interval: 1 Second | | | | | | see section 5.2.1 | |
| | | 1 | set Temperature Scanning Interval: 16 seconds | | | | | | | |

3.8.2 XTAL OFFSET (address 31h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------|-------------|----------|---|-------|-------|-------|-------|-------|-------------------|--|
| 31h | XTAL Offset | sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | |
| Bit | sign | 0 | - deviation (slower) of 32.768kHz frequency at T0 | | | | | | see section 5.2.2 | |
| | | 1 | + deviation (faster) of 32.768kHz frequency at T0 | | | | | | | |
| | XTAL Offset | 0 to 121 | Frequency Offset Compensation value | | | | | | | |
| | | 1 | | | | | | | | |

¹⁾ The XTAL Offset register value is factory programmed according to the crystal's initial frequency-tolerance. For best time-accuracy, the content of this register must not be changed by the user.

3.8.3 XTAL TEMPERATUR COEFFICIENT (address 32h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|-------|---|-------|-------|-------|-------|-------|-------------------|
| 32h | XTAL Coef | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Bit | XTAL Coef | 0 | Quadratic Coefficient of XTAL's Temperature Drift | | | | | | see section 5.2.2 |
| | | 1 | | | | | | | |

¹⁾ The XTAL Coef register value is factory programmed according to the crystal parameters over temperature. For best time-accuracy, the content of this register must not be changed by the user.

3.8.4 XTAL TURNOVER TEMPERATUR COEFFICIENT T0 (address 33h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-----------------------|------------------------------------|-------|-------|-------|-------|-------------------|-------|
| 33h | XTAL T0 | x | x | 32 | 16 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | Reference | |
| 7 to 6 | x | - | unused | | | | | | |
| 5 to 0 | XTAL T0 | ¹⁾ 4 to 67 | XTAL's Turnover Temperature in °C. | | | | | see section 5.2.2 | |

¹⁾ The XTAL T0 register value is factory programmed according to the crystal parameters over temperature. For best time-accuracy, the content of this register must not be changed by the user.

3.9 RAM DATA PAGE REGISTER FUNCTION

The RAM Data Page contains 8 RAM registers for user's application.

User RAM Data Registers (address 38h to 3Fh...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|----------|-------------------------|-------|-------|-------|-------|-------|-------|
| 38h | RAM User | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| --- | --- | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 3Fh | RAM User | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Address | Symbol | Value | Description | | | | | | |
| 38h | RAM User | 0 to 255 | RAM User Data (8 Bytes) | | | | | | |
| --- | --- | --- | | | | | | | |
| 3Fh | RAM User | 0 to 255 | | | | | | | |

4.0 DETAILED FUNCTIONAL DESCRIPTION

4.1 POWER-UP, POWER MANAGEMENT AND BATTERY SWITCHOVER

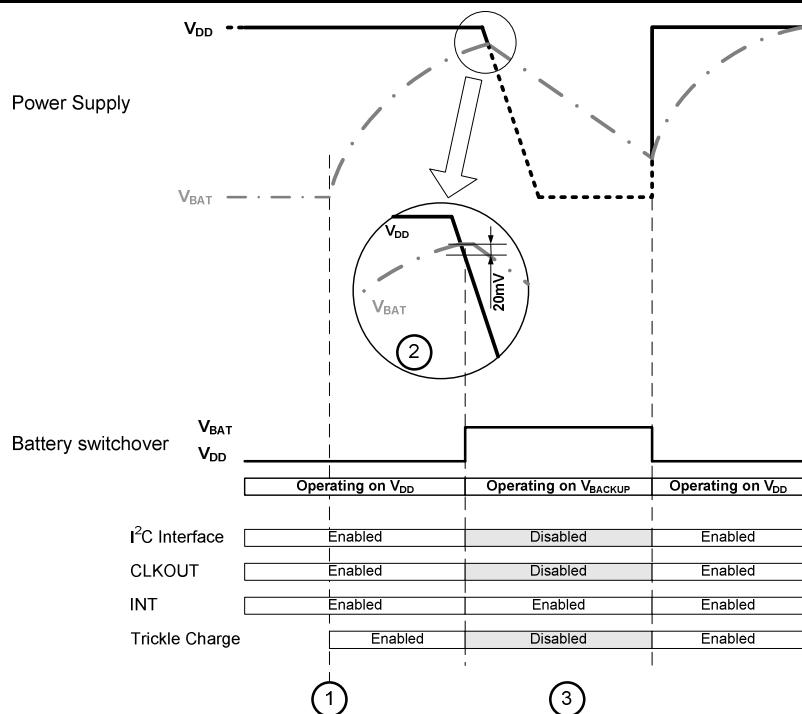
The RV-3029-C2 has two power supply pins:

- V_{DD} pin #1 the main power supply input pin
- V_{BACKUP} pin #8 the backup battery input pin

The RV-3029-C2 has multiple power management function implemented:

- Automatic switchover function between main power supply and backup supply voltage. The higher supply voltage is selected automatically, with a switchover hysteresis of 20mV.
- Low supply voltage detection V_{LOW1} and V_{LOW2} with the possibility to generate an INT if the corresponding control bits are enabled.
- Functions requiring a minimum supply voltage are automatically disabled if low supply voltage is detected.
- Interface and CLKOUT are automatically disabled when the device operates in backup supply mode.
- Programmable trickle charge circuitry to charge backup battery or supercap.

Backup Switchover Circuitry Disables non-used Functions



- ① Trickle charge circuitry is enabled by software when selecting trickle-charge resistors. When back-up supply switchover-circuitry switches to the backup supply voltage, trickle charge function is disabled.
- ② The implemented backup switchover circuitry continuously compares V_{DD} and V_{BACKUP} voltages and connects the higher of them to the internal supply voltage V_{INT} . The switchover hysteresis from V_{DD} to V_{BACKUP} and vice versa is typically 20mV.
- ③ When the device is operating at the V_{BACKUP} supply voltage, non used RTC functions are disabled to ensure optimized power consumption:
 - I²C Interface Disabled when operating in V_{BACKUP} mode.
 - CLKOUT Disabled when operating in V_{BACKUP} mode.
 - INT Enabled even when operating in V_{BACKUP} mode.
 - Trickle Charge Disabled when operating in V_{BACKUP} mode.

4.1.1 POWER UP SEQUENCE

The device can be either powered up from main supply V_{DD} pin #1 or from backup supply V_{BACKUP} pin #8.

During power-up, the chip is executing the following power-up procedure:

- The implemented battery switchover circuitry compares V_{DD} and V_{BACKUP} voltages and connects the higher of them to supply the chip.
- At power-up, the chip is kept in Reset state until the supply voltage reaches an internal threshold level. Once the supply voltage is higher than this threshold level, a Reset is executed and registers are loaded with the Register Reset Values described in section 4.2.2 on page 24.
- After the Reset is executed and registers are loaded with the Register Reset Values, “PON” is set = “1” (bit 5 in Register Control-Status), it needs to be cleared by writing = “0”.
- Once the supply voltage reaches the oscillator start-up voltage, the oscillator-circuitry starts the 32.768kHz “tuning-fork” Crystal typically within 500 ms.
- Once the 32.768kHz clocks are present, the Voltage Detector starts in fast mode to measure the supply voltage.
- When a supply voltage $>V_{Low2}$ is detected, the fast mode voltage detection is stopped, and the EEPROM read is enabled.
- Configuration registers are loaded with the configuration data read from the EEPROM Control Page and the bits V_{Low1} and V_{Low2} are reset = “0”.
- If the Thermometer is enabled by “ThE” = “1” (bit 1 in register EEPROM_Control), the temperature is measured and the frequency compensation value for time correction is calculated.
- The RV-3029-C2 becomes fully functional, the correct Time / Date informations need to be loaded into the corresponding registers and bit 5 “PON” in Register Control-Status needs to be cleared by writing “0”.

Note: 1

During power up, the Low Voltage Detection is monitoring the supply voltage at an accelerated scan rate increasing the current consumption of the device.

Once power supply voltage exceed V_{Low2} threshold, the flags V_{Low1} and V_{Low2} are cleared and the scan rate for the low voltage detection is set to 1 second to ensure optimized power consumption.

Note: 2

Please note the different meaning of the “PON”, “ V_{Low1} ” and “ V_{Low2} ” Flags:

PON

“PON” Flag is set after Power-Up Reset is executed

- Indicating that time & date information are corrupted

V_{Low1}

V_{Low1} Flag is set when supply voltage drops below V_{Low1} threshold.

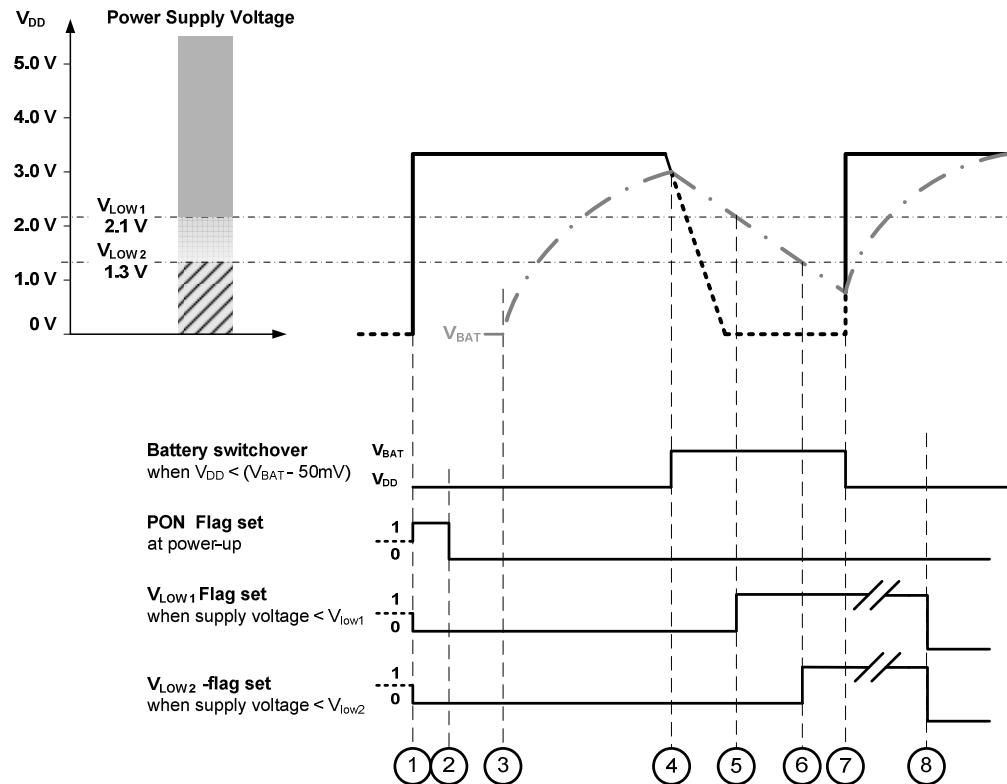
- Indicating that the Thermometer might have been disabled due to low supply voltage and the temperature compensation was operating for a while with the last temperature reading causing bigger time-deviation.

V_{Low2}

V_{Low1} Flag is set when supply voltage drops below V_{Low2} threshold.

- Indicating a risk that the 32.768kHz might have stopped due to low supply voltage and that the time & date information might be corrupted.

Example Power Up sequence, Low Voltage detection and Backup Supply switchover



- ① Power Up Reset is executed; registers are loaded with Reset Values. PON flag is set at Power up indicating that time / date information likely are corrupted.
Low voltage detection flags V_{LOW1} and V_{LOW2} are automatically cleared.
- ② PON Flag needs to be cleared by software writing "0".
- ③ Trickle charge circuitry for backup battery can be enabled by software.
- ④ Switchover to the backup supply voltage when $V_{DD} < (V_{BAT} - 20mV)$.
- ⑤ Low voltage detection sets V_{LOW1} Flag when supply voltage drops V_{LOW1} threshold.
- ⑥ Low voltage detection sets V_{LOW2} Flag when supply voltage drops V_{LOW2} threshold.
- ⑦ Switchback from backup supply voltage to main supply voltage when $V_{DD} > (V_{BAT} + 20mV)$.
- ⑧ V_{LOW1} and V_{LOW2} Flags need to be cleared by software writing "0".

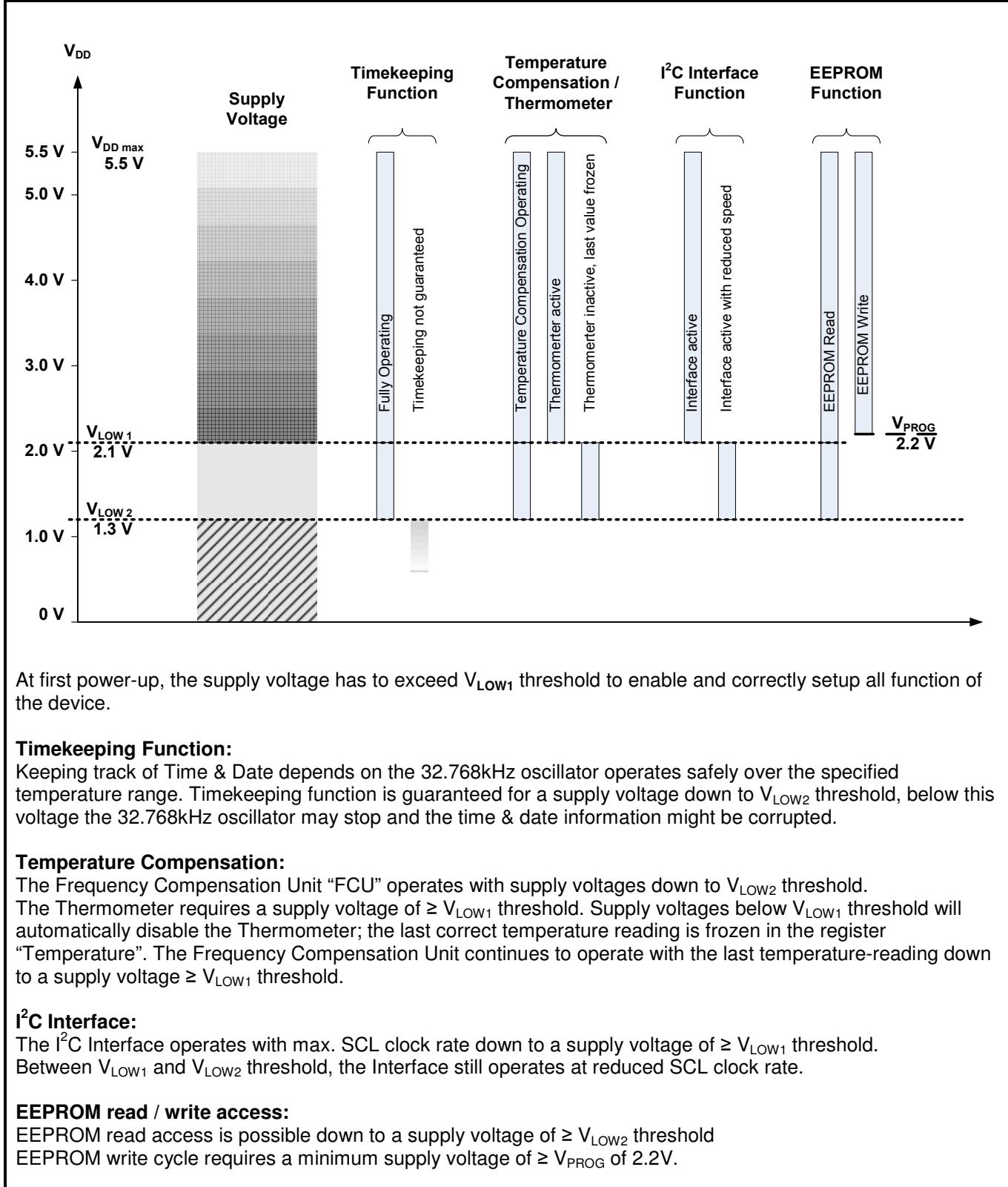
4.1.2 SUPPLY VOLTAGE OPERATING RANGE AND LOW VOLTAGE DETECTION

The RV-3029-C2 has built-in low supply voltage detection which periodically monitors supply voltage levels vs. V_{LOW1} and V_{LOW2} thresholds.

If low supply voltage is detected, the corresponding flags V_{LOW1} and V_{LOW2} are set = "1".
Device functions critical to low supply voltage are disabled.

During power up, the Low Voltage Detection is monitoring the supply voltage at an accelerated scan rate.
If power supply voltage exceed V_{LOW2} threshold, the flags V_{LOW1} and V_{LOW2} are cleared and the scan rate for the low voltage detection is set to 1 second.

Minimum Supply Voltage and Low Voltage Detection



4.2 RESET

A Reset can be initiated by 3 different ways:

- Power On Reset (automatically initiated at power-up)
- Software Reset (can be initiated by software)
- Self-Recovery System Reset (automatically initiated if enabled by Software and possible deadlock is detected)

4.2.1 POWER-UP RESET, SYSTEM RESET AND SELF-RECOVERY RESET

Power On Reset

A Reset is automatically generated at Power On.

After Power-On Reset has been executed, bit 5 "PON" in Register Control_Status is set = "1", it needs to be cleared by writing = "0".

System Reset

A Software Reset can be initiated when the System-Reset command "SysR" is set = "1" (bit 4 in Register Control_Reset). If a System-Reset is executed, the "SR" Flag (bit 4 in Register Control_Status) is set = "1", needs to be cleared by writing = "0".

It is generally recommended to make a System Reset by Software after power-up.

Note: Please consider the Register Reset Values shown in section 4.2.1 on page 24.

After a Reset has been executed, Self-Recovery System "SROn" (bit 4 in Register Control_1) is set = "1" and Self-Recovery INT Enable "SRIE" (bit 4 in Register Control_INT) is set = "0".

Self-Recovery System Reset

A Self-Recovery System Reset will be automatically initiated when the Self-Recovery function is Enabled by bit 4 "SROn" in Register Control_1 is set "1" and internally a possible deadlock-state is detected.

If a Self-Recovery System Reset is executed, the bit 4 "SR" in Register Control_Status is set "1" and need to be cleared by writing "0".

After a Self-Recovery System Reset is executed and Register Reset Values were written, bit 4 "SRF" in Register Control_INT Flag is set "1" and need to be cleared by writing "0".

In case of a Self Recovery System Reset is executed, an Interrupt is available if Self-Recovery-INT function is Enabled by bit 4 "SRIE" in Register Control_INT is set "1".

The purpose of the Self Recovery function is to generate an internal System Reset in case the on-chip state machine goes into a deadlock. The function is based on an internal counter that is periodically reset by the control logic. If the counter is not reset on time, a possible deadlock is detected and a System Reset will be triggered. The System Reset is executed latest after 2 temperature- or voltage-monitoring periods defined in Thermometer Period bit 0 "ThP" in Register EEPROM Control, i.e. latest after 2 or 32 seconds.

Note: Please consider the Register Reset Values shown in section 4.2.1 on page 24.

After a Reset has been executed, Self-Recovery System bit 4 "SROn" in Register Control_1 = "1" and Self-Recovery INT Enable "SRIE" in Register Control_INT = "0".

4.2.2 REGISTER RESET VALUES

| Address | | | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------------------|-----------|-----|------------------|--|-------|---|-----------------|-------|-------|-------|-------|--|
| Page | Address | Hex | | | | | | | | | | |
| Bit 7 - 3 | Bit 2 - 0 | | | | | | | | | | | |
| Control page | 000 | 00h | Control_1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | |
| | 001 | 01h | Control_INT | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| | 00000 | 02h | Control_INT Flag | - | - | - | 0 ¹⁾ | 0 | 0 | 0 | 0 | |
| | 011 | 03h | Control_Status | EEbusy | X | 1 | 1 | 1 | 1 | X | X | |
| | 100 | 04h | Control_Reset | - | - | - | 0 | - | - | - | - | |
| Clock page | 000 | 08h | Seconds | - | X | X | X | X | X | X | X | |
| | 001 | 09h | Minutes | - | X | X | X | X | X | X | X | |
| | 00001 | 0Ah | Hours | - | X | X | X | X | X | X | X | |
| | 011 | 0Bh | Days | - | - | X | X | X | X | X | X | |
| | 100 | 0Ch | Weekdays | - | - | - | - | - | X | X | X | |
| | 101 | 0Dh | Months | - | - | - | X | X | X | X | X | |
| | 110 | 0Eh | Years | - | X | X | X | X | X | X | X | |
| Alarm page | 000 | 10h | Second Alarm | AE_S | X | X | X | X | X | X | X | |
| | 001 | 11h | Minute Alarm | AE_M | X | X | X | X | X | X | X | |
| | 00010 | 12h | Hour Alarm | AE_H | X | X | X | X | X | X | X | |
| | 011 | 13h | Days Alarm | AE_D | - | X | X | X | X | X | X | |
| | 100 | 14h | Weekday Alarm | AE_W | - | - | - | - | X | X | X | |
| | 101 | 15h | Months Alarm | AE_M | - | - | X | X | X | X | X | |
| | 110 | 16h | Year Alarm | AE_Y | X | X | X | X | X | X | X | |
| Timer page | 000 | 18h | Timer Low | X | X | X | X | X | X | X | X | |
| | 001 | 19h | Timer High | X | X | X | X | X | X | X | X | |
| Temperature page | 000 | 20h | Temperature | X | X | X | X | X | X | X | X | |
| EEPROM User | 000 | 28h | EEPROM User | 2 bytes of EEPROM for user data | | | | | | | | |
| | 00101 | 29h | EEPROM User | | | | | | | | | |
| EEPROM Control page | 000 | 30h | EEPROM Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| | 00110 | 31h | Xtal Offset | <i>Factory setting: Xtal frequency deviation</i> | | | | | | | | |
| | 010 | 32h | Xtal Coef | <i>Factory setting: Xtal temperature coefficient</i> | | | | | | | | |
| | 011 | 33h | Xtal T0 | - | - | <i>Factory setting: Xtal T0 temperature</i> | | | | | | |
| RAM page | 000 | 38h | User RAM | 8 bytes of RAM for user data | | | | | | | | |
| | : | : | | | | | | | | | | |
| | 00111 | 3Fh | | | | | | | | | | |

- bits labelled as – are not implemented

X bits labelled as X are undefined at power-up and unchanged by subsequent resets.

¹⁾ If a Self Recovery System Reset was executed, a “1” will be written into SRF flag thereafter.

After Reset, the following mode is entered:

- CLKOUT is selected at pin #2, default frequency is 32.768 kHz defined in register EEPROM Control.
- Internal Timer Source Clock frequency is set to 32Hz.
- Self Recovery function is enabled
- Automatic EEPROM Refresh every hour is enabled
- Timer and Timer Auto-Reload mode are disabled
- All Interrupts are disabled
- No Alarm is set
- At Power-On Reset, “PON” Flag is set = “1” and has to be cleared by writing = “0”.
- At Self-Recovery Reset or System Reset, “SR” Flag is set = “1” and has to be cleared by writing = “0”.
- 24 hour mode is selected

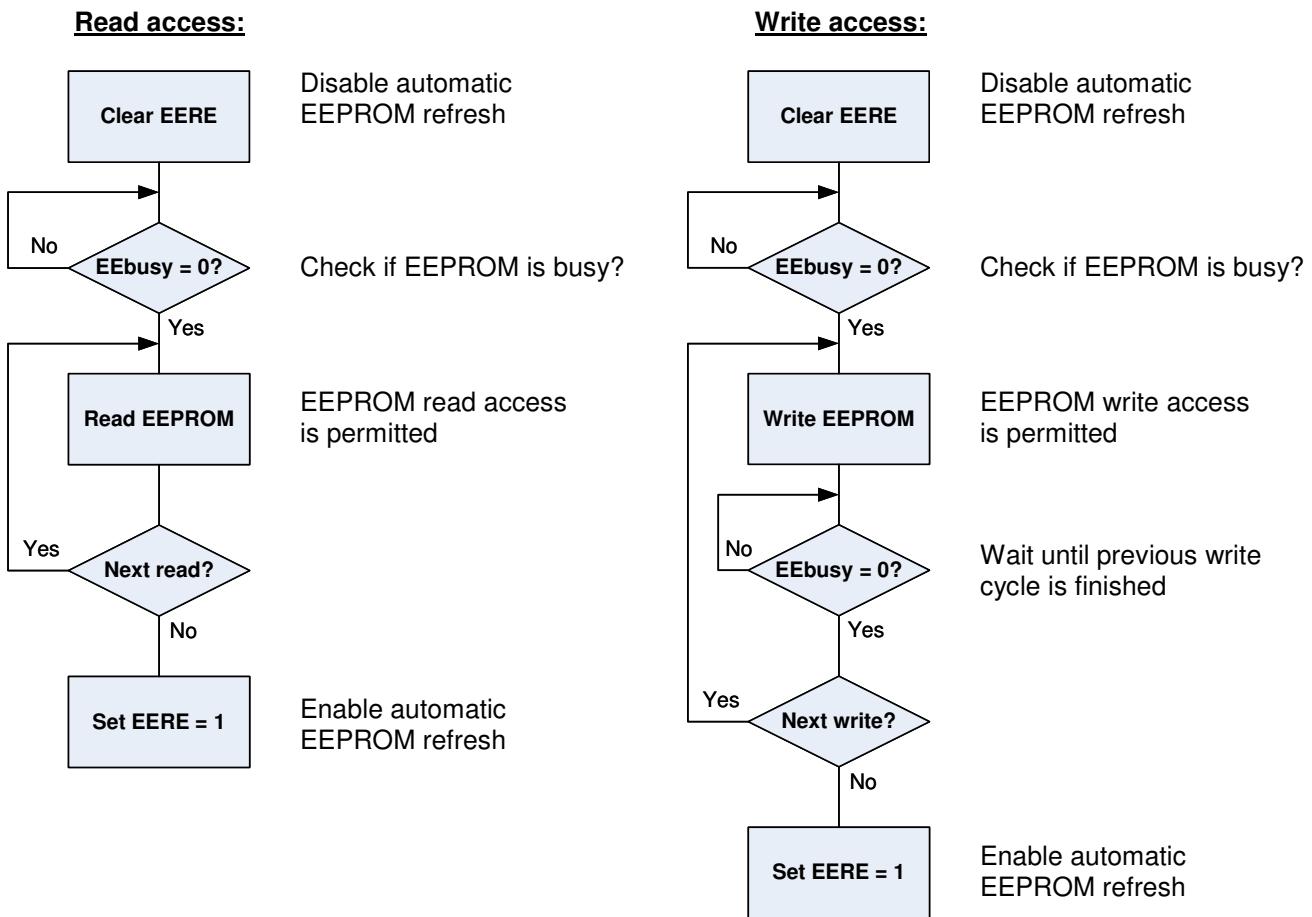
4.3 EEPROM MEMORY ACCESS

The EEPROM Memory has a built-in automatic EEPROM Refresh function, controlled by “EERE” (bit 3 in register Control_1). If enabled, this function automatically refreshes the content of the EEPROM Memory Pages once an hour.

The “EEbusy” will be set = “1” (bit 7 in register Control_Status) if the EEPROM Memory Pages are busy due to write or automatic refresh cycle is in progress. “EEbusy” goes = “0” when writing is finished, EEPROM Memory Pages shall only be accessed when not busy, i.e. when “EEbusy” = “0”.

A special EEPROM access procedure is required preventing access collision between the internal automatic EEPROM refresh cycle and external read / write access through Interface.

- Set “EERE” = “0” Automatic EEPROM Refresh needs to be disabled before EEPROM access.
- Check for “EEbusy” = “0” Access EEPROM only if not busy.
- Set “EERE” = “1” It is recommended to enable Automatic EEPROM Refresh at the end of read / write access.



Note: A minimum power supply voltage of $V_{PROG} = 2.2V$ is required during the whole EEPROM write procedure; i.e. until "EEbusy" = "0".

4.4 TIMER FUNCTION

The RV-3029-C2 offers different Alarm and Timer functions which allow simply generating highly versatile timing-functions.

The Countdown Timer is controlled by the register Control_1. Bit 1 "TE" enables the Timer function; bits 5 & 6 "TD0" and "TD1" determine one of 4 Timer Source Clock frequencies (32 Hz, 8 Hz, 1 Hz, or 0.5Hz).

The Timer counts down from a software-loaded 16-bit binary value ,n', "Timer Low" (bit 0-7 at address 18h) and "Timer High" (bit 0-7 at address 19h). Values, n' from 1 to 65536 are valid; loading the counter with ,n' = "0" effectively stops the timer. The end of every Timer countdown is achieved when the Timer Counter value ,n' reaches = "0".

Countdown Timer can be set in Automatic Reload mode by "TAR" = "1" (bit 2 of register Control_1), the counter automatically re-loads Timer countdown value ,n' and starts the next Timer period. Automatic reload of the countdown value ,n' requires 1 additional timer source clock. This additional timer source clock has no effect on the first Timer period, but it has to be taken into account since it results in a Timer duration of ,n+1' for subsequent timer periods.

The generation of Interrupts from the Countdown Timer function is enabled by "TIE" = "1" (bit 1 in register Control_INT). If Timer Interrupt is enabled by "TIE" = "1", the Timer Flag "TF" (bit 1 in register Control_INT Flag) will be set = "1" at the end of every Timer countdown. The Interrupt signal INT on pin #8 follows the condition of Timer Flag "TF" (bit 1 in register Control_INT Flag), the INT signal can be cleared by clearing the "TF" = "0".

Control of the Countdown Timer Functions (address 00h bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|---------|---|-------|-------|-------|-------|-------|-------|
| 00h | Control_1 | Clk/Int | TD1 | TD0 | SROn | EERE | TAR | TE | WE |
| Bit | Symbol | Value | Description | | | | | | |
| 6 | TD1 | 00 | Timer Source Clock Frequency: 32 Hz | | | | | | |
| | | 01 | Timer Source Clock Frequency: 8 Hz | | | | | | |
| 5 | TD0 | 10 | Timer Source Clock Frequency: 1 Hz | | | | | | |
| | | 11 | Timer Source Clock Frequency : 0.5 Hz | | | | | | |
| 2 | TAR | 0 | Disables Countdown Timer Auto-Reload mode | | | | | | |
| | | 1 | Enables Countdown Timer Auto-Reload mode | | | | | | |
| 1 | TE | 0 | Disables Countdown Timer | | | | | | |
| | | 1 | Enables Countdown Timer | | | | | | |

The Timer Source Clock Frequency "TD0" & "TD1" and the Timer Auto Reload mode "TAR" can only be written when the Timer is stopped by "TE" = "0" (bit 1 in register Control_1).

The Countdown Timer values in "Timer Low" and "Timer High" can only be written when the Timer is stopped by "TE" = "0" and Timer Auto Reload mode is disabled "TAR" = "0".

Register Countdown Timer (address 18h / 19h bits description)

Register 18h is loaded with the low byte of the 16-bit Countdown Timer value ,n'

Register 19h is loaded with the high byte of the 16-bit Countdown Timer value ,n'

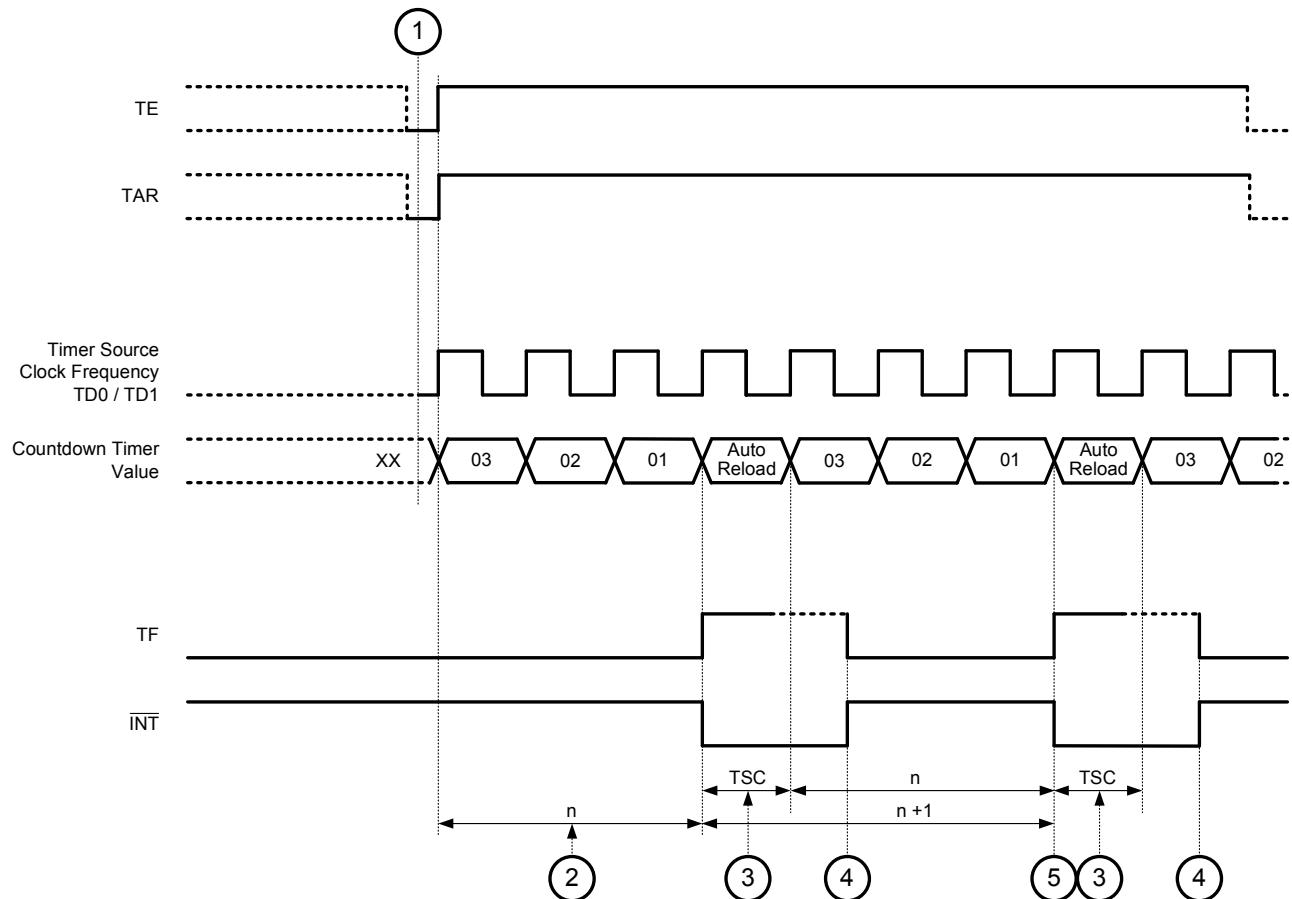
| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------|--------------|---|-------|-------|-------|-------|-------|-------|
| 18h | Timer Low | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 19h | Timer High | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 18h | Timer Low | xx01 to xxFF | Countdown value = n | | | | | | |
| | | | Countdown period = $\frac{n}{SourceClockFrequency}$ | | | | | | |
| 19h | Timer High | 00xx to FFxx | | | | | | | |

Example Countdown Timer function with Timer in Auto Reload mode

In this example, the Countdown Timer is set to Automatic Reload Mode, the Countdown Timer value is set = "3".

Automatic reload of the countdown value ,n' requires 1 additional Timer Source Clock. This additional timer source clock has no effect on the first Timer period but it has to be taken into account since it results in a Timer duration of ,n+1' for subsequent timer periods.

The Interrupt signal (INT) is cleared by clearing the Timer Flag "TF" = "0".



- ① Timer Source Clock Frequency TD0 / TD1 can only be modified when Timer is disabled "TE" = "0" Countdown Timer value ,n' in "Timer Low" and "Timer High" only can be modified when Timer "TE" = "0" and Timer Auto Reload "TAR" = "0" are both disabled.
- ② Duration of first Timer Period =
$$\frac{n}{SourceClockFrequency}$$
 The additional timer source clock for automatic reload of the countdown Timer value ,n' has no effect on the first Timer Period.
- ③ Timer Automatic Reload mode "TAR" requires one Timer Source Clock period for automatic reload of the Countdown Timer value ,n'.
- ④ To reset Interrupt signal (INT), Timer Flag "TF" has to be cleared by writing = "0".
- ⑤ When Countdown Timer is in automatic reload mode, one additional timer source clock has to be taken into account since it results in a Timer duration of ,n+1' for subsequent timer periods.

4.4.1 TIMER INTERRUPT

The generation of Interrupts from the Countdown Timer function is enabled by “TIE” = “1” (bit 1 in register Control_INT). If Timer Interrupt is enabled by “TIE” = “1”, the Timer Flag “TF”(bit 1 in register Control_INT Flag) will be set = “1” at the end of every Timer countdown.

The Interrupt signal INT on pin #7 follows the condition of Timer Flag “TF” (bit 1 in register Control_INT Flag), the Timer Flag “TF” and the Interrupt signal (INT) remain set until cleared by software writing “TF” = “0”.

Timer Interrupt Control (address 01h / 02h bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------------|-------|--|-------|-------|-------|-------|------------|-------|
| 01h | Control_INT | X | X | X | SRIE | V2IE | V1IE | TIE | AIE |
| bit 1 | TIE | 0 | TF is disabled, no Timer Interrupt generated | | | | | | |
| | | 1 | TF is enabled, Timer Interrupt generated when Countdown Timer value reaches zero and TF is set “1”. | | | | | | |
| 02h | Control_INT Flag | X | X | X | SRF | V2IF | V1IF | TF | AF |
| bit 1 | TF | 0 | No Timer Interrupt generated | | | | | | |
| | | 1 | Timer Flag is set “1” when TIE is enabled and Countdown Timer value reaches zero, TF needs to be cleared to clear INT. | | | | | | |

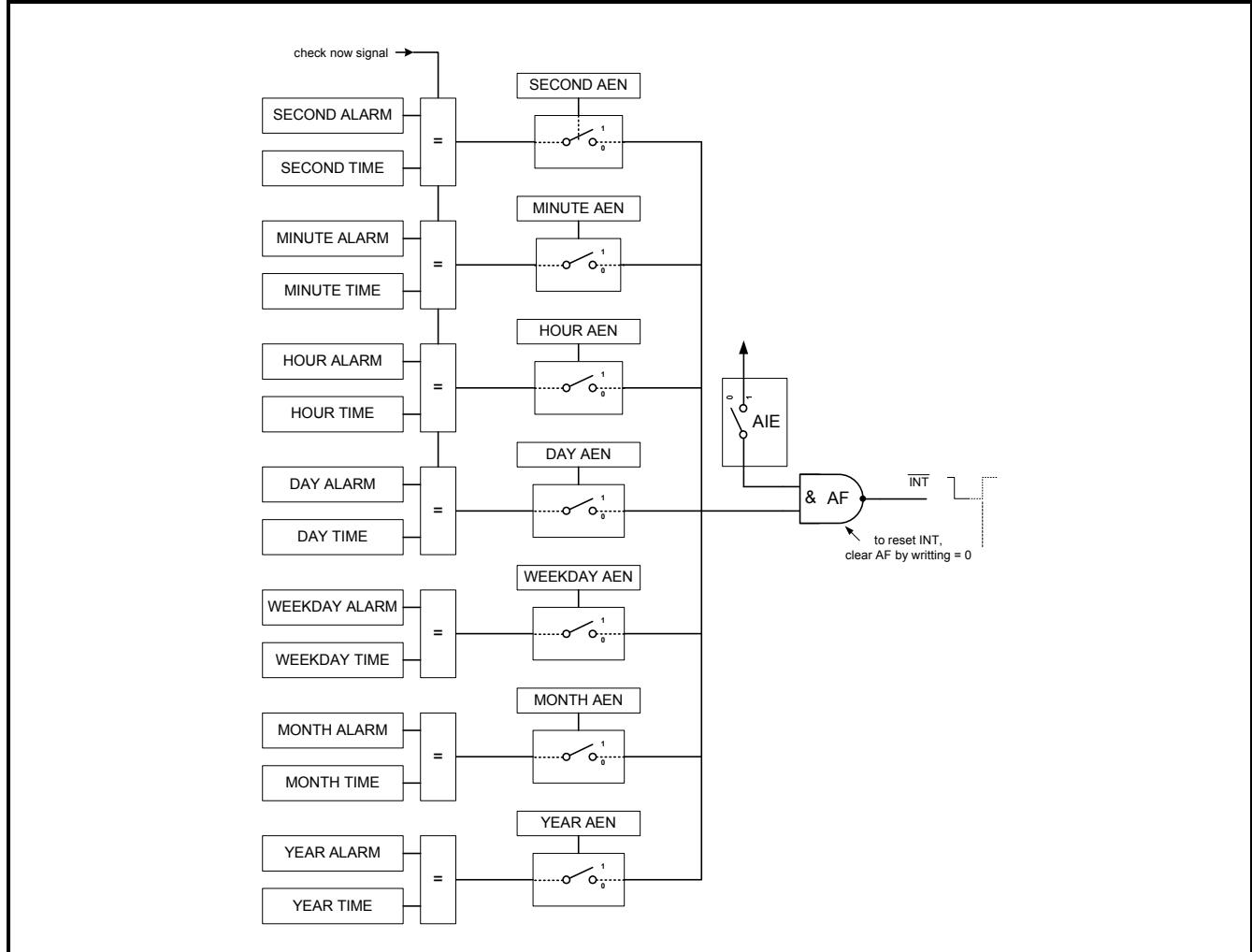
Bit positions labelled as “X” are not implemented and will return a “0” when read.

4.5 ALARM FUNCTION

Every Alarm Register in Alarm Page can be individually enabled by setting bit 7(AE_x) = "1".
Disabled alarm registers which have their bit "AE_x" at logic = "0" are ignored.

When one or more of these registers are loaded with a valid second, minute, hour, day, weekday, month or year information and its corresponding alarm enable bit (AE_x) is logic = "1", then that information will be compared with the current time / date information in Watch Page registers.

Alarm function Blockdiagram



4.5.1 ALARM INTERRUPT

The generation of Interrupts from the Alarm function is enabled by “AIE” = “1” (bit 0 in register Control_INT).

When all enabled Alarm comparisons first match (wired “AND”) and the Alarm Interrupt is enabled by, the Alarm Flag “AF” (bit 0 in Register Control_INT Flag) is set to logic = “1”.

The Interrupt signal on pin #7 follows the condition of “AF”.

The Interrupt signal INT on pin #8 follows the condition of Alarm Flag “AF” (bit 0 in register Control_INT Flag), The Alarm Flag “AF” and the Interrupt signal (INT) remain set until cleared by software writing “AF” = “0”.

Once bit “AF” has been cleared, it will only be set again when the time increments and matches the alarm condition once more.

Alarm Interrupt Control (address 01h / 02h bits description)

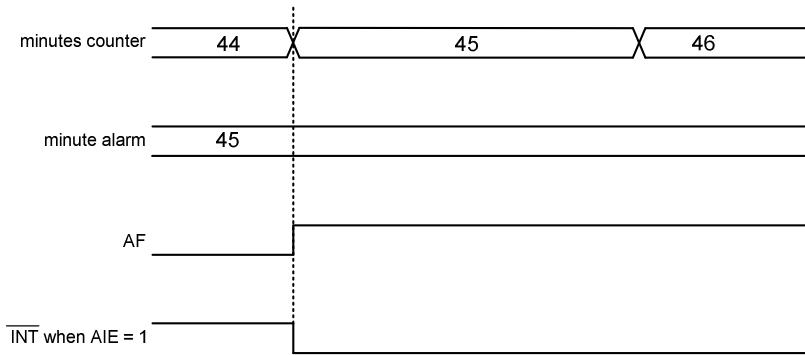
| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------------|-------|--|-------|-------|-------|-------|-------|-------|
| 01h | Control_INT | X | X | X | SRIE | V2IE | V1IE | TIE | AIE |
| 0 | AIE | 0 | AF is disabled, no Alarm Interrupt generated | | | | | | |
| | | 1 | AF is enabled, AF is set “1” and Alarm Interrupt generated when all enabled Alarm comparisons first match. | | | | | | |
| 02h | Control_INT Flag | X | X | X | SRF | V2IF | V1IF | TF | AF |
| 0 | AF | 0 | No Alarm Interrupt generated | | | | | | |
| | | 1 | Alarm Flag is set “1” when all enabled Alarm comparisons first match, needs to be cleared to clear INT. | | | | | | |

Bit positions labelled as “X” are not implemented and will return a “0” when read.

Example for Alarm Flag and Alarm INT

Example where “Minute Alarm” is enabled and set to 45 and no other Alarm is enabled.

If bit AIE is enabled, the INT pin follows the condition of bit 0 “AF” in register Control_INT Flag at address 02h.



4.6 INTERRUPT OUTPUT INT

An active LOW interrupt signal is available at INT pin #7.

The INT is an open-drain output and requires a pull-up resistor to V_{DD} .

Interrupts may be sourced from five places:

- Alarm function
- Countdown Timer function
- V_{LOW1} detection
- V_{LOW2} detection
- System Reset function

All Interrupt signals follow the condition of their corresponding flags in the bits 0 to 4 of register Control_INT Flag at address 02h.

Alarm Interrupt

Generation of interrupts from the Alarm function is enabled via “AIE” = “1” (bit 0 in register Control_INT).

If “AIE” is enabled, the INT pin follows the condition of Flag “AF” (bit 0 in register Control_INT Flag).

To clear Interrupt signal (INT), the corresponding flag “AF” needs to be cleared by writing = “0”, clearing “AF” will immediately clear INT.

Timer Interrupt

Generation of interrupts from the Countdown Timer is enabled via “TIE” = “1” (bit 1 in register Control_INT).

If “TIE” is enabled, the INT pin follows the condition of Flag “TF” (bit 1 in register Control_INT Flag).

To clear Interrupt signal (INT), the corresponding flag “TF” needs to be cleared by writing = “0”, clearing “TF” will immediately clear INT.

V_{LOW1} Interrupt

Generation of interrupts from the Voltage Low 1 detection is enabled via “V1IE” = “1” (bit 2 in register Control_INT).

If “V1IE” is enabled, the INT pin follows the condition of Flag “V1IF” (bit 2 in register Control_INT Flag).

To clear Interrupt signal (INT), both corresponding flags “V1IF” (bit 2 in register Control_INT Flag) and “V1F” (bit 2 in register Control_Status) need to be cleared by writing = “0”.

V_{LOW2} Interrupt

Generation of interrupts from the Voltage Low 2 detection is enabled via “V2IE” = “1” (bit 3 in register Control_INT).

If “V2IE” is enabled, the INT pin follows the condition of Flag “V2IF” (bit 3 in register Control_INT Flag).

To clear Interrupt signal (INT), both corresponding flags “V2IF” (bit 3 in register Control_INT Flag) and “V2F” (bit 3 in register Control_Status) need to be cleared by writing = “0”.

System Reset Interrupt

Generation of interrupts from the System Reset function is enabled via “SRIE” = “1” (bit 4 in register Control_INT). If “SRIE” is enabled, the INT pin follows the condition of Flag “SRF” (bit 4 in register Control_INT Flag). To clear Interrupt signal (INT), both corresponding flags “SRF” (bit 4 in register Control_INT Flag) and “SR” (bit 4 in register Control_Status) need to be cleared by writing = “0”.

4.7 WATCH ENABLE FUNCTION

The function Watch Enable function “WE” (bit 0 in register Control_1) enables / disables the 1 Hz clock for the watch function. After power-up reset, the bit “WE” is automatically set = “1” and the 1 Hz clock is enabled. Setting “WE” = “0” stops the watch-function and the time circuits can be set and will not increment until the stop is released. Setting “WE” = “1” allows for accurate start of the time circuits triggered by an external event.

“WE” will not affect the clock outputs at CLKOUT.

4.8 SELF-RECOVERY SYSTEM

The purpose of the Self-Recovery System is to automatically generate an internal Reset in case the on-chip state machine goes into a deadlock. A possible source for such a deadlock could be disturbed electrical environment like EMC problem, disturbed power supply or any kind of communication issues on the I²C-Interface.

The function of the Self-Recovery System is based on internal counter that is periodically reset by the Control Logic. If the counter is not reset in time, a Self-Recovery Reset will be executed, at the latest after 2 thermometer scanning interval periods, i.e. 2 or 32 seconds.

The Self-Recovery System is enabled / disabled by “SROn” (bit 4 in register Control_), it is automatically enabled “SROn” = “1” after power-up by the register reset values, see section 4.2.2 Thermometer scanning interval is defined with “ThP” (bit 0 in register EEPROM_Control).

Generation of interrupts from the System Reset function is enabled via “SRIE” = “1” (bit 4 in register Control_INT). If “SRIE” is enabled, the INT pin #7 follows the condition of Flag “SRF” (bit 4 in register Control_INT Flag). To clear Interrupt signal (INT), both corresponding flags “SRF” (bit 4 in register Control_INT Flag) and “SR” (bit 4 in register Control_Status) need to be cleared by writing = “0”.

During Self-Recovery or System Reset, the internal logic is reset and registers are loaded with the Register Reset Values shown in section 4.2.2, Watch / Alarm and Timer information are not affected.

After Self-Recovery Reset, “SRF” is set = “1” (bit 4 in Register Control_INT Flag), indicating that an automatic Self-Recovery System Reset has been executed.

4.9 CLOCK OUTPUT CLKOUT

The internal reference frequency is generated by the oscillator-circuitry operating a 32.768 kHz “Tuning-Fork” Quartz Crystal.

A programmable square wave is available at pin #2 CLKOUT.

Frequencies of 32.768 kHz, 1024 Hz, 32 Hz or 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump or for test purposes.

The duty cycle of the selected clock is not controlled.

However, due to the nature of the clock generation, all frequencies will be 50:50 except the 32.768 kHz.

The frequency 32.768 kHz is clocked directly from the oscillator-circuitry, as a consequence of that, this frequency does not contain frequency compensation clock pulses. The frequencies 1024 / 32 / 1 Hz are clocked from the prescaler and contain frequency compensation clock pulses.

Operation is controlled by the bits “FD1” / “FD0” (bit 2 & 3 in the register EEPROM Control).

If “Clk/Int” is = “1” (bit 7 in register Control_1), pin #2 becomes a push-pull CLKOUT output and can be enabled / disabled with the pin #10 CLKOE. When disabled with CLKOE pin #10 = “low”, the CLKOUT output is pulled low.

Register EEPROM Control. FD0 / FD1 CLKOUT Frequency Selection (address 30Eh...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|------------|------------------|-----------------|-------|--|------------|-------|-------|
| 30h | EEPROM Control | R80k | R20k | R5k | R1k | FD1 | FD0 | ThE | 1 |
| Bit | 3 | 2 | CLKOUT Frequency | Typ. Duty Cycle | | Remarks | | | |
| | FD1 | FD0 | [Hz] | % | | | | | |
| 3 to 2 | 0 | 0 | 32768 | 40:60 to 60:40 | | Directly from 32.768kHz oscillator-circuitry, without frequency compensation | | | |
| | 0 | 1 | 1024 | 50:50 | | With frequency compensation | | | |
| | 1 | 0 | 32 | 50:50 | | With frequency compensation | | | |
| | 1 | 1 | 1 | 50:50 | | With frequency compensation | | | |

¹⁾ Duty cycle definition: % HIGH-level time : % LOW-level time

5.0 COMPENSATION OF FREQUENCY DEVIATION AND FREQUENCY DRIFT vs. TEMPERATURE

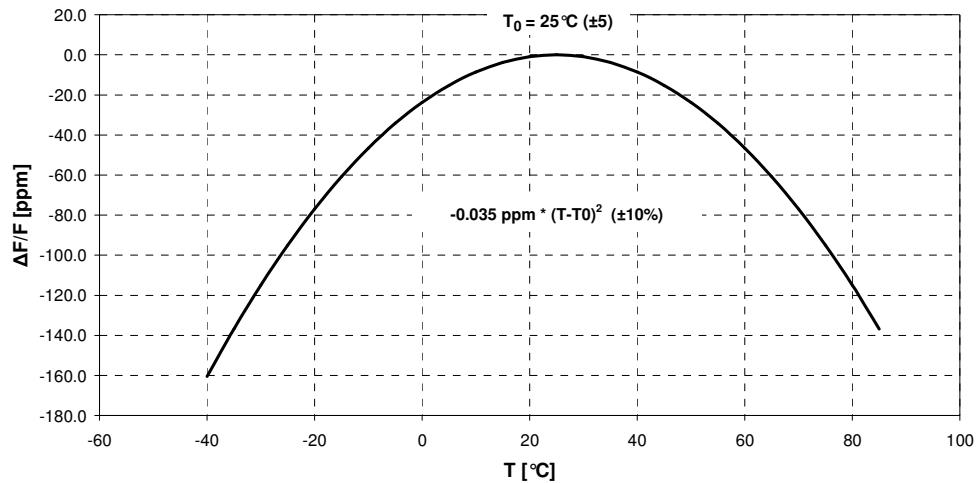
There is a Thermometer and a Frequency Compensation Unit "FCU" built-in the RV-3029-C2.

Based on all known tolerances and the measured ambient temperature, this Frequency Compensation Unit "FCU" is calculating a Frequency Compensation Value. The frequency compensation itself is achieved by adding or subtracting clock-pulses to the 32.768 kHz reference clock, one compensation period takes 32 seconds.

All required parameters for frequency compensation are factory calibrated and should not be modified to profit from best time accuracy.

Frequency deviations affecting the time accuracy of Real Time Clocks:

| | | |
|-------------------------|--|--|
| XTAL Offset: | Xtal's frequency deviation | $\pm 20\text{ppm}$ @ 25°C |
| XTAL T0: | Xtal's turnover temperature | 25°C $\pm 5^\circ\text{C}$ |
| XTAL temp. coefficient: | Xtal's frequency drift vs. temperature | $-0.035\text{ppm} * (T-T0)^2$ $\pm 10\%$ |

5.1 TEMPERATURE CHARACTERISTICS TUNING FORK CRYSTAL**Typical Frequency Deviation of a 32.768 kHz Tuning Fork Crystal over Temperature**

Above graph shows the typical frequency-deviation of a 32.768kHz "Tuning-Fork" Crystal over temperature. The parabolic curve is specified in terms of turnover temperature "T0" and the quadratic thermal coefficient " β "

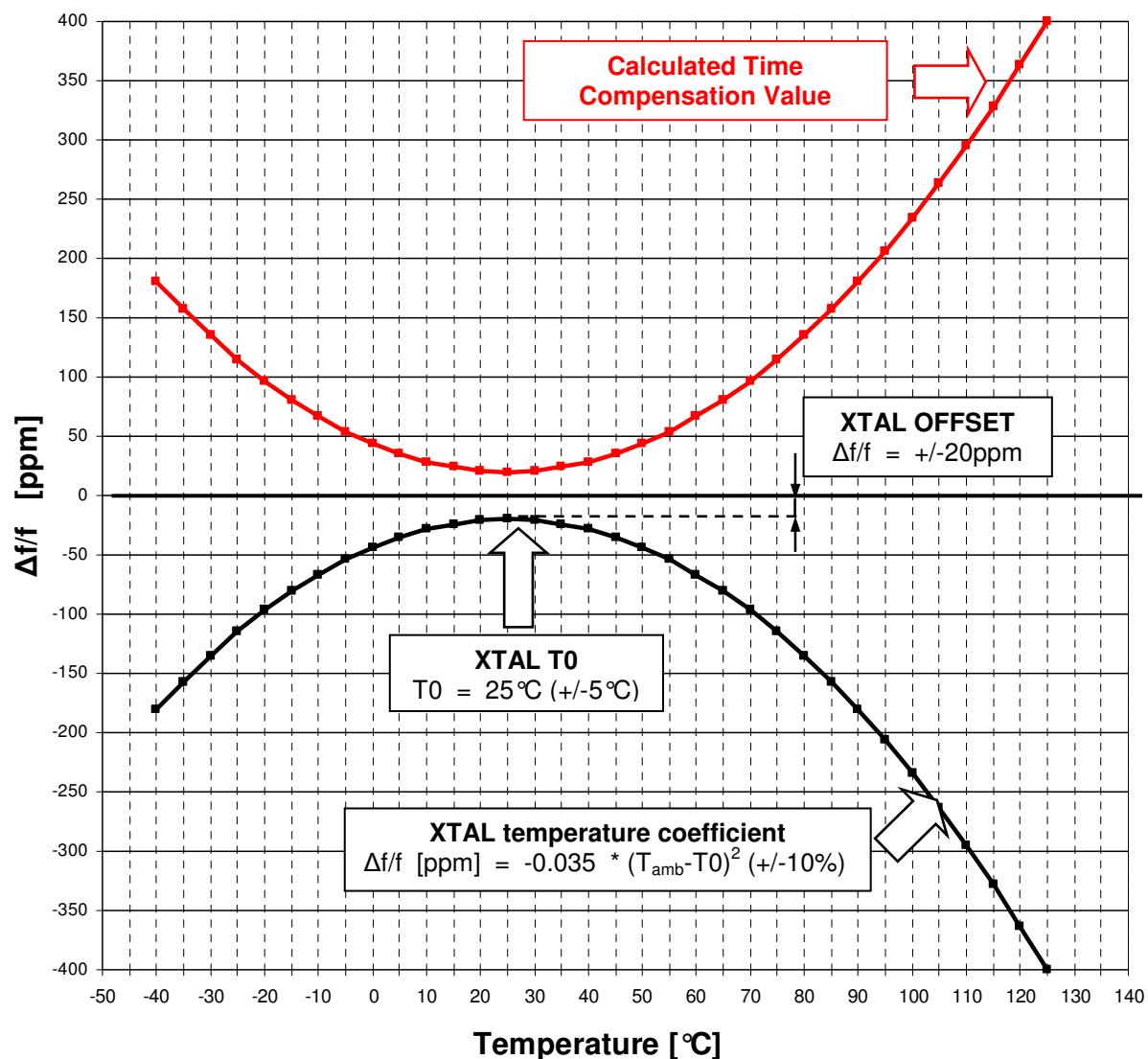
| | | | |
|---------|---|-------------------------------|--|
| T0 | Turnover Temperature | 25°C | $\pm 5^\circ\text{C}$ |
| β | 2 nd order temperature coefficient | $-0.035\text{ppm} * (T-T0)^2$ | $\pm 10\%$ (quadratic thermal coefficient) |

5.2 COMPENSATION PRINCIPLE

The Frequency Compensation Unit "FCU" is calculating a Frequency Compensation Value based on individual device data:

- XTAL Offset: Device individual frequency deviation @ 25 °C ± 20 ppm
- XTAL T0: Xtal's turnover temperature 25 °C ± 5 °C
- XTAL temp. coefficient: Xtal's frequency drift vs. temperature $-0.035\text{ppm} * (T-T0)^2$ $\pm 10\%$
- Temperature Measured ambient temperature

Calculating the anticipated Frequency Deviation and the Time Compensation Value



The 32.768 kHz frequency is adjusted according to the calculated Time Compensation value.

The compensation itself is achieved by adding or subtracting clock-pulses to the 32.768 kHz reference clock. One complete compensation period takes 32 seconds.

5.2.1 THERMOMETER AND TEMPERATURE VALUE

The function of the Thermometer is controlled by “ThP” and “ThE” (bit 0 & bit 1 in the register EEPROM Control).

Register EEPROM Control. Thermometer Control (address 30Eh...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------------|-------|---|-------|-------|-------|-------|-------|-------|
| 30h | EEPROM Control | R80k | R20k | R5k | R1k | FD1 | FD0 | ThE | ThP |
| Bit | Symbol | Value | Description | | | | | | |
| 1 | ThE | 0 | Disable Thermometer | | | | | | |
| | | 1 | Enable Thermometer | | | | | | |
| 0 | ThP | 0 | Thermometer scanning interval: 1 Second | | | | | | |
| | | 1 | Thermometer scanning interval: 16 Seconds | | | | | | |

The measured temperature value is stored in the register “Temperature” at address 20h.

The measured temperature is binary coded ranging from -60°C (=0d) to +190°C (=250d).

Example: Temperature of 0°C corresponding to a content of = 60d.

The thermometer has a resolution of 1°C per LSB; the typical accuracy is +/-4°C within the temperature-range -40°C to +125°C.

The Thermometer is automatically disabled if status bit “Vlow1” is set = “1”, the result of the last temperature measurement is frozen in register “Temperature” and the frequency compensation continues working with this last temperature reading.

The actual temperature value can be read from register “Temperature” at address 20h.

The Thermometer has to be disabled by ThE = “0” to externally write a temperature value into the register “Temperature” at address 20h.

Temperature Value (address 20h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 20h | Temperature | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| These bits hold the Temperature Value coded in binary format | | | | | | | | | |
| Temperature | Value hex | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| -60°C | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -59°C | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0°C | 3Ch | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 194°C | FEh | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 195°C | FFh | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

5.2.2 SETTING THE FREQUENCY COMPENSATION PARAMETERS

In order to achieve best time accuracy, correct parameters have to be stored into the corresponding registers of the EEPROM Control page.

Attention: These parameters are factory calibrated, it is recommended not to modify these register values.

XTAL Offset (address 31h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|----------|---|-------|-------|-------|-------|-------|-------|
| 31h | XTAL Offset | sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | | |
| 7 | sign | 0 | - deviation (slower) of 32.768kHz frequency at T0 | | | | | | |
| | | 1 | + deviation (faster) of 32.768kHz frequency at T0 | | | | | | |
| 6 to 0 | XTAL Offset | 0 to 121 | Frequency Offset Compensation value | | | | | | |

The register value "XTAL Offset" is used by the Frequency Compensation Unit "FCU" to compensate the initial frequency-deviation of the 32.768 kHz clock at the crystal's turnover temperature "XTAL T0".

The required register value "XTAL Offset" is calculated as follows:

$$\text{XTAL Offset} = \text{Xtal}_{\text{OFFSET}} \times 1.05$$

XTAL COEF Temperature Coefficient (address 32h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-----------|------------------------|---|-------|-------|-------|-------|-----------|-------|
| 32h | XTAL Coef | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | Reference | |
| 7 to 0 | XTAL Coef | ¹⁾ 0 to 255 | Quadratic Coefficient of XTAL's Temperature Drift | | | | | | |

¹⁾ The factory programmed register value XTAL Coef may also contain Thermometer Error compensation.

The register value "XTAL Coef" is used by the Frequency Compensation Unit "FCU" to compensate the frequency deviation caused by 2nd order temperature coefficient of the 32.768 kHz crystal. (frequency-drift vs. temperature)

The required register value XTAL Coef is calculated as follows:

$$\text{XTAL Coef} = \text{Xtal}_{\text{TEMPERATURE COEFFICIENT}} \times 4096 \times$$

XTAL T0 Turnover Temperature (address 33h...bits description)

| Address | Function | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|----------|-----------------------|------------------------------------|-------|-------|-------|-------|-----------|-------|
| 33h | XTAL T0 | x | x | 32 | 16 | 8 | 4 | 2 | 1 |
| Bit | Symbol | Value | Description | | | | | Reference | |
| 7 to 6 | x | - | unused | | | | | | |
| 5 to 0 | XTAL T0 | ¹⁾ 4 to 67 | XTAL's Turnover Temperature in °C. | | | | | | |

¹⁾ The factory programmed register value XTAL T0 may also contain Thermometer Error compensation.

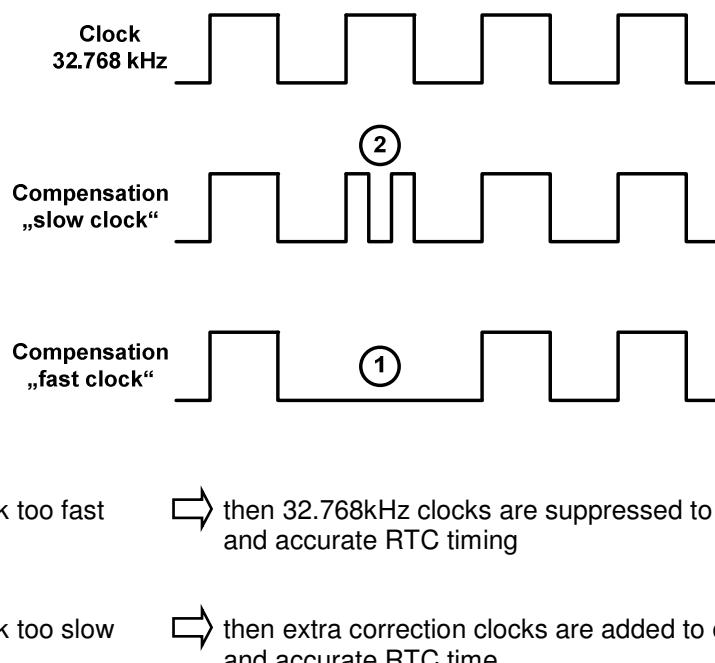
The register value "XTAL T0" is used by the Frequency Compensation Unit "FCU" to compensate the frequency deviation caused by the turnover temperature T0 of the 32.768 kHz crystal.

The required register value XTAL T0 is calculated as follows:

$$\text{XTAL T0} = \text{Xtal}_{\text{TURNOVER TEMP T0}} - 4$$

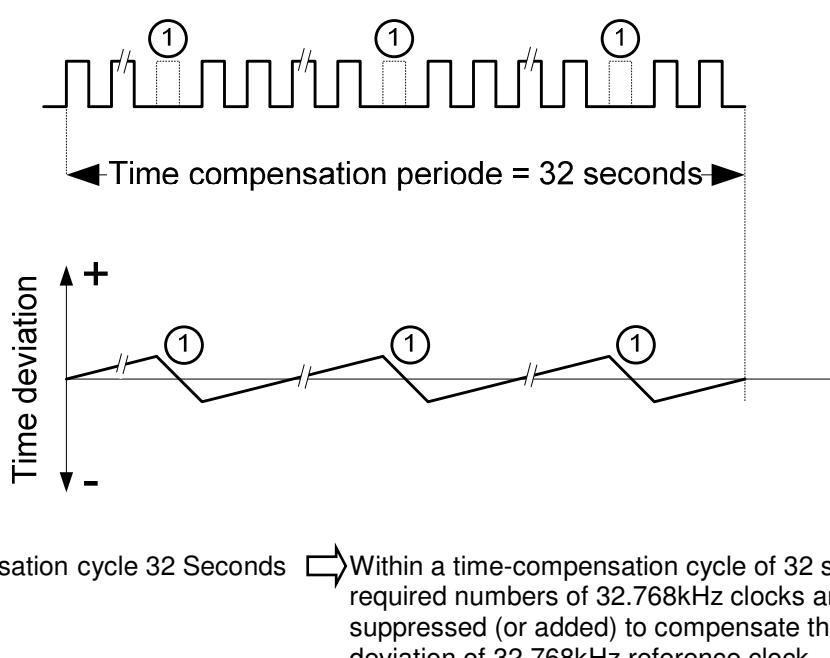
5.3 METHOD OF COMPENSATING THE FREQUENCY DEVIATION

The Frequency Compensation Unit (FCU) calculates the compensation factor needed to obtain accurate time information. The compensation is made by adding or subtracting correction-clocks to the 32.768kHz reference-frequency at the first stage of the frequency divider-chain, thereby changing the period of a single second. Extra clocks are added for to speed-up the timing, subtracting clocks to slow-down the timing.



Each compensation period takes 32 seconds.

Correction clocks are periodically applied during one complete compensation period. Within a compensation period of 32 seconds, one correction-clock will compensate the time-information by ± 1 ppm.



Effect of correction clocks:

- CLKOUT 32.768kHz not affect, this frequency is not compensated
- CLKOUT 1024 / 32 / 1 Hz affected, these frequencies are compensated
- Timer / INT Output affected; the internal Timer Source Clocks are compensated
- Time / Date affected, Time & date information are compensated

5.3.1 CORRECT METHOD FOR TESTING THE TIME ACCURACY

The compensation method of adding or subtracting correction-clocks is changing the period of a single second; therefore the duration of single seconds may vary within a compensation cycle of 32 seconds.

For a test result correctly representing the time-accuracy of the RTC module, it is mandatory to measure the device during one complete compensation cycle of 32 seconds.

When the device is tested over a shorter period of time, an error will be caused by the test method and shall be considered for interpretation of the test-results:

| Measuring Time | Resolution of Compensation Method | Test Error / Deviation per day |
|-----------------------|--|---------------------------------------|
| 1 Second | ± 1 clock (32.768 kHz) | ± 30.5 ppm / ± 2.7 sec. per day |
| 2 Seconds | ± 1 clock (32.768 kHz) | ± 15.3 ppm / ± 1.3 sec. per day |
| 4 Seconds | ± 1 clock (32.768 kHz) | ± 7.7 ppm / ± 0.7 sec. per day |
| 8 Seconds | ± 1 clock (32.768 kHz) | ± 3.9 ppm / ± 0.4 sec. per day |
| 32 Seconds | ± 1 clock (32.768 kHz) | represents real performance |

5.3.2 TESTING THE TIME ACCURACY USING CLKOUT OUTPUT

The simplest method to test the time accuracy of the Frequency Compensation Unit (FCU) is by measuring the compensated frequencies at the CLKOUT pin #2.

Enable Temperature compensation:

- Select scanning interval 1 s set “ThP” = “0” (bit 0 register EEPROM Control)
- Enable Thermometer set “ThE” = “1” (bit 1 register EEPROM Control)

Select compensated frequency at CLKOUT:

- Set CLKOUT frequency set “FD0” / “FD1” (bit 1&3 register EEPROM Control) to select CLKOUT frequency = 1024Hz or alternatively 1Hz.

Measuring equipment and setup:

- Use appropriate frequency counter for example: Agilent A53132A Universal Counter
- Correct setup set gate-time to 32 seconds (one complete compensation cycle) to measure frequency and calculate time deviation upon the measured frequency deviation.

5.3.3 TESTING THE TIME ACCURACY USING INTERRUPT OUTPUT 1 Hz

The internal Countdown Timer can be used to generate a 1 Hz test signal at the INT output. However, this procedure is more complicated then using CLKOUT, therefore the following instructions shall be read carefully to avoid mistakes.

Enable Temperature compensation:

- Select scanning interval 1 s
- Enable Thermometer

set "ThP" = "0" (bit 0 register EEPROM Control)
set "ThE" = "1" (bit 1 register EEPROM Control)

Set appropriate test condition using Countdown Timer & 1 Hz INT Output:

- Disable Timer
- Disable Timer Auto-Reload Mode

set "TE" = "0" (bit 1 register Control_1)
set "TAR" = "0" (bit 2 register Control_1)

Timer & Timer Auto Reload Mode needs to be disabled to allow changes in settings of the Timer Source Clock and Countdown Timer value.

- Set Timer Source Clock = 8 Hz
- Set Countdown Timer Value n = 7
- Enable Timer Interrupt
- Set Timer in Auto-Reload Mode
- Enable Timer

set "TD0" = "1" & "TD1" = "0" (bit 5&6 register Control_1)
set register "Timer Low" = 07h (bit 0-7 register Timer Low)
set register "Timer High" = 00h (bit 0-7 register Timer High)
set "TIE" = "1" (bit 1 register Control_INT)
set "TAR" = "1" (bit 2 register Control_1)
set "TE" = "1" (bit 1 register Control_1)

Prepare MCU Software Driver to clear INT signal

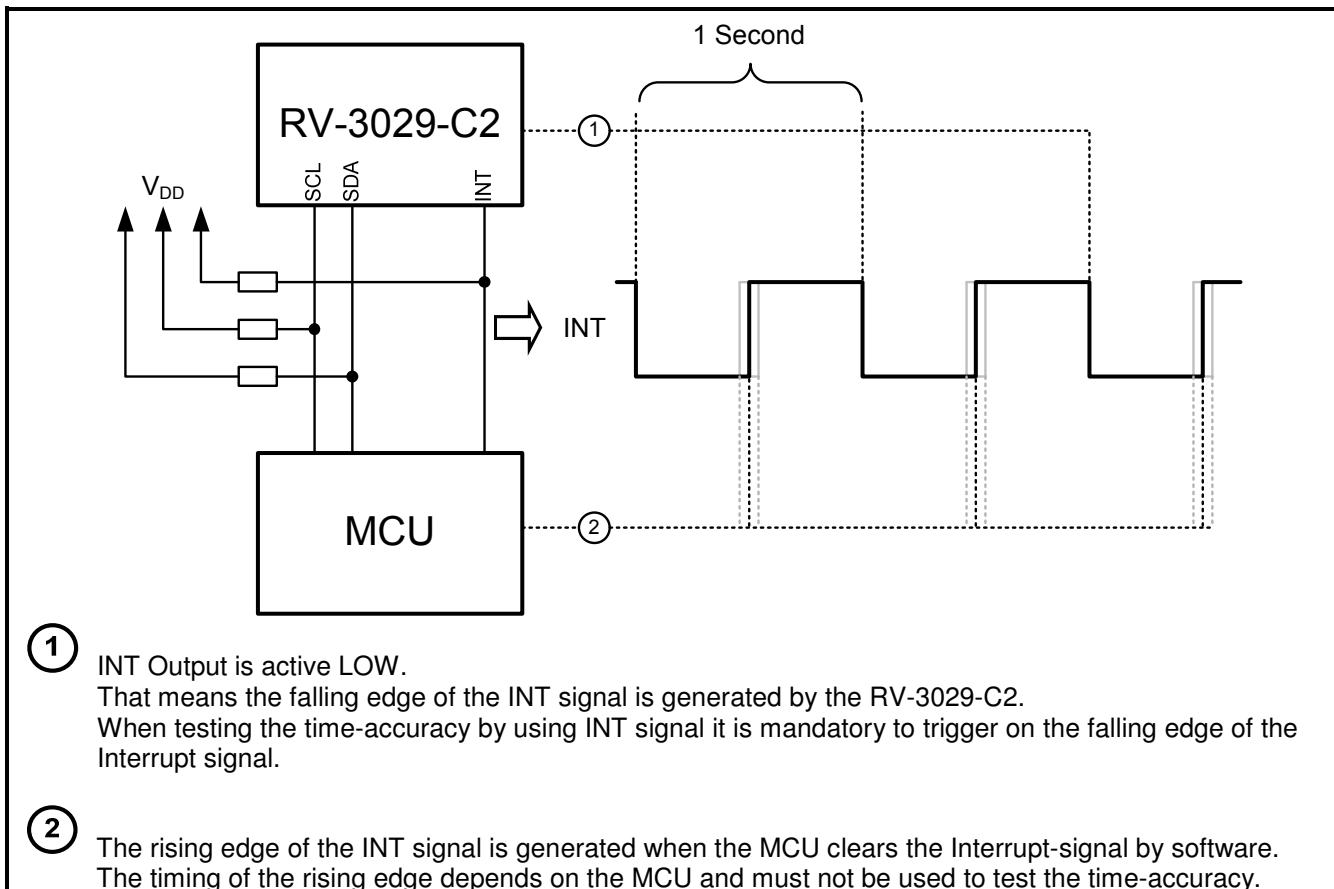
- MCU clears INT signal

clear INT by setting "TF" = "0" (bit 1 register Control_INT Flag)

Measuring equipment and setup:

- Use appropriate frequency counter
- Gate Time:
- Trigger to negative slope:

for example: Agilent A53132A Universal Counter
set gate-time to 32 seconds (one complete compensation cycle)
set Trigger to falling edge (negative slope)



5.4 TIME ACCURACY OPT: A / OPT: B

Option A: Parts individually calibrated over the Temperature range.

To obtain the best possible accuracy over the temperature-range, Option A parts are individually calibrated over the entire temperature range.

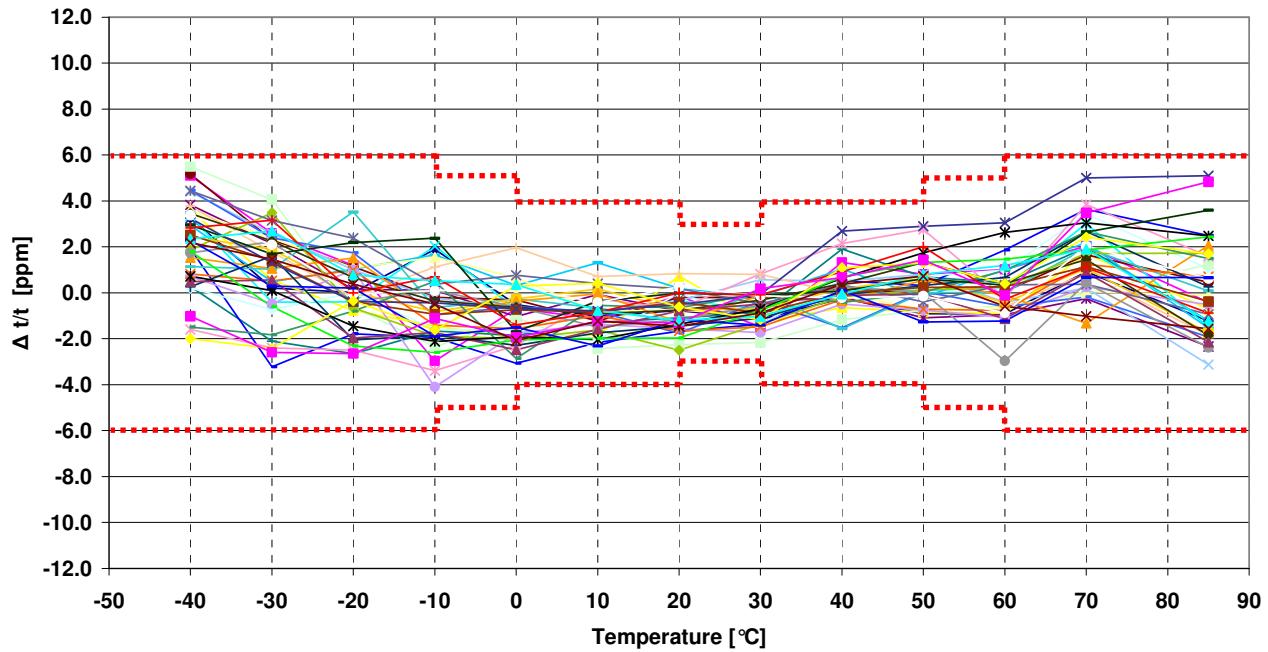
| | | |
|-------------------------|---------------------------------|--|
| XTAL Offset: | Frequency deviation @ 25 °C | Individually compensated |
| XTAL T0: | Turnover Temperature | Individually calibrated over temperature |
| XTAL temp. coefficient: | Frequency drift vs. temperature | Individually calibrated over temperature |
| Thermometer error: | Thermometer accuracy | Individually acquired over temperature, correction value individually embedded in XTAL parameters. |

Every part RV-3029-C2 Opt: A is individually measured over the temperature range to derive the Thermometer's and Crystal's characteristics over the temperature range in order to achieve optimized time-accuracy. Based on the temperature data, frequency correction values are calculated and individually programmed into the corresponding EEPROM-register by the factory.

Below chart shows the time deviation of 30 tested devices over the temperature-range of 30 individually calibrated RTC's (Opt: A) after the components were reflow-soldered onto a PCB, the red dotted line shows the specified time accuracy for Option: A devices.

| Option A: | Temperature Range | Time deviation |
|-----------|-------------------|---------------------------------|
| | 25 °C | ± 3 ppm = ±0.26 seconds per day |
| | 0 °C to + 50 °C | ± 4 ppm = ±0.35 seconds per day |
| | -10 °C to + 60 °C | ± 5 ppm = ±0.44 seconds per day |
| | -40 °C to + 85 °C | ± 6 ppm = ±0.52 seconds per day |
| | -40 °C to +125 °C | ± 8 ppm = ±0.70 seconds per day |

Option: A (calibrated)
Time Deviation vs. Temperature



Option B: Parts individually calibrated based on generic Temperature data.

The Option: B devices are designed for an optimized trade off accuracy vs. cost.

Option B parts are individually programmed to compensate the frequency-deviation at 25°C but using generic batch data to compensate the crystal's temperature-characteristics. Option B parts offer a good time-accuracy at little cost.

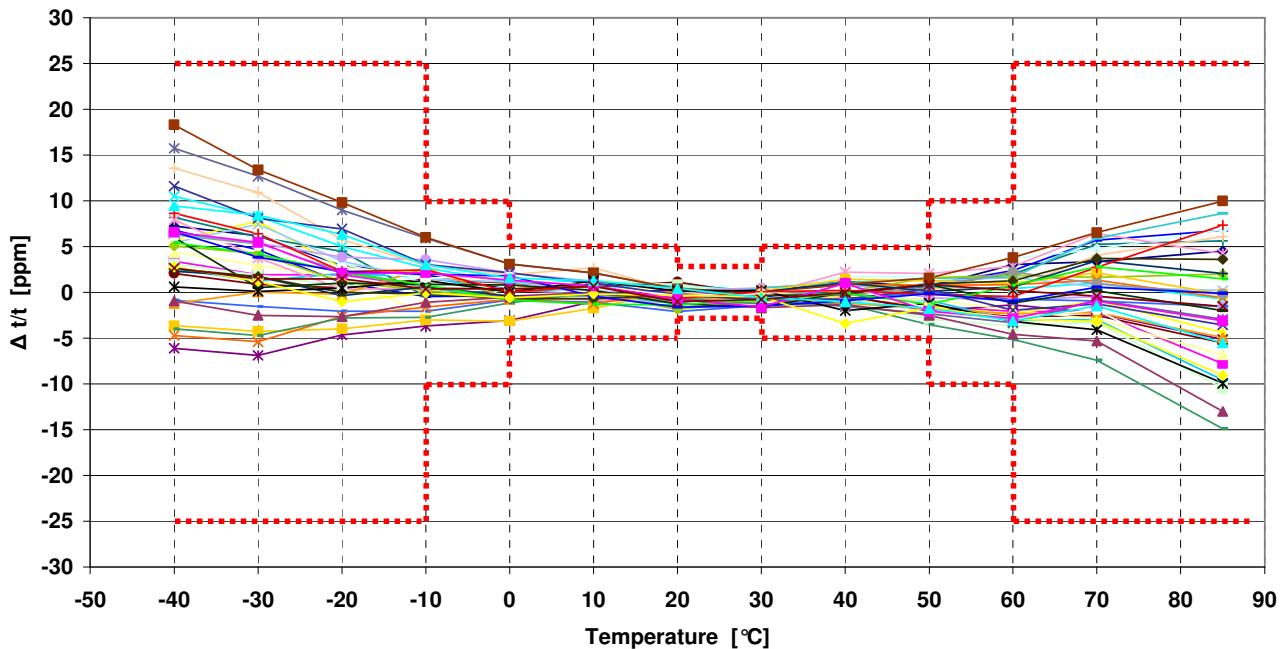
| | | |
|-------------------------|---------------------------------|---|
| XTAL Offset: | Frequency deviation @ 25°C | Individually compensated |
| XTAL T0: | Turnover Temperature | Compensated with generic batch data |
| XTAL temp. coefficient: | Frequency drift vs. temperature | Compensated with generic batch data |
| Thermometer error: | Thermometer accuracy | Individually acquired at 25°C, correction value individually embedded in XTAL parameters. |

Samples of RV-3029-C2 Opt: B parts are individually measured over the temperature range to derive the generic batch data for the Thermometer's and Crystal's characteristics over the temperature range. Based on the temperature data, frequency correction values are calculated and individually programmed into the corresponding EEPROM-register by the factory.

Below chart shows the time deviation of 30 tested devices over the temperature-range of individually calibrated RTC's (Opt: B) after the components were reflow-soldered onto a PCB, the red dotted line shows the specified time accuracy for Option: B devices.

| Option B: | <u>Temperature Rang</u> | <u>Time deviation</u> | |
|-----------|-------------------------|-----------------------|---------------------------------|
| | | 25°C | ± 3 ppm = ±0.26 seconds per day |
| | 0°C to + 50°C | ± 5 ppm | = ±0.44 seconds per day |
| | -10°C to + 60°C | ± 10 ppm | = ±0.87 seconds per day |
| | -40°C to + 85°C | ± 25 ppm | = ±2.17 seconds per day |
| | -40°C to +125°C | ± 30 ppm | = ±2.60 seconds per day |

**Option: B (default)
Time Deviation vs. Temperature**



6.0 I²C INTERFACE

The I²C-Interface is for bidirectional, two-line communication between different ICs or modules. The two lines are a **S**erial-**D**Atoline (SDA) and a **S**erial-**C**lockline (SCL).

6.1 I²C INTERFACE CHARACTERISTICS

SCL and SDA ports are open-drain architecture to allow connections of multiple devices. Both lines must be connected to a positive supply via pull-up resistors.

6.2 I²C INTERFACE SYSTEM CONFIGURATION

Since multiple devices can be connected with the I²C-bus, all I²C-bus devices have a fixed, unique device number built-in to allow individual addressing of each device.

Data transfer may be initiated only when the bus is not busy.

The device that controls the I²C-bus is the “Master”; the devices which are controlled by the master are the “Slaves”. A device generating a message is a “Transmitter”; a device receiving a message is the “Receiver”.

The communication is controlled by the Master. To start a transmission, the Master applies the “START condition” and generates the SCL clocks during the whole transmission.

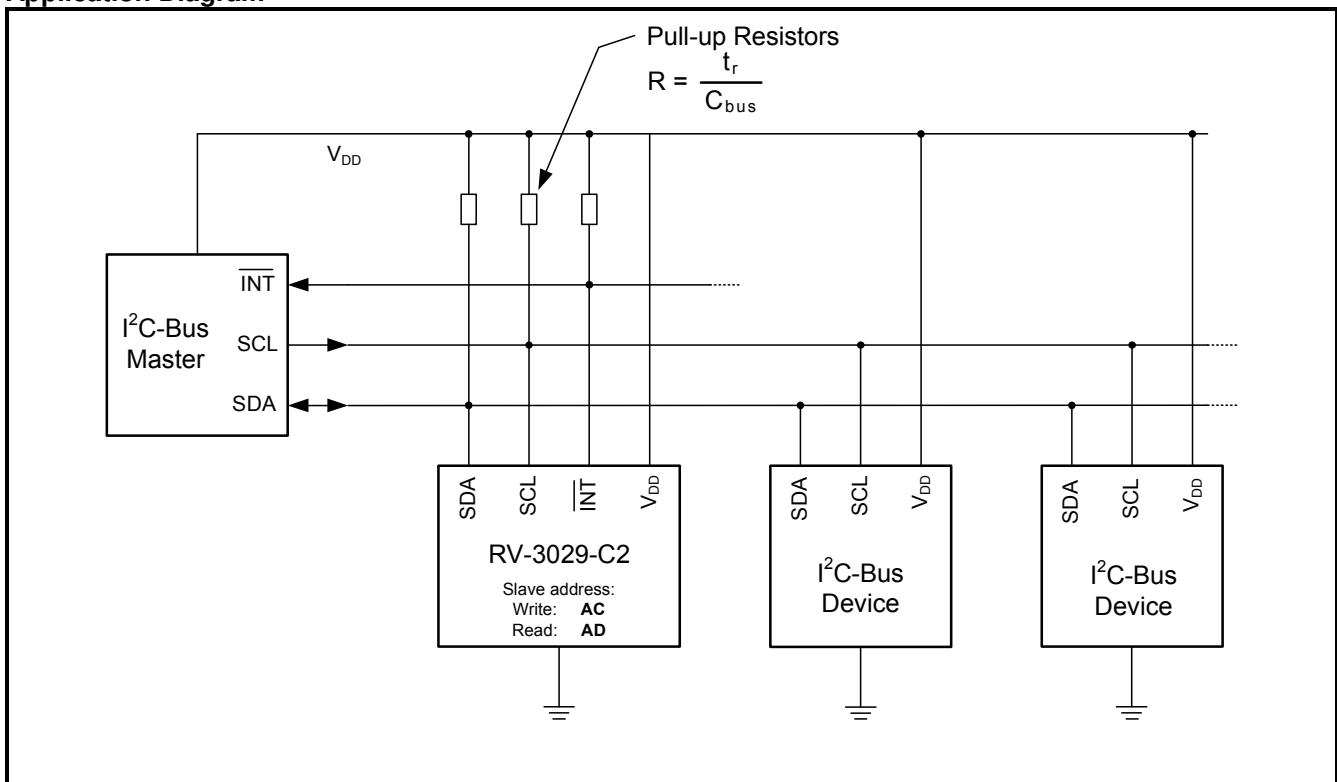
Before any data is transmitted on the I²C-bus, the device which should respond is addressed first.

The addressing is always carried out with the first byte transmitted after the “START condition”, most significant Bit MSB is sent first. The master terminates the transmission by sending the “STOP condition”.

The RV-3029-C2 acts as a Slave-Receiver or Slave-Transmitter.

Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

Application Diagram

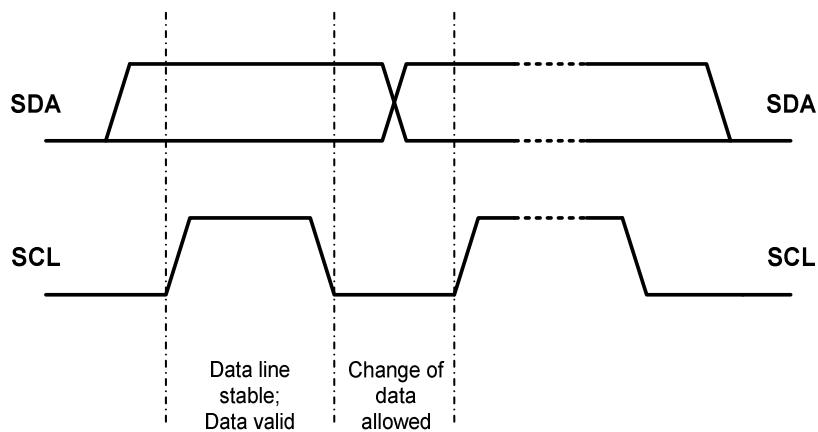


6.3 BIT TRANSFER

One Data Bit is transferred during each clock pulse.

The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals. Data change should be executed during the LOW period of the clock pulse.

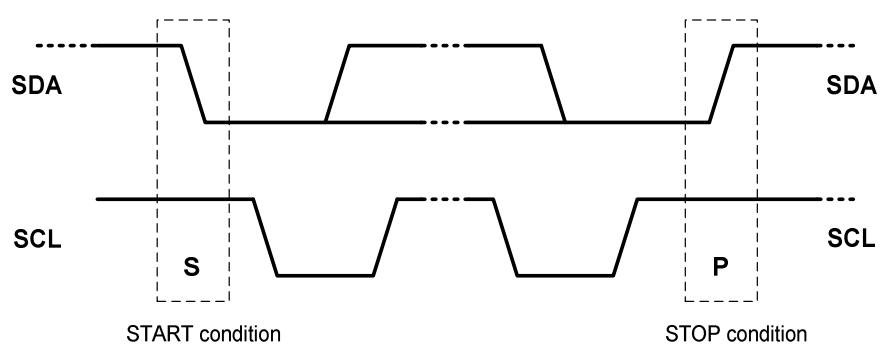
Bit Transfer



6.4 START AND STOP CONDITIONS

Any serial communication with the RV-3029-C2 starts with a “START condition” and terminates with the “STOP condition”.

Definition of START and STOP Condition



Both, SDA data and SCL clock-line remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The RV-3029-C2 does not allow a repeated START.

Therefore a STOP has to be released before the next START.

6.5 ACKNOWLEDGE

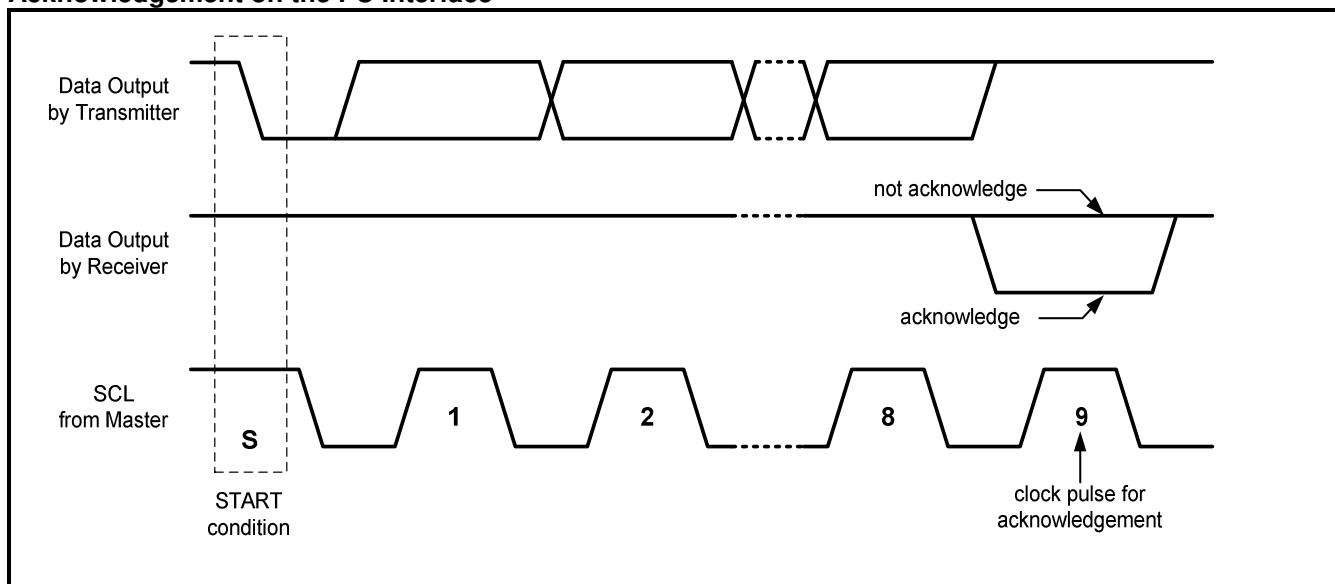
There is no limit to the numbers of data bytes transmitted between the start and stop conditions.

Each byte (of 8 bits) is followed by an acknowledge cycle.

Therefore, the Master generates an extra acknowledge-clock pulse. The acknowledge bit is a HIGH level signal put on the SDA line by the Transmitter-Device, the Receiver-Device must pull down the SDA line during the acknowledge-clock-pulse to confirm the correct reception of the last byte.

- A Slave-Receiver, which is addressed, must generate an acknowledge after the correct reception of each byte.
- Also a Master-Receiver must generate an acknowledge after correct reception of each byte that has been clocked-out of the Slave-Transmitter.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. (set-up and hold times must be taken into consideration).
- If the Master is addressed as Receiver, it can stop data transmission by **not** generating an acknowledge on the last byte that has been sent from the Slave Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.

Acknowledgement on the I²C Interface



6.6 I²C INTERFACE PROTOCOL

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START condition.

Any serial communication with the RV-3029-C2 starts with a “START condition” and terminates with the “STOP condition”.

When the “START condition” is detected, a copy of the content of the addressed Watch-, Alarm-, Timer- and Temperature-register is stored into a cache memory. During read / write operation, data are provided from this cache memory.

To prevent faulty reading, data in the cache memory are kept stable until the “STOP condition” terminates the Interface communication

When the “STOP condition” after a “Write transmission” terminates the Interface communication, the content of the modified registers in the cache memory are copied back into the corresponding Watch-, Alarm, Timer- and/or Temperature-registers.

6.7 I²C DEVICE ADDRESSES

The RV-3029-C2 is addressed with the first byte sent after the “START condition”
The first byte contains the 7 bit slave address and the R/W bit.

The following two slave addresses are reserved for the RV-3029-C2.

| | | | |
|--------|------------------|-----------------|------------|
| WRITE: | Slave address is | ACh, (R/W = 0) | (10101100) |
| READ: | Slave address is | ADh, (R/W = 1). | (10101101) |

RV-3029-C2 Slave Addresses

| | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|-------|--|-------|-------|-------|-------|-------|--|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---|---|---|---|---|---|---|--|
| Write | AC h | | | | | | | | | | | | | | | | | | | | | | | | | |
| Read | AD h | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | | C / D | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td> </tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td> </tr> </table> | | | | | | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| A C | | <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td> </tr> </table> | | | | | | | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Write | | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | |
| A D | | <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td> </tr> </table> | | | | | | | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | Read | | | | | | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | |

6.8 I²C INTERFACE READ AND WRITE DATA TRANSMISSION

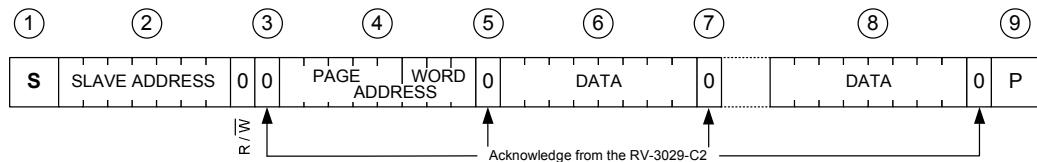
- Any serial communication with the RV-3029-C2 starts by initiating the “START condition”.
- The first byte sent contains the 8 bit address of RV-3029-C2, were the LSB is the R/W bit which defines if the device is addressed in READ or WRITE mode.

6.8.1 WRITE MODE DATA TRANSMISSION

- With the first byte, the Master has addressed the RV-3029-C2 in Write-Mode.
- The next byte contains the Page & Word-Address. The upper 5 bits address a specific “Memory Page”, the 3 lower bits are the auto-incrementing address part.
- The next byte contains the Data the Master sends to the addressed Page & Word-Address.
- After reading or writing one byte, the Word-Address is automatically incremented by 1 within the same Memory-Page. If “Acknowledge” is not received, no auto-increment of the address is executed and a following reading transmits data of the same address.

Example of Data Transmission in Write Mode

- 1) Master sends-out the “Start Condition”.
- 2) Master sends-out the “Slave Address”, ACh for the RV-3029-C2; the R/W bit = “0” for write mode.
- 3) Acknowledgement from the RV-3029-C2.
- 4) Master sends-out the “Page & Word Address” to the RV-3029-C2.
- 5) Acknowledgement from the RV-3029-C2.
- 6) Master sends-out the “Data” to write to the address specified in step 4).
- 7) Acknowledgement from the RV-3029-C2.
- 8) Steps 6) and 7) can be repeated if necessary. Within the same Memory Page, the RV-3029-C2 will increment the word-address automatically.
- 9) Master sends-out the “Stop Condition”.

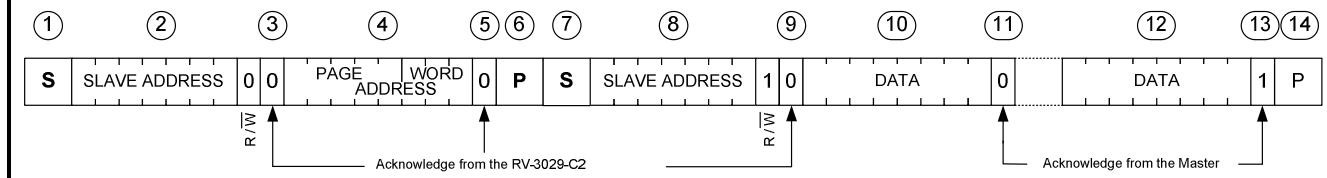


6.8.2 READ MODE DATA TRANSMISSION AT SPECIFIC ADDRESS

- With the first byte, the Master has addressed the RV-3029-C2 in Write-Mode.
- The next byte contains the Page & Word-Address. The upper 5 bits address a specific "Memory Page", the 3 lower bits are the auto-incrementing address part.
- The I²C Interface communication is halted by sending the "Stop Condition".
- Then the I²C Interface communication is re-established by sending the "Start Condition".
- With the next byte, the Master is addressing the RV-3029-C2 in Read-Mode.
- Then the Slave transmits the first byte starting from the previously addressed Page & Word address. Within the same Memory-Page, the Word-Address will be incremented automatically by 1. If "Acknowledge" is not received, no auto-increment of the address is executed and a following reading transmits data of the same address.

Example of Data Transmission in Read Mode after setting a specific Page & Word address

- Master sends-out the "Start Condition".
- Master sends-out the "Slave Address", ACh for the RV-3029-C2; the R/W bit = "0" for write mode.
- Acknowledgement from the RV-3029-C2.
- Master sends-out the "Page & Word Address" to the RV-3029-C2.
- Acknowledgement from the RV-3029-C2.
- Master sends-out the "Stop Condition".
- Master sends-out the "Start Condition".
- Master sends-out the "Slave Address", ADh for the RV-3029-C2; the R/W bit = "1" for read mode.
- Acknowledgement from the RV-3029-C2.
At this point, the Master becomes a Receiver, the Slave becomes the Transmitter.
- The RV-3029-C2 sends-out the "Data" from the "Page & Word Address" specified in step 4).
- Acknowledgement from the Master. At this time, the "Page & Word" Address will be automatically incremented by 1.
- Steps 10) and 11) can be repeated if necessary. Within the same Page-Address, the Word-Address will be incremented automatically
- The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
- Master sends-out the "Stop Condition".

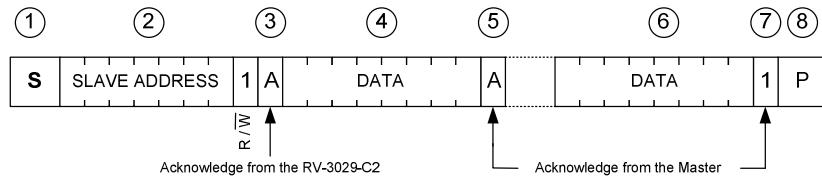


6.7.3 READ MODE

- With the first byte, the Master has addressed the RV-3029-C2 in Write-Mode.
- The Slave becomes the Transmitter and sends-out the Data from the last accessed Page / Word address incremented by 1.
- After reading a byte, within the same Memory-Page the Word-Address is automatically incremented by 1. If "Acknowledge" is not received, no auto-increment of the address is executed and a following reading transmits data of the same address.

Example of Reading Data at the last accessed Page & Word address incremented by 1.

- Master sends-out the "Start Condition".
- Master sends-out the "Slave Address", ADh for the RV-3029-C2; the R/W bit = "1" for read mode.
- Acknowledgement from the RV-3029-C2.
At this point, the Master becomes a Receiver, the Slave becomes the Transmitter
- The RV-3029-C2 sends-out the "Data" from the last accessed Page / Word Address incremented by 1.
- Acknowledgement from the Master.
- Steps 4) and 5) can be repeated if necessary. Within the same Page-Address, the Word-Address will be incremented by 1 automatically
- The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a stop condition.
- Master sends-out the "Stop Condition".



7.0 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System IEC 60134

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------------------------|---------------------|------------------------|--------------------------------|-------------------------|--------|
| Supply voltage | V_{DD} | > GND / < V_{DD} | GND -0.3 | +6.0 | V |
| Supply current | I_{DD} ; I_{SS} | V_{DD} Pin | -50 | +50 | mA |
| Input voltage | V_I | Input Pin | GND -0.3 | V_{DD} +0.3 | V |
| Output voltage | V_O | INT / CLKOUT | GND -0.5 | V_{DD} +0.5 | V |
| DC Input current | I_I | | -10 | +10 | mA |
| DC Output current | I_O | | -10 | +10 | mA |
| Total power dissipation | P_{TOT} | | | 300 | mW |
| Operating ambient temperature range | T_{OPR} | | -40 | +125 | °C |
| Storage temperature range | T_{STO} | stored as bare product | -55 | +125 | °C |
| Electro Static Discharge voltage | V_{ESD} | HBM MM | ¹⁾ ²⁾ | ± 2000 ± 300 | V V |
| Latch-up current | I_{LU} | ³⁾ | | 200 | mA |

¹⁾ HBM: Human Body Model, according to JESD22-A114.

²⁾ MM: Machine Model, according to JESD22-A115.

³⁾ Latch-up testing, according to JESD78.

Stresses above these listed maximum ratings may cause permanent damage to the device.
Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

7.2 FREQUENCY AND TIME CHARACTERISTICS

$V_{DD} = 3.0$ V; $V_{SS} = 0$ V; $T_{amb} = +25$ °C; $f_{OSC} = 32.768$ kHz

| PARAMETER | SYMBOL | CONDITIONS | TYP. | MAX. | UNIT |
|---|---------------------------|--|---|---------|---------|
| 32.768 kHz Oscillator Characteristics | | | | | |
| Frequency accuracy | $\Delta f / f$ | $F_{CLKOUT} = 32.7678$ kHz $T_{amb} = +25$ °C $V_{DD} = 3.0$ V | +/- 10 | +/- 20 | ppm |
| Frequency vs. voltage characteristics | $\Delta f / (f \Delta V)$ | $T_{amb} = +25$ °C $V_{DD} = 1.4$ V to 5.5 V | +/- 0.5 | +/- 1.0 | ppm / V |
| Frequency vs. temperature characteristics | $\Delta f / T_{OPR}$ | $T_{OPR} = -40$ °C to +125 °C $V_{DD} = 3.0$ V | $-0.035^{ppm/^\circ C} (T_{OPR} - T_O)^2$ (+/-10%) | | ppm |
| Turnover temperature | T_O | | +25 | 20 - 30 | °C |
| Aging first year max. | $\Delta f / f$ | $T_{amb} = +25$ °C | | +/- 3 | ppm |
| Oscillator start-up voltage | V_{Start} | $T_{amb} = +25$ °C $T_{Start} < 10$ s | 1.0 | | V |
| Oscillator start-up time | T_{Start} | $T_{amb} = -40$ °C to +85 °C $T_{amb} = -40$ °C to +125 °C | 0.5 1 | 3 3 | s |
| Frequency drift vs supply voltage | $\Delta f / (f \Delta V)$ | $V_{DD} = 1.4$ to 5.5V $T_{amb} = 25$ °C | 0.5 | 1 | ppm |
| CLKOUT duty cycle | | $F_{CLKOUT} = 32.7678$ kHz $T_{AMB} = +25$ °C | 50 | 40 / 60 | % |
| Time accuracy, DTCXO Digitally Temperature Compensated | | | | | |
| Time accuracy Opt: A | $\Delta t / t$ | $T_{amb} = +25$ °C | +/- 1 | +/- 3 | ppm |
| | | $T_{amb} = 0$ °C to +50 °C | +/- 2 | +/- 4 | |
| | | $T_{amb} = -10$ °C to +65 °C | +/- 3 | +/- 5 | |
| | | $T_{amb} = -40$ °C to +85 °C | +/- 4 | +/- 6 | |
| | | $T_{amb} = -40$ °C to +125 °C | +/- 5 | +/- 8 | |
| Time accuracy Opt: B | $\Delta t / t$ | $T_{amb} = +25$ °C | +/- 1 | +/- 3 | ppm |
| | | $T_{amb} = 0$ °C to +50 °C | +/- 3 | +/- 5 | |
| | | $T_{amb} = -10$ °C to +65 °C | +/- 5 | +/- 10 | |
| | | $T_{amb} = -40$ °C to +85 °C | +/- 10 | +/- 25 | |
| | | $T_{amb} = -40$ °C to +125 °C | +/- 15 | +/- 30 | |

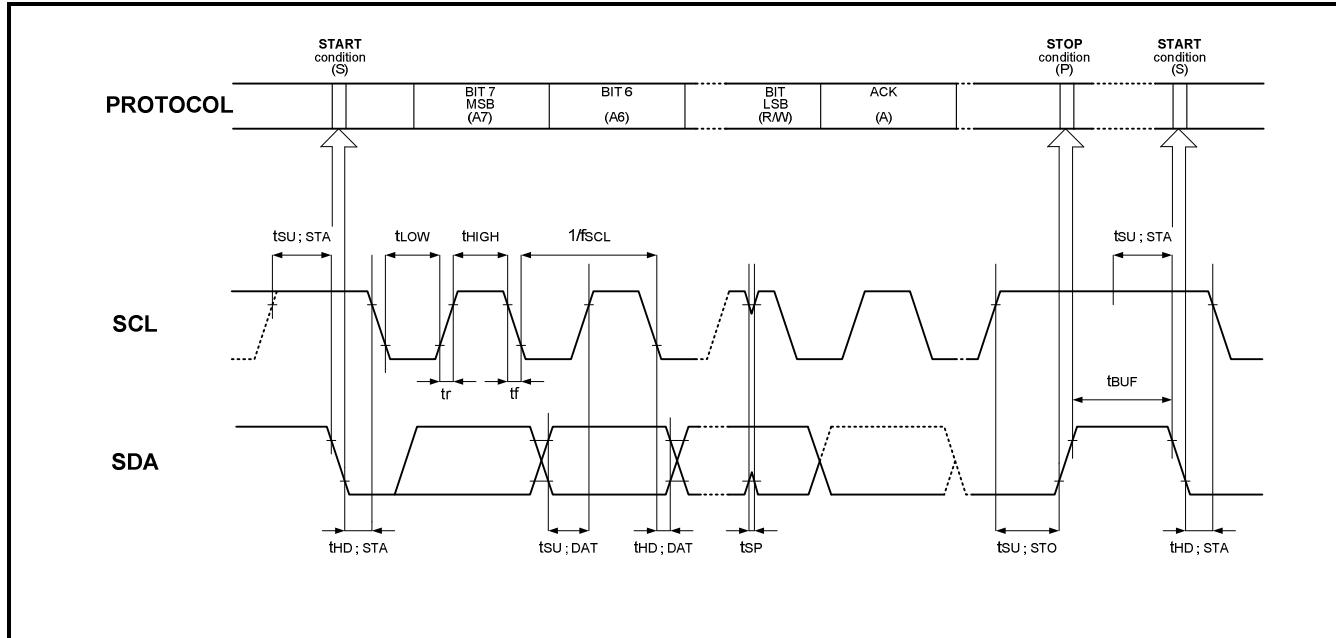
7.3 STATIC CHARACTERISTICS

 $V_{DD} = 1.4 \text{ V to } 5.5 \text{ V}; V_{SS} = 0 \text{ V}; T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}; f_{OSC} = 32.768 \text{ kHz}$

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|---|------------------------|------|------|---------------|
| Supplies | | | | | | |
| Supply voltage | V_{DD} | time-keeping mode $I^2\text{C}$ bus reduced speed | 1.4 | | 5.5 | V |
| | | $I^2\text{C}$ bus full speed | 2.1 | | 5.5 | V |
| Minimum supply voltage detection | V_{LOW1} | $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | 1.8 | | 2.1 | V |
| Minimum supply voltage detection | V_{LOW2} | $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | 1.0 | | 1.4 | V |
| Main Supply to Backup Supply Switchover Hysteresis | V_{HYST} | $V_{DD} \text{ to } V_{BACK} = 3.0 \text{ V}$ | | 20 | | mV |
| Supply current $I^2\text{C}$ bus inactive CLKOUT disabled $V_{BACK} = 0 \text{ V}$ or $V_{DD} = 0 \text{ V}$ | I_{DD} ($V_{BACK} = 0 \text{ V}$) | $V_{DD} = 1.4 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | 0.6 | 1.5 | μA |
| | | $V_{DD} = 1.4 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 4.6 | μA |
| | | $V_{DD} = 3.3 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | 0.8 | 2.0 | μA |
| | I_{BACK} ($V_{DD} = 0 \text{ V}$) | $V_{DD} = 3.3 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 5.2 | μA |
| | | $V_{DD} = 5.0 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | 0.9 | 2.2 | μA |
| | | $V_{DD} = 5.0 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 5.5 | μA |
| | | $SCL = 100 \text{ kHz}$ $V_{DD} = 1.4 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | | 12 | μA |
| Supply current $I^2\text{C}$ bus active CLKOUT disabled | I_{DD} | $SCL = 100 \text{ kHz}$ $V_{DD} = 1.4 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 15 | μA |
| | | $SCL = 400 \text{ kHz}$ $V_{DD} = 3.3 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | | 35 | μA |
| | | $SCL = 400 \text{ kHz}$ $V_{DD} = 3.3 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 40 | μA |
| | | $SCL = 400 \text{ kHz}$ $V_{DD} = 5.0 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | | | 50 | μA |
| | | $SCL = 400 \text{ kHz}$ $V_{DD} = 5.0 \text{ V}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 60 | μA |
| | | $V_{DD} = 5.0 \text{ V}$ | | 2.5 | 3.4 | μA |
| | | $V_{DD} = 3.3 \text{ V}$ | | 1.5 | 2.2 | μA |
| | | $V_{DD} = 1.4 \text{ V}$ | | 1.1 | 1.6 | μA |
| Inputs | | | | | | |
| LOW level input voltage | V_{IL} | $V_{DD} = 1.4 \text{ V to } 5.0 \text{ V}$ Pins: SCL, SDA, CLKOE | | | 20% | V_{DD} |
| HIGH level input voltage | V_{IH} | | $80\% \text{ } V_{DD}$ | | | V |
| Input leakage current $V_{SS} > V_I < V_{DD}$ | I_L | $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | -1 | | +1 | μA |
| | | $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | -1.5 | | +1.5 | μA |
| Input capacitance | C_I | | ³⁾ | | 7 | pF |
| Outputs | | | | | | |
| HIGH level output voltage | V_{OH} | $V_{DD} = 1.4 \text{ V}; I_{OH} = 0.1 \text{ mA}$ | 1.0 | | | V |
| | | $V_{DD} = 3.3 \text{ V}; I_{OH} = 1.5 \text{ mA}$ | 2.7 | | | |
| | | $V_{DD} = 5.0 \text{ V}; I_{OH} = 2.0 \text{ mA}$ | 4.5 | | | |
| LOW level output voltage | V_{OL} | $V_{DD} = 1.4 \text{ V}; I_{OL} = 0.4 \text{ mA}$ | | | 0.2 | V |
| | | $V_{DD} = 3.3 \text{ V}; I_{OL} = 1.5 \text{ mA}$ | | | 0.25 | |
| | | $V_{DD} = 5.0 \text{ V}; I_{OL} = 5.0 \text{ mA}$ | | | 0.8 | |
| HIGH level output current | I_{OH} | $V_{OH} = 4.5 \text{ V} / V_{DD} = 5 \text{ V}$ | | | 1.5 | mA |
| LOW level output current | I_{OL} | $V_{OL} = 0.8 \text{ V} / V_{DD} = 5 \text{ V}$ | | | -5.0 | mA |
| Output leakage current | I_{LO} | $V_O = V_{DD} \text{ or } V_{SS}$ $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ | -1 | 0 | +1 | μA |
| | | $V_O = V_{DD} \text{ or } V_{SS}$ $T_{amb} = -40^\circ\text{C to } +125^\circ\text{C}$ | -1.5 | 0 | +1.5 | |
| Operating Temperature Range | | | | | | |
| Operating temperature range | T_{OPR} | | -40 | | +125 | °C |

7.3 STATIC CHARACTERISTICS...(continue)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|-------------------|--|------|--|------|------------|
| EEPROM Characteristics | | | | | | |
| Read voltage | V_{Read} | $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | 1.4 | | | V |
| Programming voltage | V_{Prog} | $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | 2.2 | | | V |
| EEPROM Programming Time | T_{Prog} | $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | | | 30 | ms |
| EEPROM write / erase cycles | V_{HYST} | V_{DD} to $V_{\text{BACK}} = 3.0\text{ V}$ | 5000 | | | Cycles |
| Trickle charger | | | | | | |
| Current limiting resistors $V_{\text{DD}} = 5.0\text{V}$ $V_{\text{BACK}} = 3.0\text{V}$ | R80k | $T_{\text{amb}} = 25^{\circ}\text{C}$ | | 80 | | k Ω |
| | R20k | $T_{\text{amb}} = 25^{\circ}\text{C}$ | | 20 | | |
| | R5k | $T_{\text{amb}} = 25^{\circ}\text{C}$ | | 5 | | |
| | R1.5k | $T_{\text{amb}} = 25^{\circ}\text{C}$ | | 1.5 | | |
| Thermometer | | | | | | |
| Thermometer precision | T_E | $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | | +/-4 | | °C |
| | | $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | | +/-6 | | |

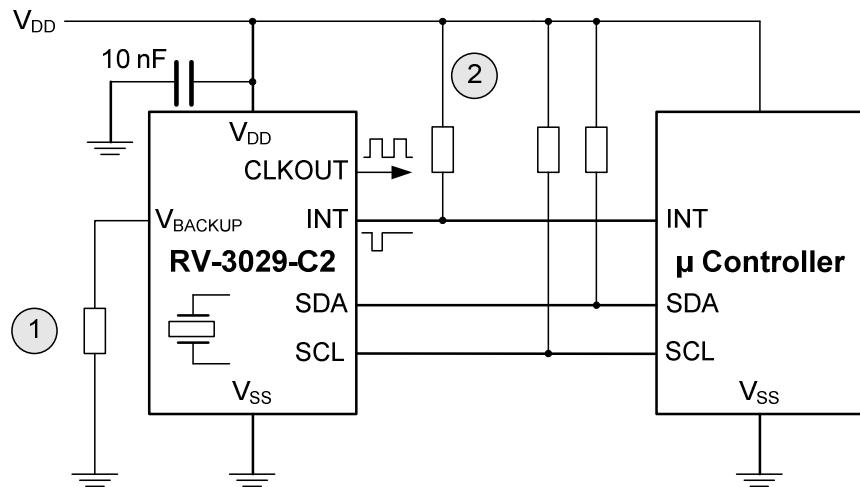
7.4 I²C INTERFACE TIMING CHARACTERISTICS

7.4 I²C INTERFACE TIMING CHARACTERISTICS...(continue)

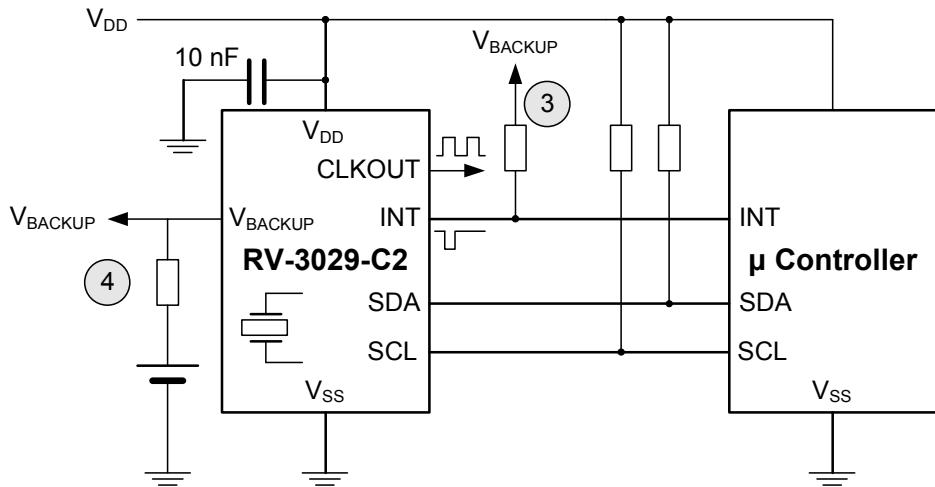
$V_{SS} = 0\text{ V}$; $T_{amb} = -40^\circ\text{C}$ to $+125^\circ\text{C}$. All timing values are valid within the operating supply voltage range and references to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD} .

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNIT |
|--|-----------------------|---------------------------|------|------|------|
| SCL Clock Frequency | f _{SCL} | $V_{DD} \geq 1.4\text{V}$ | | 100 | kHz |
| | | $V_{DD} \geq 1.8\text{V}$ | | 300 | |
| | | $V_{DD} \geq 3.0\text{V}$ | | 400 | |
| Start Condition Set-up Time | t _{SU} ; STA | $V_{DD} \geq 1.4\text{V}$ | 50 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | 30 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 20 | | |
| Start Condition Hold Time | t _{HD} ; STA | $V_{DD} \geq 1.4\text{V}$ | 0.2 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | | | |
| | | $V_{DD} \geq 3.0\text{V}$ | | | |
| Data Set-up Time | t _{SU} ; DAT | $V_{DD} \geq 1.4\text{V}$ | 100 | | ns |
| | | $V_{DD} \geq 1.8\text{V}$ | 80 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 50 | | |
| Data Hold Time | t _{HD} ; DAT | $V_{DD} \geq 1.4\text{V}$ | 50 | | ns |
| | | $V_{DD} \geq 1.8\text{V}$ | 30 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 20 | | |
| Data Valid Time | t _{VD} ; DAT | $V_{DD} \geq 1.4\text{V}$ | 4.0 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | 1.5 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 1.2 | | |
| Data Valid Acknowledge Time | t _{VD} ; ACK | $V_{DD} \geq 1.4\text{V}$ | 3.5 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | 1.1 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 0.9 | | |
| Stop Condition Set-up Time | t _{SU} ; STO | $V_{DD} \geq 1.4\text{V}$ | 50 | | ns |
| | | $V_{DD} \geq 1.8\text{V}$ | 30 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 20 | | |
| Bus Free Time between STOP and START condition | t _{BUF} | $V_{DD} \geq 1.4\text{V}$ | 1.0 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | 0.5 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 0.4 | | |
| SCL "LOW time" | t _{LOW} | $V_{DD} \geq 1.4\text{V}$ | 4.5 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | 1.7 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 1.3 | | |
| SCL "HIGH time" | t _{HIGH} | $V_{DD} \geq 1.4\text{V}$ | 0.6 | | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | 0.5 | | |
| | | $V_{DD} \geq 3.0\text{V}$ | 0.4 | | |
| SCL and SDA Rise Time | tr | $V_{DD} \geq 1.4\text{V}$ | | 1.0 | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | | 0.3 | |
| | | $V_{DD} \geq 3.0\text{V}$ | | 0.2 | |
| SCL and SDA Fall Time | tf | $V_{DD} \geq 1.4\text{V}$ | | 0.4 | μs |
| | | $V_{DD} \geq 1.8\text{V}$ | | 0.3 | |
| | | $V_{DD} \geq 3.0\text{V}$ | | 0.2 | |
| Tolerance Spike Time on Bus | t _{SP} | | | 50 | ns |
| SCL and SDA I/O Capacitance | C _{I/O} | | | 10 | pF |
| Capacitive Load Bus Lines | C _B | | | 200 | pF |

8.0 APPLICATION INFORMATION

Operating RV-3029-C2 without V_{BACKUP} Supply:

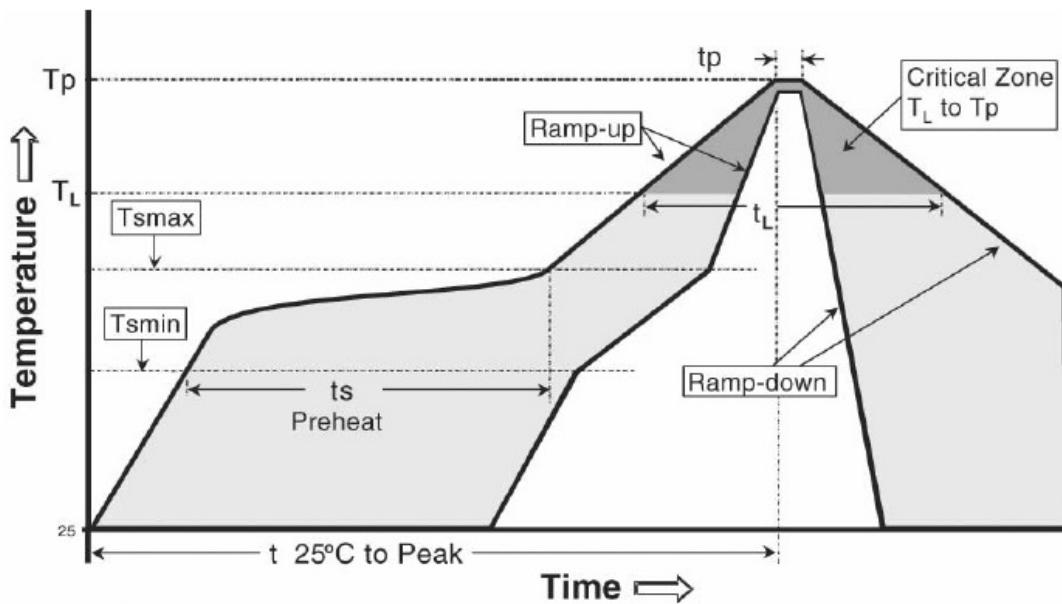
- ① When operating the RV-3029-C2 without Backup Supply Voltage, it is recommended to tie V_{BACKUP} pin #8 to GND, 10kOhm resistor is recommended.
- ② Pull-up resistor of the INT signal pin #7 can be tied directly to supply voltage V_{DD}.

Operating RV-3029-C2 with Backup Supply Voltage V_{BACKUP}:

- ③ When operating the RV-3029-C2 with either Supercap or Lithium Battery as Backup Supply, the INT signal on pin #7 also works when the device operates on V_{BACKUP} supply voltage, therefore it is recommended to tie the INT pull-up resistor to V_{BACKUP}.
- ④ When a Lithium Battery is used, it is recommended to insert a protection resistor of 100 – 1'000 Ω to limit battery current and to prevent damage in case of soldering issues causing short between supply pins.

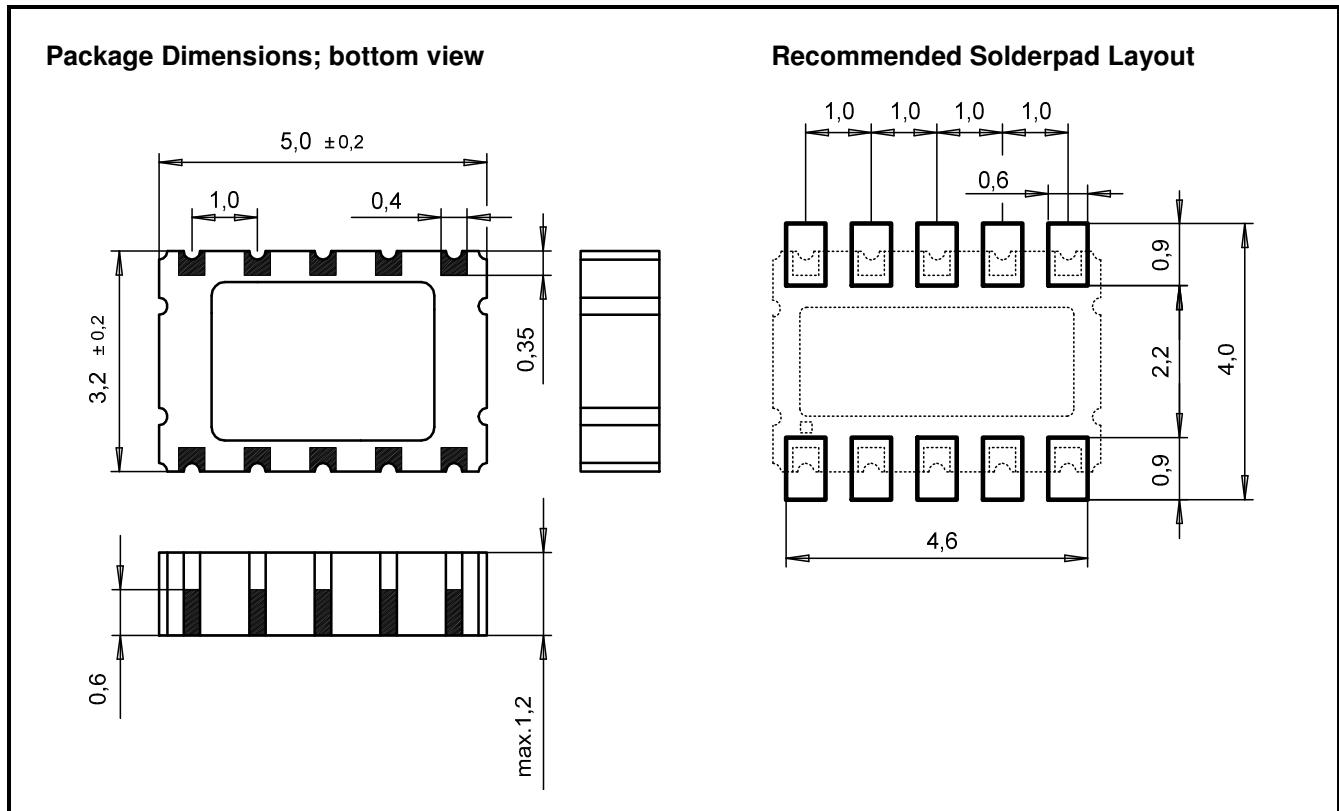
8.1 RECOMMENDED REFLOW TEMPERATURE (for "lead-free" soldering)

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"

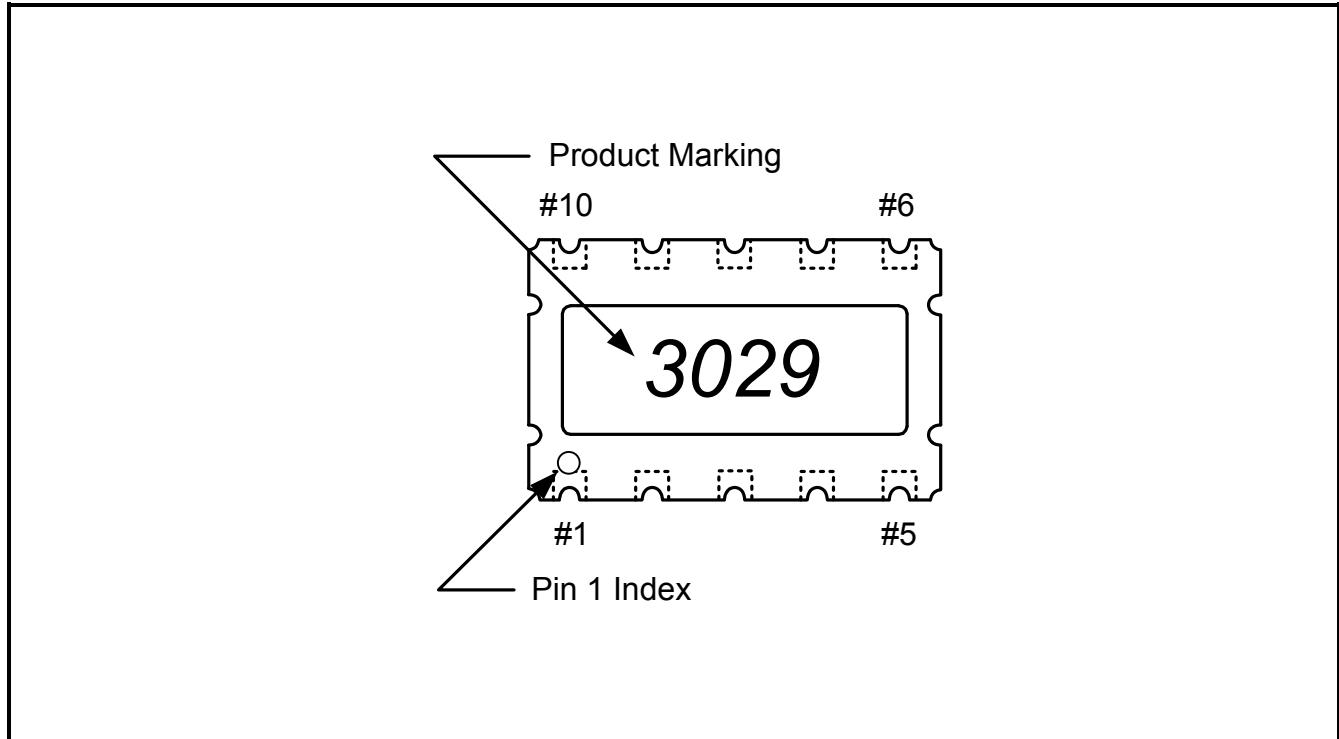


| Temperature Profile | Symbol | Condition | Unit |
|---|--|-------------------|--------|
| Average ramp-up rate | (T _{smax} to T _p) | 3 °C / second max | °C / s |
| Ramp down Rate | T _{cool} | 6 °C / second max | °C / s |
| Time 25 °C to Peak Temperature | T _{to-peak} | 8 minutes max | m |
| Preheat | | | |
| Temperature min | T _{smin} | 150 | °C |
| Temperature max | T _{smax} | 200 | °C |
| Time T _{smin} to T _{smax} | t _s | 60 - 180 | Sec |
| Soldering above liquidus | | | |
| Temperature liquidus | T _L | 217 | °C |
| Time above liquidus | t _L | 60 – 150 | sec |
| Peak temperature | | | |
| Peak Temperature | T _p | 260 | °C |
| Time within 5 °C of peak temperature | t _p | 20 - 40 | sec |

9.0 PACKAGE DIMENSIONS AND SOLDERPAD LAYOUT



9.1 PACKAGE MARKING AND PIN #1 INDEX



10.0 PACKING INFO CARRIER TAPE

12 mm Carrier-Tape:

Material:

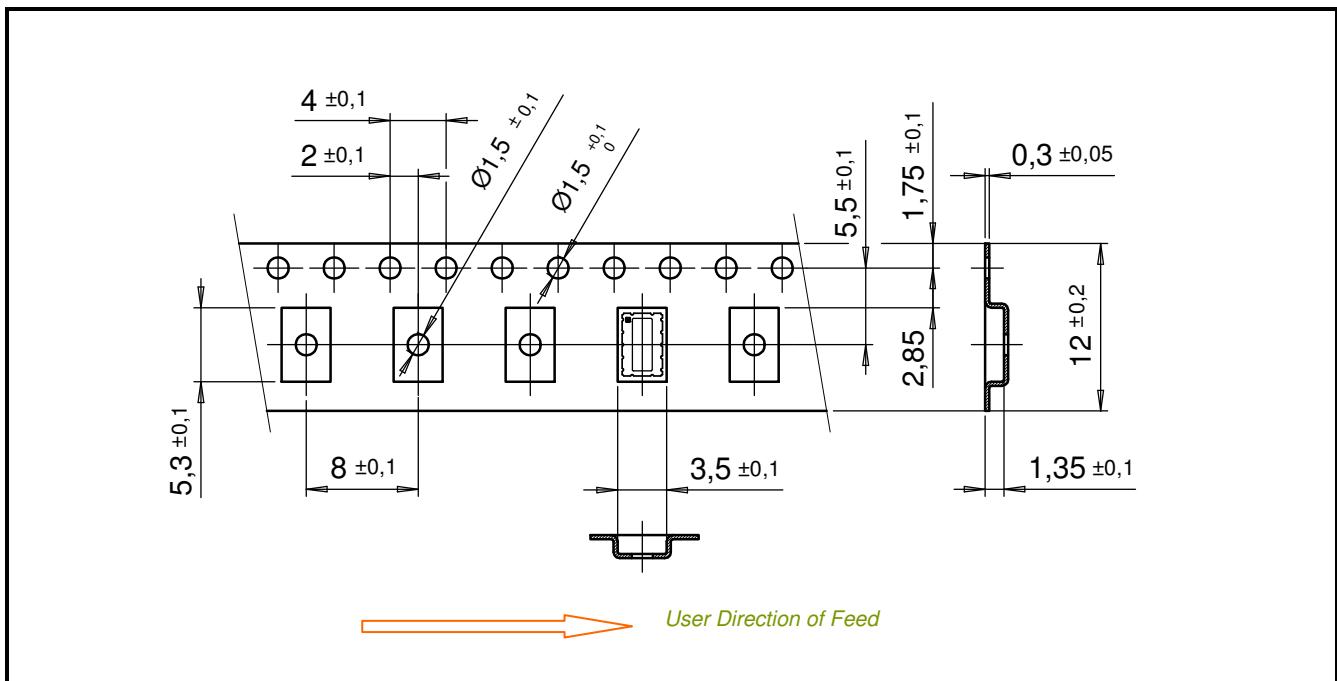
Polystyrene / Butadine or
Polystyrol black, conductive**Cover Tape:**

Base Material:

Polyester, conductive 0.061 mm

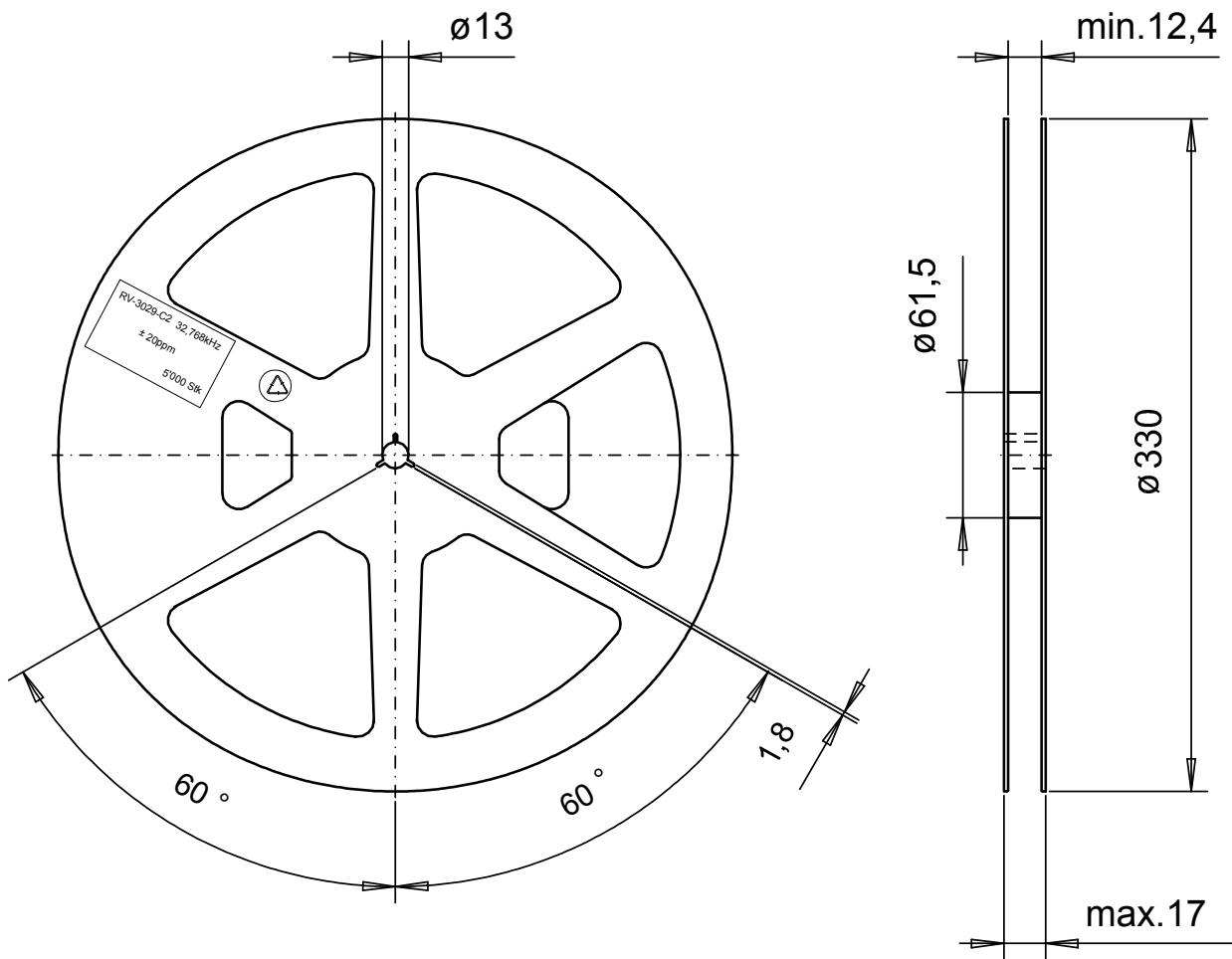
Adhesive Material:

Pressure-sensitive Synthetic Polymer



Tape Leader and Trailer: 300 mm minimum All dimensions are in mm

| REELS: | DIAMETER | MATERIAL. | RTC's per REEL. |
|--------|----------|----------------------|-----------------|
| | 7" | Plastic, Polystyrene | 1000 |
| | 13" | Plastic, Polystyrol | 5000 |

10.1 REEL 13 INCH FOR 12 mm TAPE**Reel:**

| <i>Diameter</i> | <i>Material</i> |
|-----------------|----------------------------|
| 13" | <i>Plastic, Polystyrol</i> |

11.0 HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration

Keep the crystal from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal will bear a mechanical shock of 5000g / 0.3 ms.

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic Cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damage crystals due to mechanical resonance of the crystal blank.

Overheating, rework high-temperature-exposure

Avoid overheating the package. The package is sealed with a sealring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280 °C. Heating the sealring up to >280 °C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300 °C.

Use the following methods for re-work:

- Use a hot-air- gun set at 270 °C
- Use 2 temperature-controlled soldering irons, set at 270 °C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

12.0 DOCUMENT REVISION HISTORY

| Date | Revision # | Revision Details |
|------------|------------|------------------|
| April 2010 | 1.2 | First release |

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