

BATTERY PROTECTION IC FOR 2-SERIAL / 3-SERIAL CELL PACK (SECONDARY PROTECTION)

www.sii-ic.com

© SII Semiconductor Corporation, 2012-2017

Rev.1.4_00

The S-8213 Series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short-circuits between VC3 to VSS accommodate serial connection of two cells or three cells.

■ Features

- High-accuracy voltage detection circuit for each cell
 - Overcharge detection voltage n (n = 1 to 3)
 - 4.100 V to 4.500 V (in 50 mV steps)
 - Accuracy: ± 25 mV ($T_a = +25^\circ\text{C}$)
 - Accuracy: ± 30 mV ($T_a = 0^\circ\text{C}$ to $+60^\circ\text{C}$)
 - Overcharge hysteresis voltage n (n = 1 to 3)
 - 0 V \pm 25 mV, -0.05 V \pm 25 mV, -0.40 V \pm 80 mV
- Delay times for overcharge detection can be set by an internal circuit only (external capacitors are unnecessary)
- Output form is selectable: CMOS output, Nch open-drain output
- Output logic is selectable: Active "H", Active "L"
- High-withstand voltage: Absolute maximum rating 26 V
- Wide operation voltage range: 3.6 V to 24 V
- Wide operation temperature range: $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$
- Low current consumption
 - At $V_{\text{CU}n} - 1.0$ V for each cell: 2.0 μA max. ($T_a = +25^\circ\text{C}$)
 - At 2.0 V for each cell: 0.3 μA max. ($T_a = +25^\circ\text{C}$)
- Lead-free (Sn 100%), halogen-free

■ Application

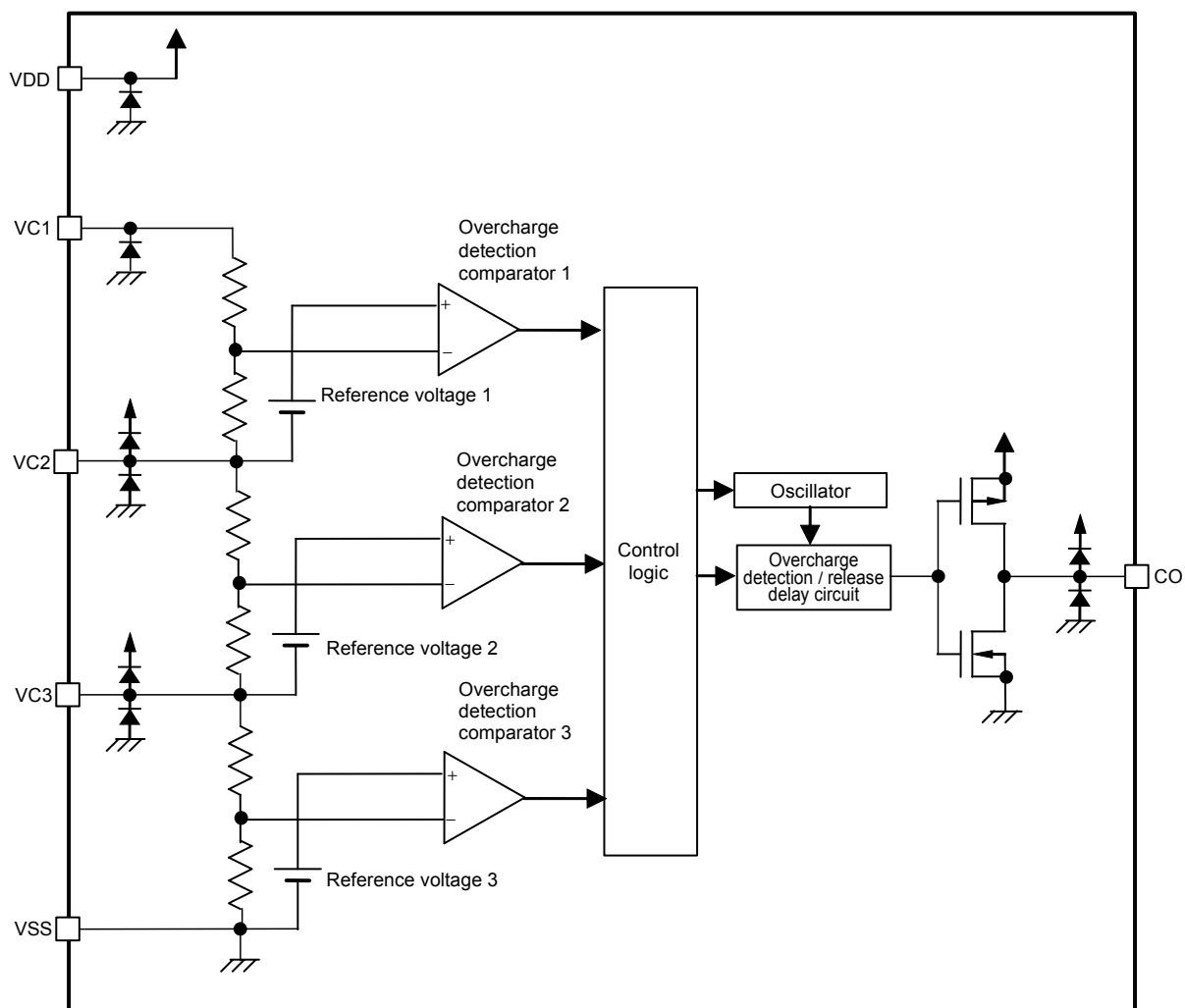
- Lithium-ion rechargeable battery pack (for secondary protection)

■ Packages

- SOT-23-6
- SNT-6A

■ Block Diagram

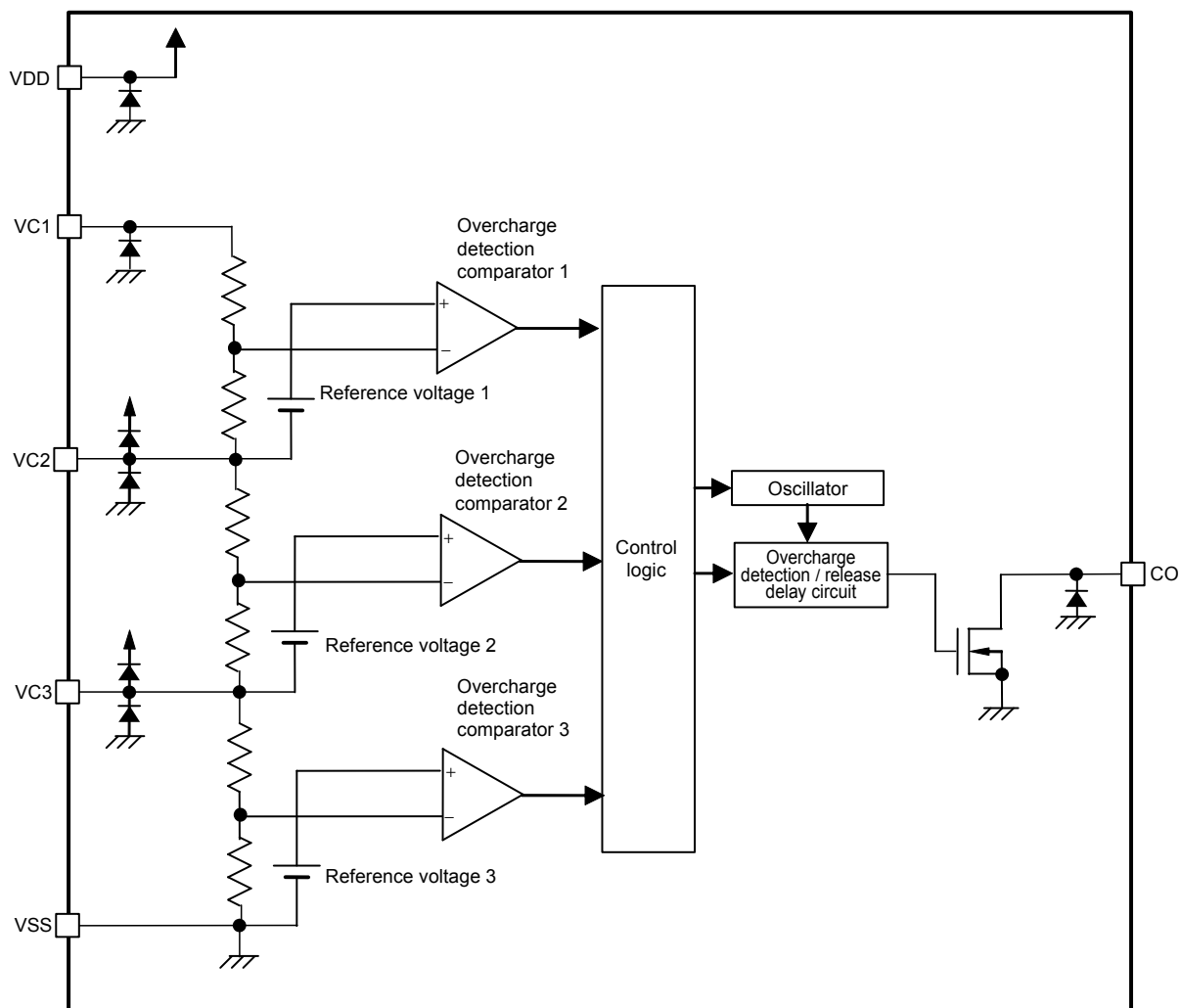
1. CMOS output product



Remark The diodes in the figure are parasitic diodes.

Figure 1

2. Nch open-drain output product

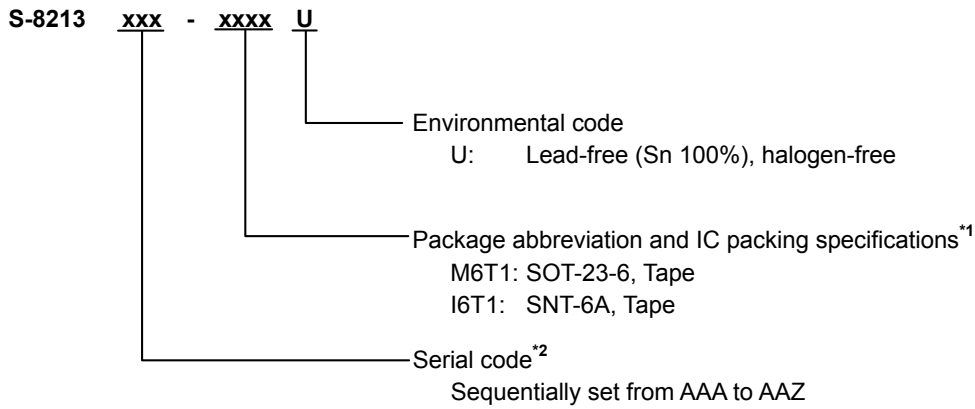


Remark The diodes in the figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product name



*1. Refer to the tape drawing.

*2. Refer to "3. Product name list".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD	–
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

3.1 SNT-6A

Table 2

Product Name	Overcharge Detection Voltage [V _{CU}]	Overcharge Hysteresis Voltage [V _{HC}]	Overcharge Detection Delay Time [t _{CU}]	Output Form	Output Logic
S-8213AAB-I6T1U	4.300 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAC-I6T1U	4.350 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAD-I6T1U	4.400 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAE-I6T1U	4.450 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAF-I6T1U	4.500 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAG-I6T1U	4.300 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAH-I6T1U	4.350 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAI-I6T1U	4.400 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAJ-I6T1U	4.450 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAK-I6T1U	4.500 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAL-I6T1U	4.300 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAM-I6T1U	4.350 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAN-I6T1U	4.400 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAO-I6T1U	4.450 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAP-I6T1U	4.500 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAQ-I6T1U	4.150 V	–0.05 V	2.0 s	CMOS output	Active "L"
S-8213AAR-I6T1U	4.250 V	–0.05 V	2.0 s	CMOS output	Active "L"
S-8213AAS-I6T1U	4.150 V	–0.05 V	2.0 s	Nch open-drain output	Active "H"
S-8213AAT-I6T1U	4.250 V	–0.05 V	2.0 s	Nch open-drain output	Active "H"

Remark Please contact our sales department for the products with detection voltage value other than those specified above.

■ Pin Configurations

1. SOT-23-6

Top view

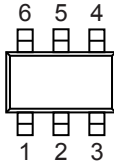


Figure 3

Table 3

Pin No.	Symbol	Description
1	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 3
2	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
3	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
4	VC1	Connection pin for positive voltage of battery 1
5	VDD	Input pin for positive power supply
6	CO	Connection pin of charge control FET gate

2. SNT-6A

Top view

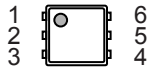


Figure 4

Table 4

Pin No.	Symbol	Description
1	CO	Connection pin of charge control FET gate
2	VDD	Input pin for positive power supply
3	VC1	Connection pin for positive voltage of battery 1
4	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
5	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
6	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 3

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD and VSS	V_{DS}	VDD	$V_{SS} - 0.3$ to $V_{SS} + 26$	V
Input pin voltage	V_{IN}	VC1, VC2, VC3	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
CO output pin voltage	CMOS output product	CO	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
	Nch open-drain output product		$V_{SS} - 0.3$ to $V_{SS} + 26$	V
Power dissipation	SOT-23-6	—	650 ^{*1}	mW
	SNT-6A		400 ^{*1}	mW
Operation ambient temperature	T_{opr}	—	−40 to +85	°C
Storage temperature	T_{stg}	—	−40 to +125	°C

*1. When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

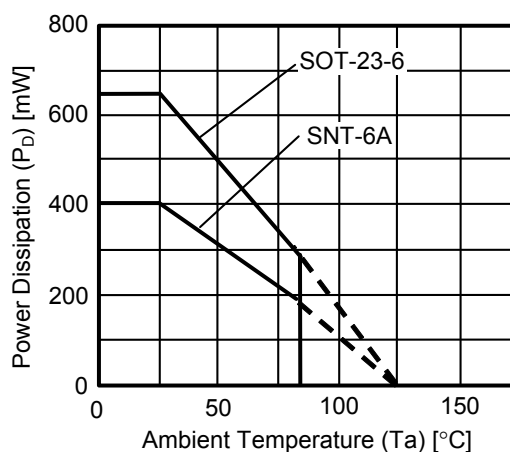


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
DETECTION VOLTAGE							
Overcharge detection voltage n (n = 1, 2, 3)	V _{CU_n}	–	V _{CU} – 0.025	V _{CU}	V _{CU} + 0.025	V	1
		Ta = 0°C to +60°C*1	V _{CU} – 0.030	V _{CU}	V _{CU} + 0.030	V	1
Overcharge hysteresis voltage n (n = 1, 2, 3)	V _{HC_n}	V _{HC} = –0.40 V	V _{HC} – 0.080	V _{HC}	V _{HC} + 0.080	V	1
		V _{HC} = 0 V, –0.05 V	V _{HC} – 0.025	V _{HC}	V _{HC} + 0.025	V	1
INPUT VOLTAGE							
Operation voltage between VDD and VSS	V _{DSOP}	–	3.6	–	24	V	–
INPUT CURRENT							
Current consumption during operation	I _{OPE}	V1 = V2 = V3 = V _{CU} – 1.0 V	–	–	2.0	μA	3
Current consumption during overdischarge	I _{PDN}	V1 = V2 = V3 = 2.0 V	–	–	0.3	μA	3
VC1 pin current	I _{VC1}	V1 = V2 = V3 = V _{CU} – 1.0 V	–	–	0.3	μA	4
VC2 pin, VC3 pin current	I _{VC2} , I _{VC3}	V1 = V2 = V3 = V _{CU} – 1.0 V	–0.3	0	0.3	μA	4
OUTPUT CURRENT							
CO pin sink current	I _{COL}	–	0.4	–	–	mA	5
CO pin source current (CMOS output product)	I _{COH}	–	20	–	–	μA	5
CO pin leakage current (Nch open-drain output product)	I _{COLL}	–	–	–	0.1	μA	5
DELAY TIME							
Overcharge detection delay time	t _{CU}	–	t _{CU} × 0.8	t _{CU}	t _{CU} × 1.2	s	1
Transition time to test mode	t _{TST}	–	–	–	20	ms	2

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

1. Overcharge detection voltage, overcharge hysteresis voltage (Test circuit 1)

Set SW1 to OFF and ON in CMOS output product and Nch open-drain output product, respectively.

1. 1 Overcharge detection voltage n (V_{CU_n})

Set $V1 = V2 = V3 = V_{CU} - 0.05$ V. The Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when the CO pin's output changes after the voltage of V1 has been gradually increased.

Overcharge detection voltage V_{CU_n} ($n = 2, 3$) can be determined in the same way as when $n = 1$.

1. 2 Overcharge hysteresis voltage n (V_{HC_n})

Set $V1 = V_{CU} + 0.05$ V, $V2 = V3 = 2.5$ V. The overcharge hysteresis voltage 1 (V_{HC1}) is the difference between V1 voltage and V_{CU1} when the CO pin's output changes after the V1 voltage has been gradually decreased.

Overcharge hysteresis voltage V_{HC_n} ($n = 2, 3$) can be determined in the same way as when $n = 1$.

2. Output current (Test circuit 5)

Set SW1 and SW2 to OFF.

2. 1 Active "H"

2. 1. 1 CO pin source current (I_{COH})

Set SW1 to ON after setting $V1 = 5.0$ V, $V2 = V3 = 3.0$ V, $V4 = 0.5$ V. I1 is the CO pin source current (I_{COH}) at that time.

2. 1. 2 CO pin sink current (I_{COL})

Set SW2 to ON after setting $V1$ to $V3 = 3.5$ V, $V5 = 0.5$ V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 1. 3 CO pin leakage current (I_{COLL})

Set SW2 to ON after setting $V1 = 5.0$ V, $V2 = V3 = 3.0$ V, $V5 = 26$ V. I2 is the CO pin leakage current (I_{COLL}) at that time.

2. 2 Active "L"

2. 2. 1 CO pin source current (I_{COH})

Set SW1 to ON after setting $V1$ to $V3 = 3.5$ V, $V4 = 0.5$ V. I1 is the CO pin source current (I_{COH}) at that time.

2. 2. 2 CO pin sink current (I_{COL})

Set SW2 to ON after setting $V1 = 5.0$ V, $V2 = V3 = 3.0$ V, $V5 = 0.5$ V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 2. 3 CO pin leakage current (I_{COLL})

Set SW2 to ON after setting $V1$ to $V3 = 3.5$ V, $V5 = 26$ V. I2 is the CO pin leakage current (I_{COLL}) at that time.

3. Overcharge detection delay time (t_{CU})
(Test circuit 1)

Set SW1 to OFF and ON in CMOS output product and Nch open-drain output product, respectively.

Increase V1 up to 5.0 V after setting V1 = V2 = V3 = 3.5 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output changes.

4. Transition time to test mode (t_{TST})
(Test circuit 2)

Set SW1 to OFF and ON in CMOS output product and Nch open-drain output product, respectively.

Increase V4 up to 4.0 V, and decrease V4 again to 0 V after setting V1 = V2 = V3 = 3.5 V, and V4 = 0 V.

When the period from when V4 was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the delay time is t_{CU} . However, when the period from when V4 is raised to when it has fallen is gradually made longer, the delay time during the subsequent overcharge detection operation is shorter than t_{CU} . The transition time to test mode (t_{TST}) is the period from when V4 was raised to when it has fallen at that time.

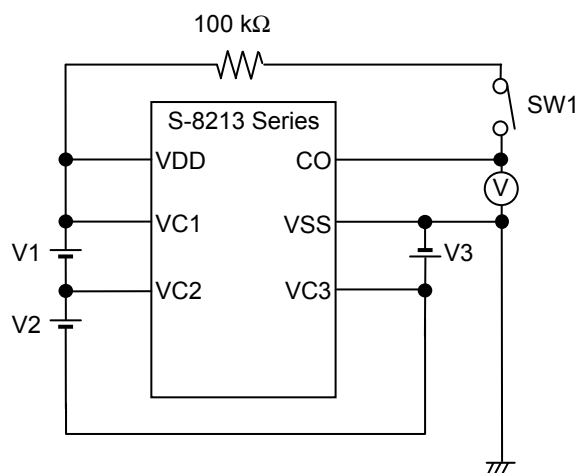


Figure 6 Test Circuit 1

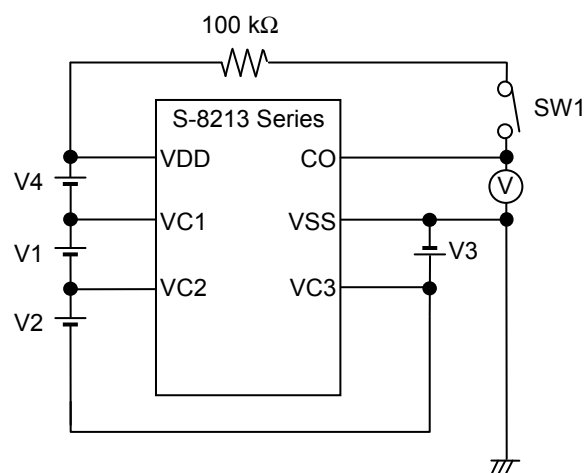


Figure 7 Test Circuit 2

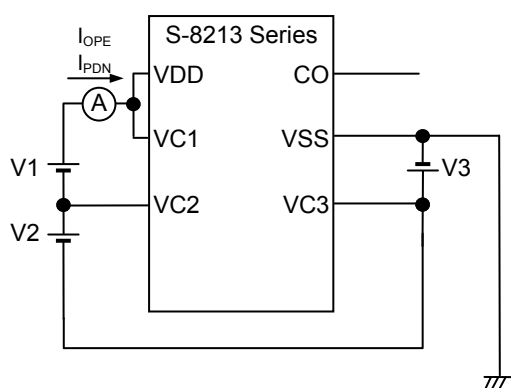


Figure 8 Test Circuit 3

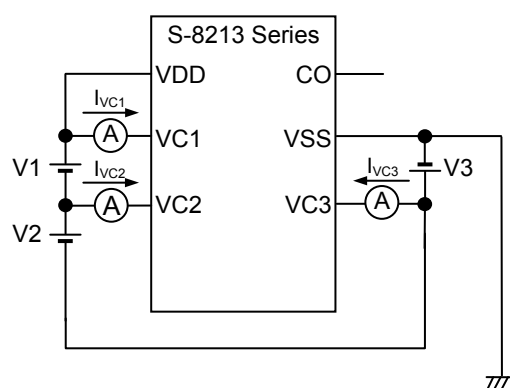


Figure 9 Test Circuit 4

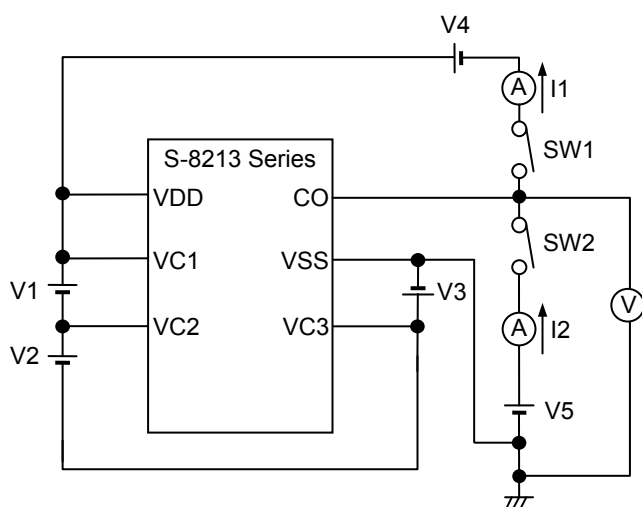


Figure 10 Test Circuit 5

■ Operation

Remark Refer to "■ Battery Protection IC Connection Examples".

1. Normal status

If the voltage of each of the batteries is lower than "the overcharge detection voltage (V_{CU_n}) + the overcharge hysteresis voltage (V_{HC_n})", CO pin output changes to "L" (Active "H") or "H" (Active "L"). This is called normal status.

2. Overcharge status

When the voltage of one of the batteries exceeds V_{CU_n} during charging under normal conditions and the status is retained for the overcharge detection delay time (t_{CU}) or longer, CO pin output changes. This is called overcharge status. Connecting FET to the CO pin provides charge control and a second protection.

If the voltage of each of the batteries is lower than $V_{CU_n} + V_{HC_n}$ and the status is retained for 2.0 ms typ. or longer, the S-8213 Series changes to normal status.

3. Test mode

The overcharge detection delay time (t_{CU}) can be shortened by entering the test mode.

The test mode can be set by retaining the VDD pin voltage 4.0 V or more higher than the VC1 pin voltage for 20 ms or longer. The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the VC1 pin voltage.

After that, the latch for retaining the test mode is reset and the S-8213 Series exits from test mode under the overcharge status.

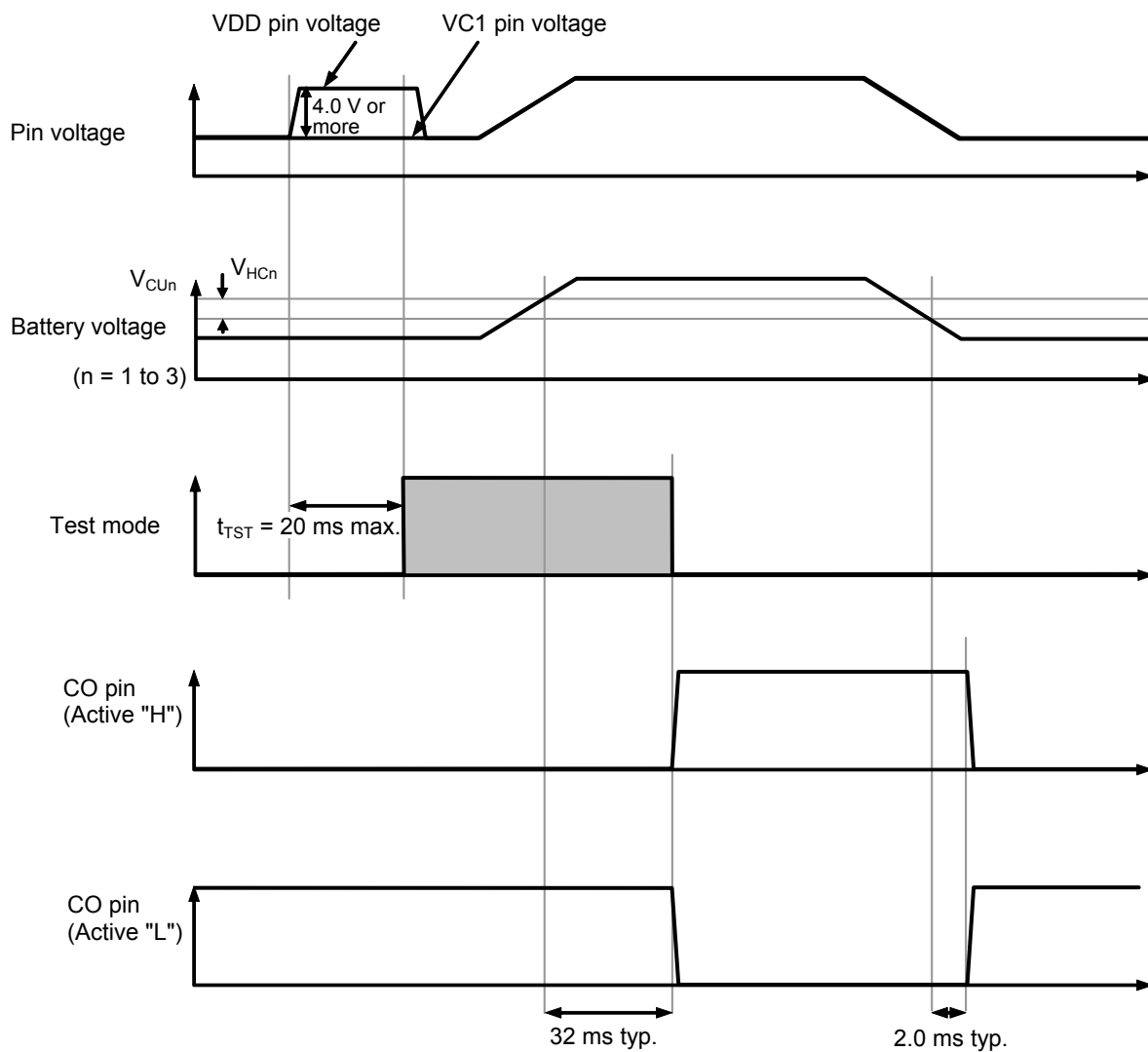


Figure 11

■ Timing Charts

1. Overcharge detection operation

1.1 CMOS output product

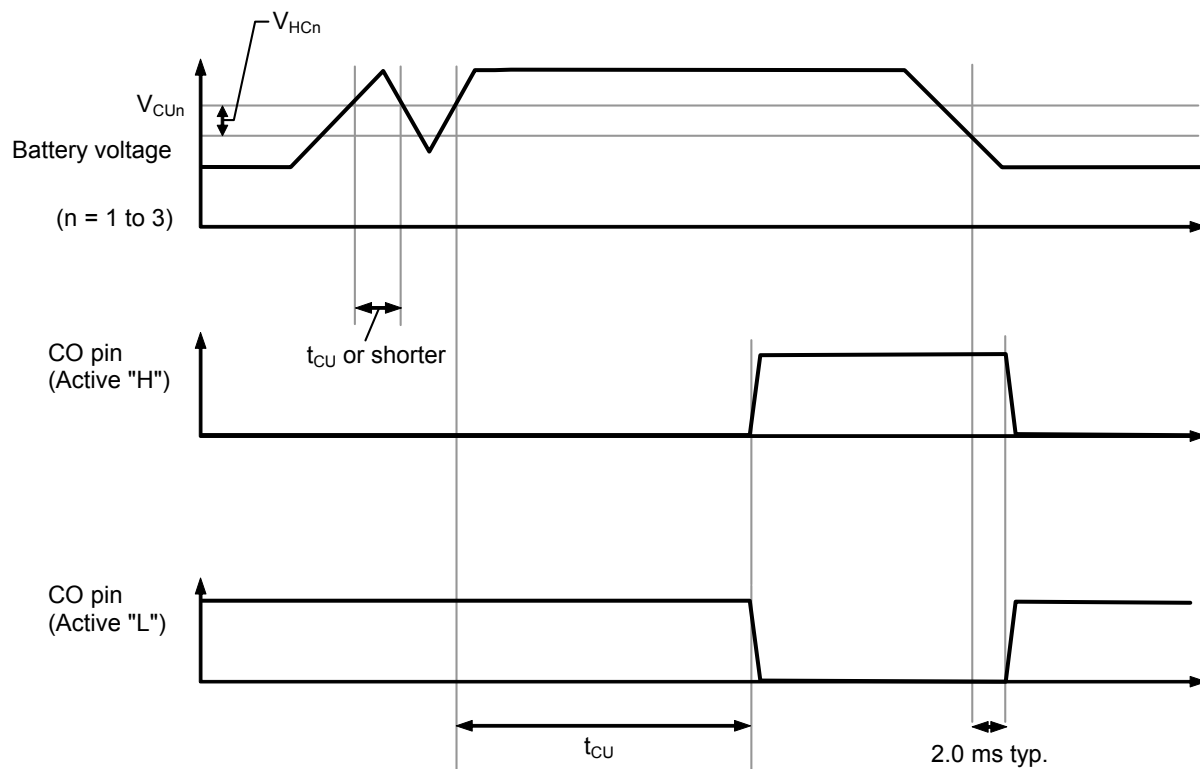


Figure 12

1.2 Nch open-drain output product

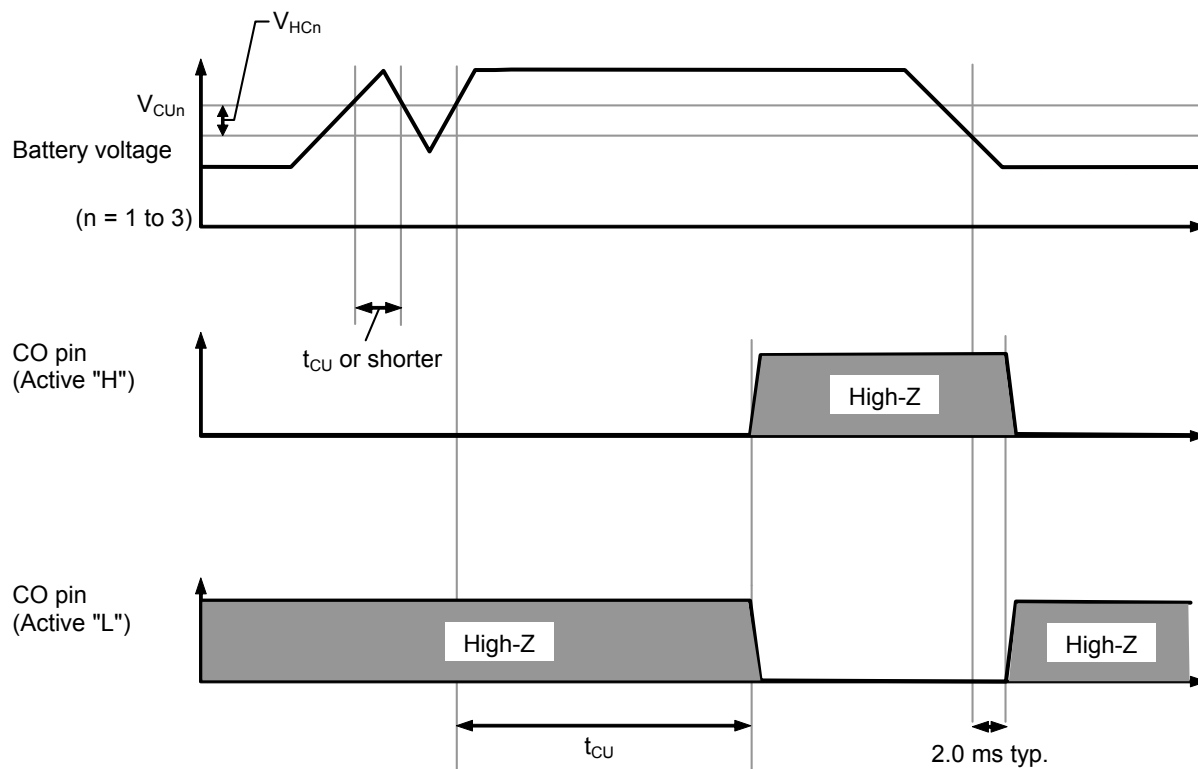


Figure 13

■ Battery Protection IC Connection Examples

1. 3-serial cell (CMOS output product)

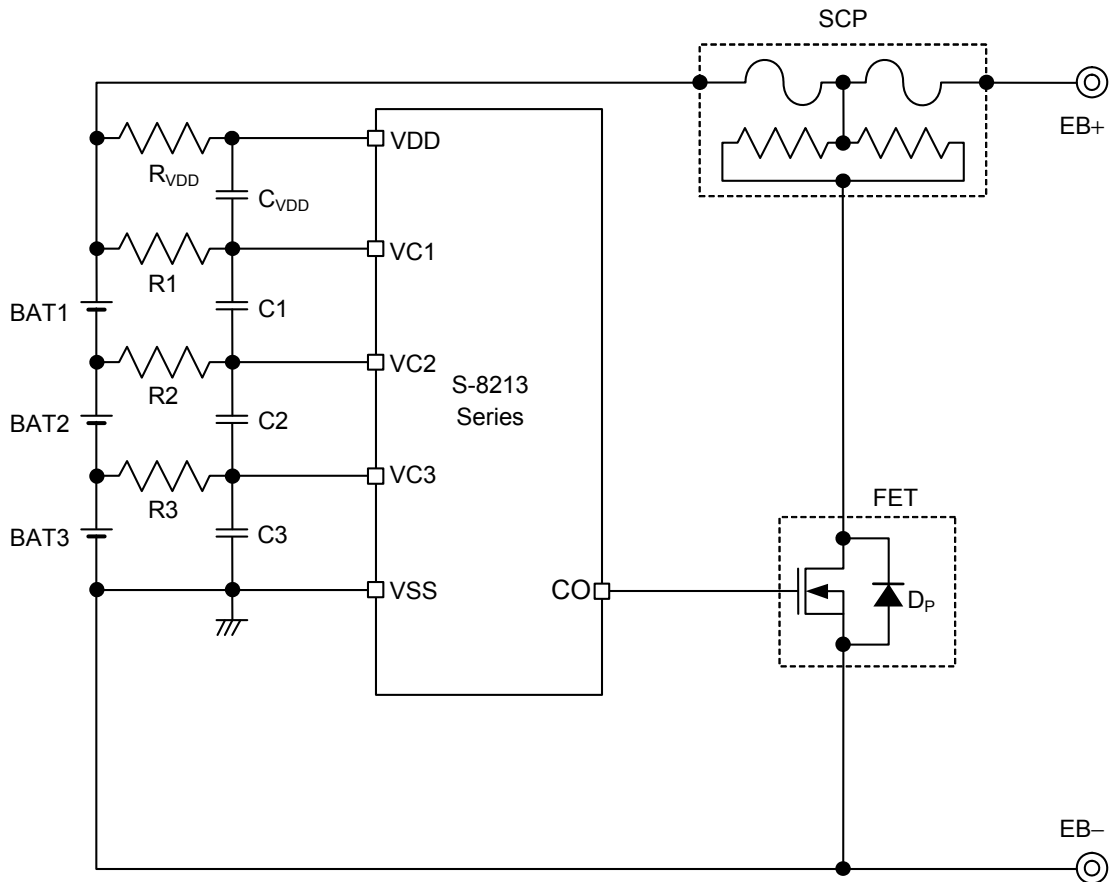


Figure 14

Table 7 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.2	1	2	kΩ
2	C1 to C3, C _{VDD}	0.01	0.1	1	μF
3	R _{VDD}	50	100	500	Ω

- Caution**
1. The above constants are subject to change without prior notice.
 2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
 3. Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.
 4. Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition $(R_{VDD}) \times (C1 \text{ to } C3, C_{VDD}) \geq 5 \times 10^{-6}$ is satisfied.
 5. Set R1 to R3, C1 to C3, and C_{VDD} so that the condition $(R1 \text{ to } R3) \times (C1 \text{ to } C3, C_{VDD}) \geq 1 \times 10^{-4}$ is satisfied.
 6. Since CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

2. 2-serial cell (CMOS output product)

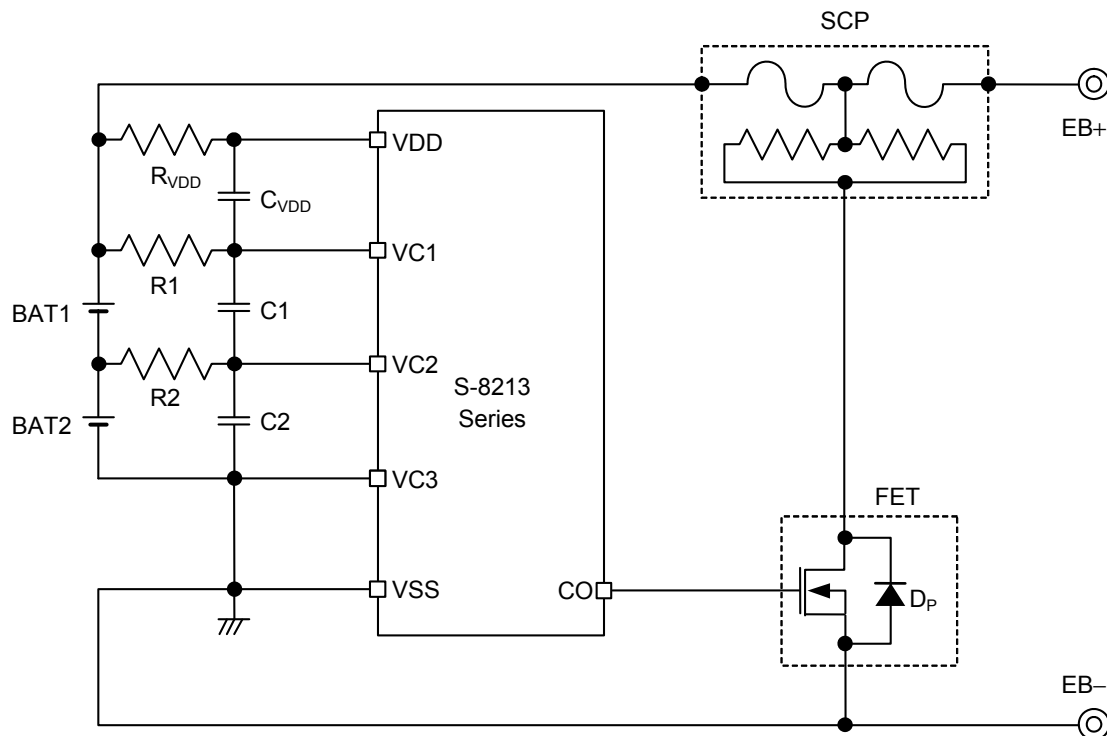


Figure 15

Table 8 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1, R2	0.2	1	2	kΩ
2	C1, C2, C_VDD	0.01	0.1	1	μF
3	R_VDD	50	100	500	Ω

- Caution**
1. The above constants are subject to change without prior notice.
 2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
 3. Set the same constants to R1, R2 and to C1, C2 and C_VDD.
 4. Set R_VDD, C1, C2, and C_VDD so that the condition $(R_{VDD}) \times (C1, C2, C_{VDD}) \geq 5 \times 10^{-6}$ is satisfied.
 5. Set R1, R2, C1, C2, and C_VDD so that the condition $(R1, R2) \times (C1, C2, C_{VDD}) \geq 1 \times 10^{-4}$ is satisfied.
 6. Since CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.

[For SCP, contact]

Global Sales & Marketing Division, Dexerials Corporation
Gate City Osaka East Tower 8F, 1-11-2
Osaka, Shinagawa-ku, Tokyo, 141-0032, Japan
TEL +81-3-5435-3946
Contact Us: <http://www.dexerials.jp/en/>

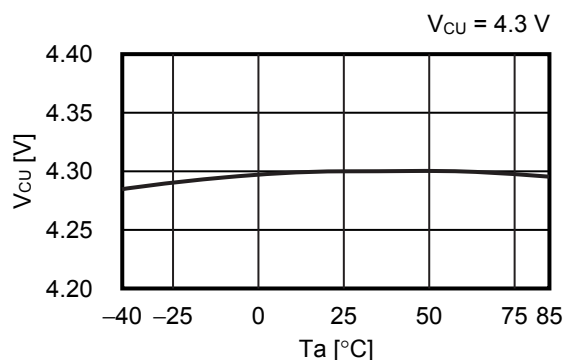
■ Precautions

- Do not connect batteries charged with $V_{CUH} + V_{HCN}$ or higher. If the connected batteries include a battery charged with $V_{CUH} + V_{HCN}$ or more, the S-8213 series may become overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in "**■ Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

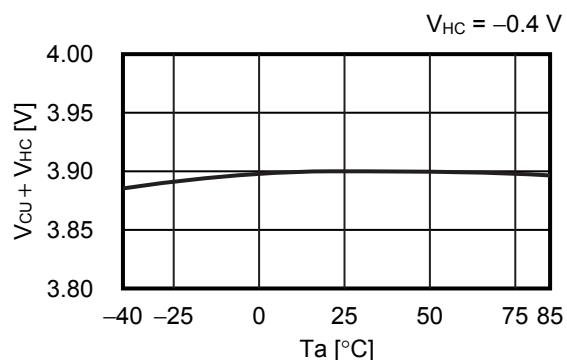
■ Characteristics (Typical Data)

1. Detection voltage

1. 1 V_{CU} vs. T_a

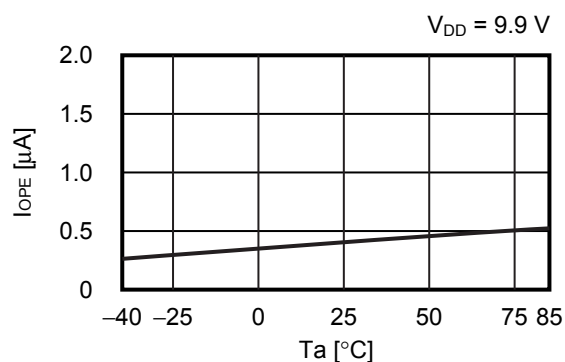


1. 2 $V_{CU} + V_{HC}$ vs. T_a

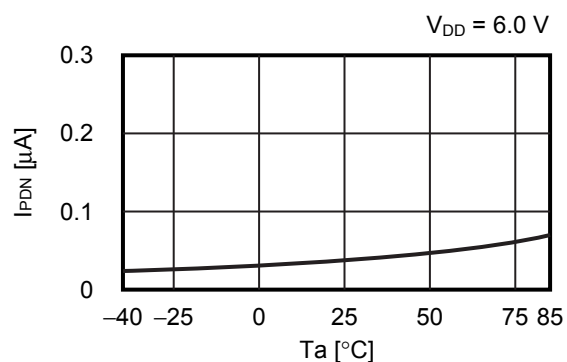


2. Current consumption

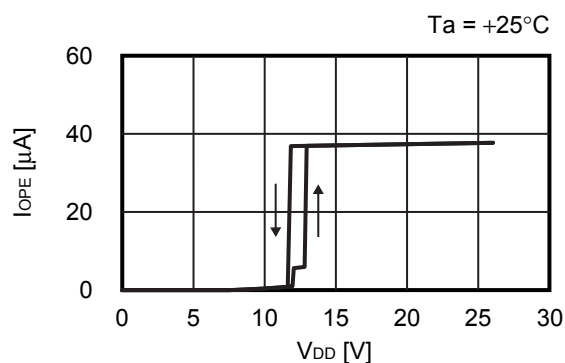
2. 1 I_{OPE} vs. T_a



2. 2 I_{PDN} vs. T_a

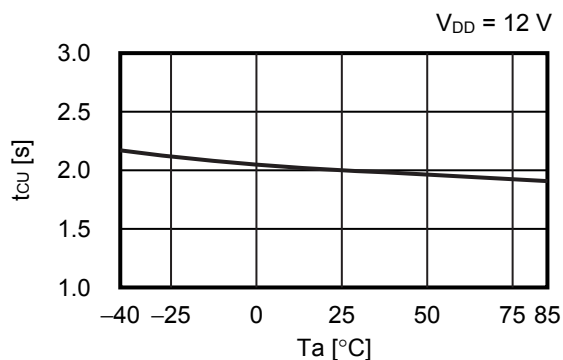


2. 3 I_{OPE} vs. V_{DD}



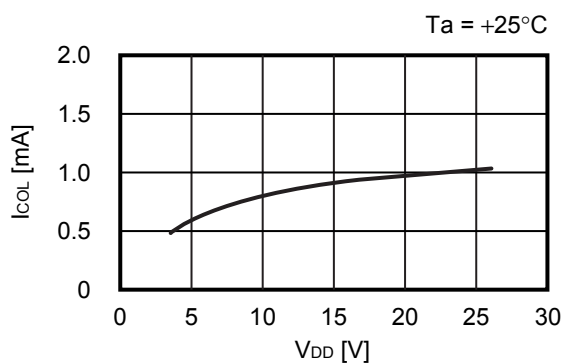
3. Delay time

3.1 t_{CU} vs. T_a

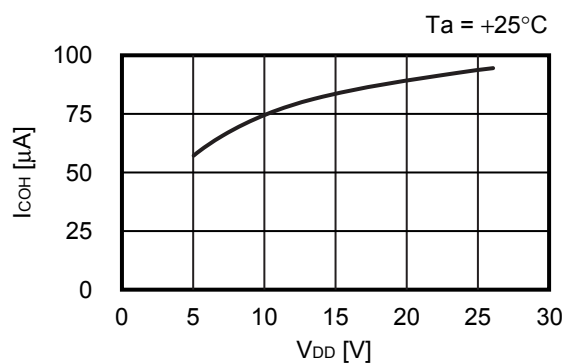


4. Output current

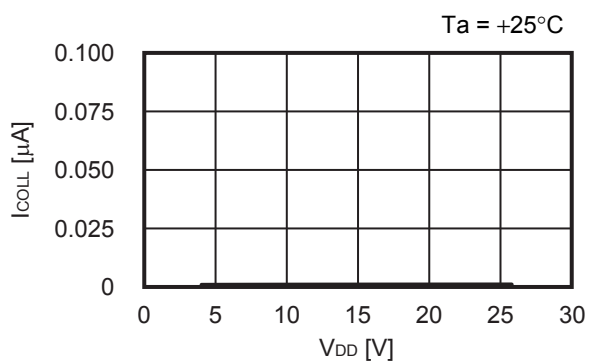
4.1 I_{COL} vs. V_{DD}



4.2 I_{COH} vs. V_{DD}

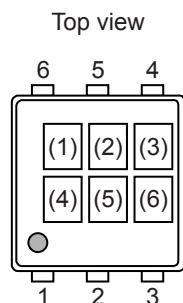


4.3 I_{COLL} vs. V_{DD}



■ Marking Specification

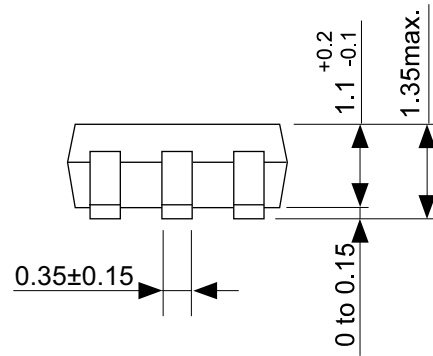
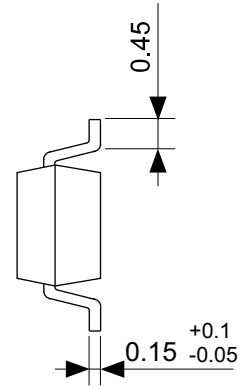
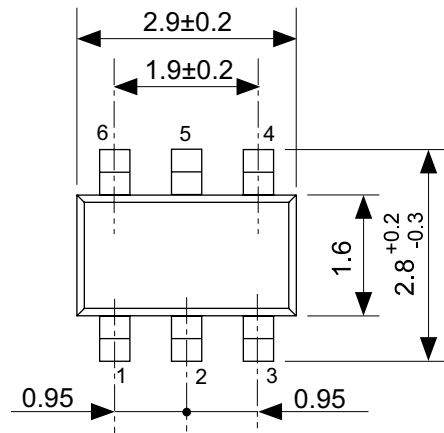
1. SNT-6A




(1) to (3): Product code (Refer to **Product name vs. Product code**)
 (4) to (6): Lot number

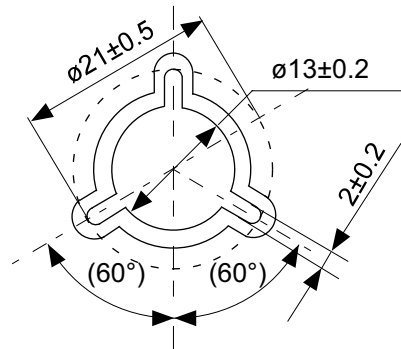
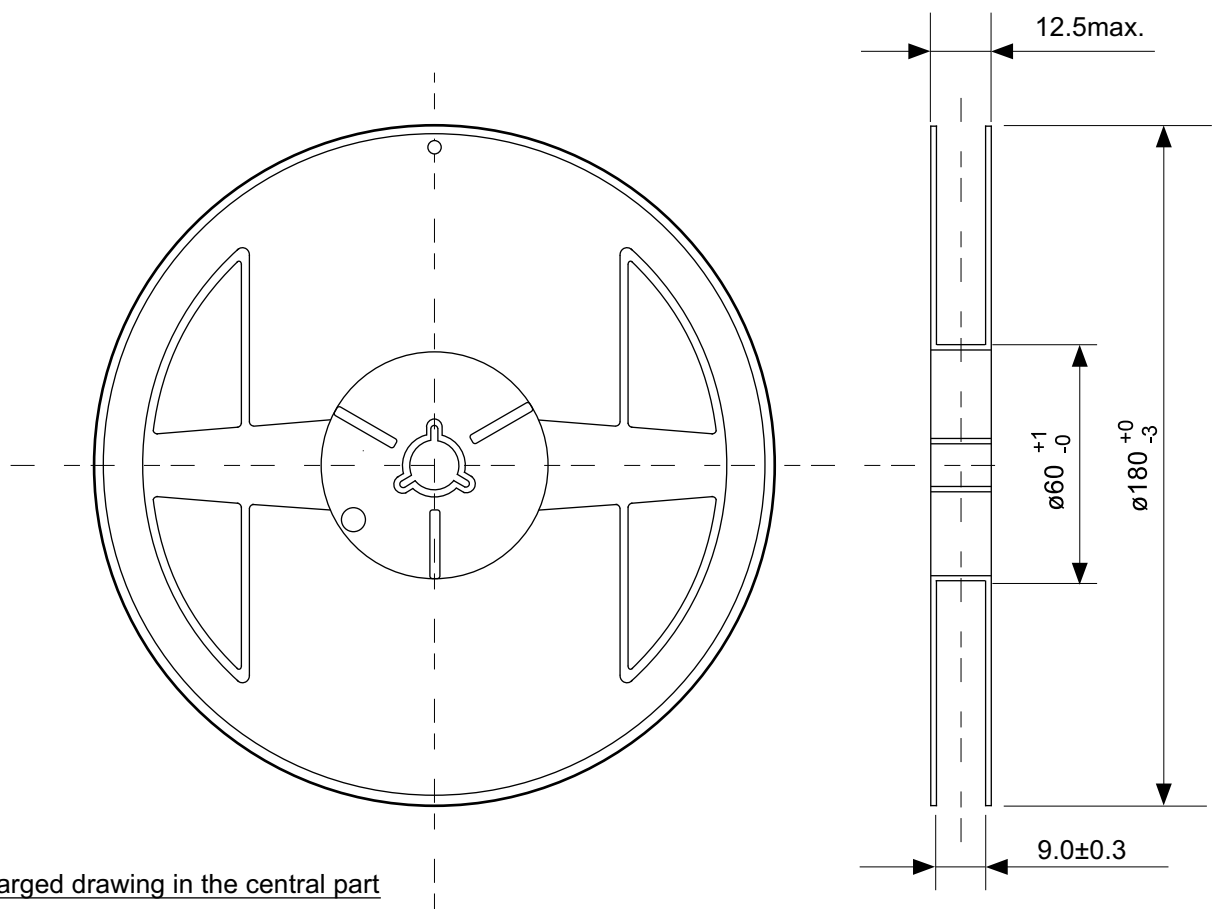
Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8213AAB-I6T1U	S	U	B
S-8213AAC-I6T1U	S	U	C
S-8213AAD-I6T1U	S	U	D
S-8213AAE-I6T1U	S	U	E
S-8213AAF-I6T1U	S	U	F
S-8213AAG-I6T1U	S	U	G
S-8213AAH-I6T1U	S	U	H
S-8213AAI-I6T1U	S	U	I
S-8213AAJ-I6T1U	S	U	J
S-8213AAK-I6T1U	S	U	K
S-8213AAL-I6T1U	S	U	L
S-8213AAM-I6T1U	S	U	M
S-8213AAN-I6T1U	S	U	N
S-8213AAO-I6T1U	S	U	O
S-8213AAP-I6T1U	S	U	P
S-8213AAQ-I6T1U	S	U	Q
S-8213AAR-I6T1U	S	U	R
S-8213AAS-I6T1U	S	U	S
S-8213AAT-I6T1U	S	U	T



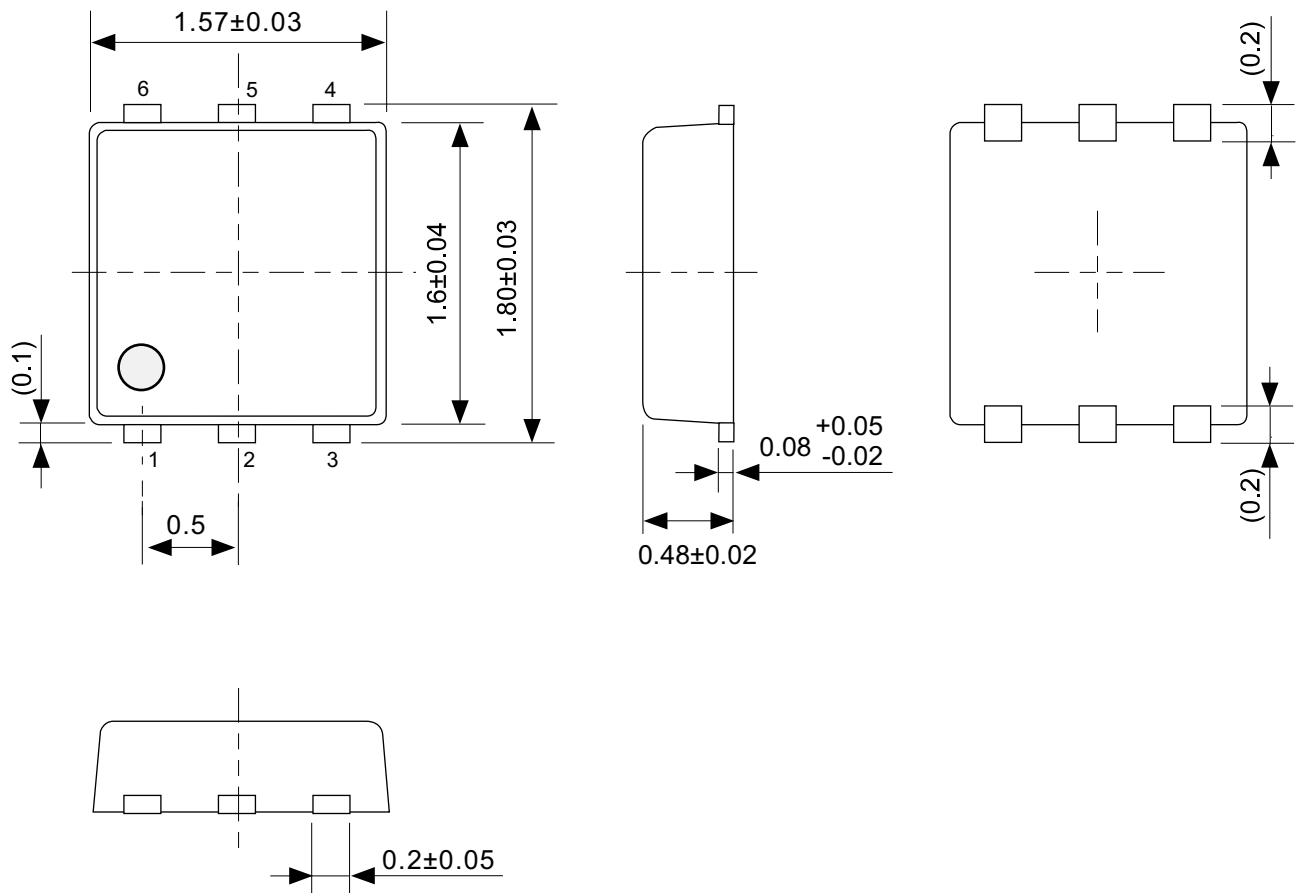
No. MP006-A-P-SD-2.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	




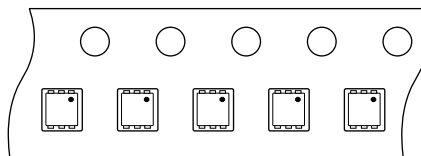
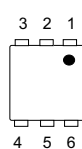
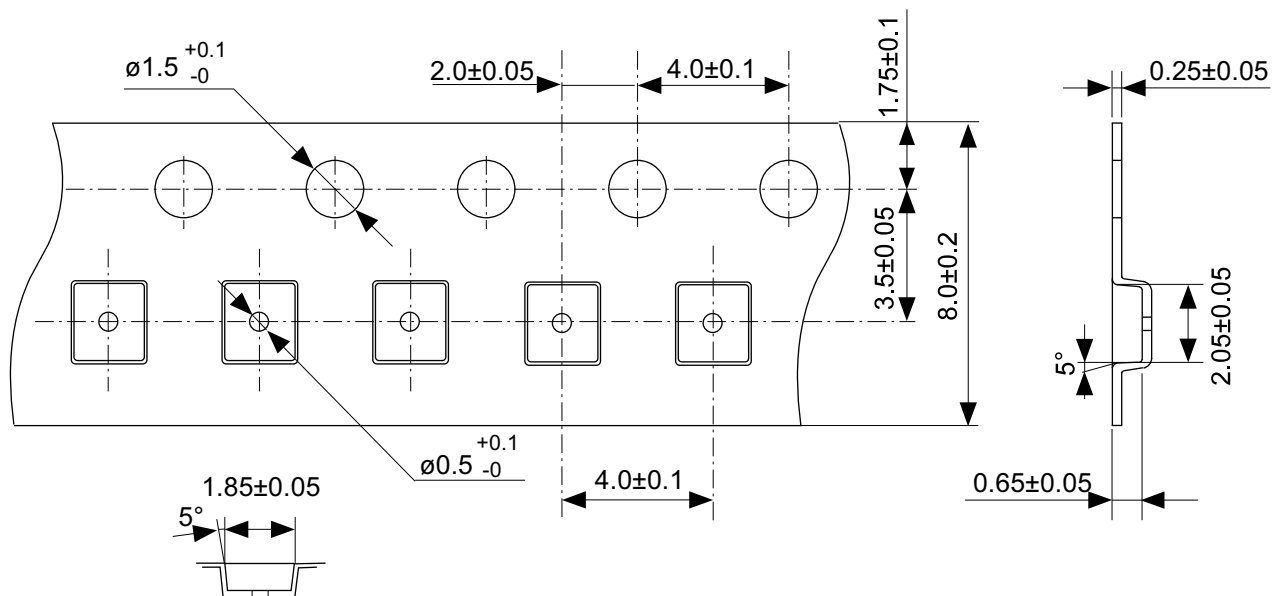
No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
ANGLE		QTY	3,000
UNIT	mm		
SII Semiconductor Corporation			



No. PG006-A-P-SD-2.1

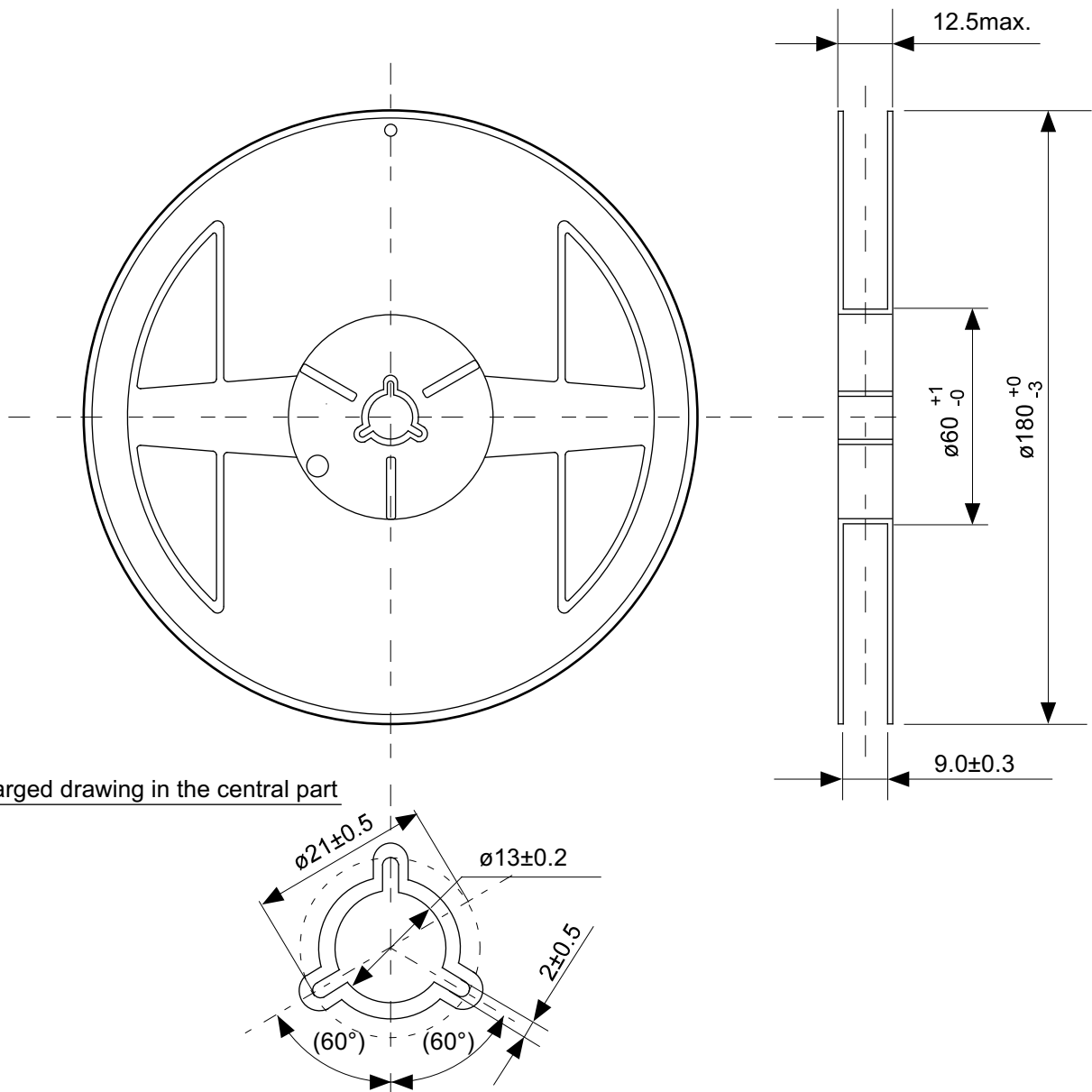
TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	



Feed direction

No. PG006-A-C-SD-1.0

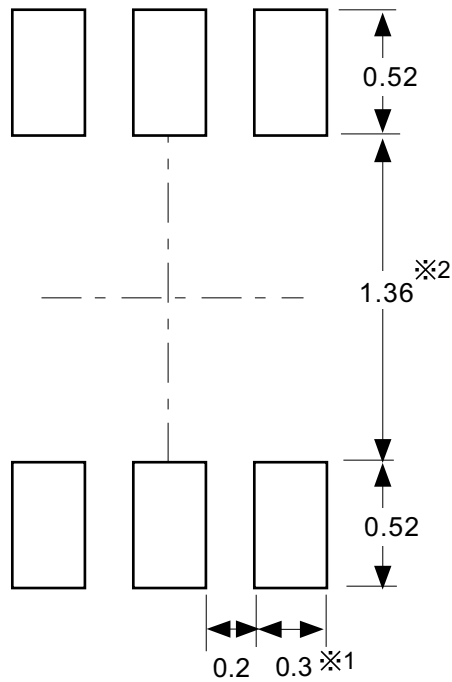
TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-1.0
ANGLE	
UNIT	mm
SII Semiconductor Corporation	



Enlarged drawing in the central part

No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
SII Semiconductor Corporation			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.).

※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

- 注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
 2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
 3. マスク開口サイズと開口位置はランドパターンと合わせてください。
 4. 詳細は“SNTパッケージ活用の手引き”を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).

※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

- Caution**
1. Do not do silkscreen printing and solder printing under the mold resin of the package.
 2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
 3. Match the mask aperture size and aperture position with the land pattern.
 4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.).

※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

- 注意
1. 请勿在树脂型封装的下面印刷丝网、焊锡。
 2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
 3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
 4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
SII Semiconductor Corporation	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
SII Semiconductor Corporation is not responsible for damages caused by the reasons other than the products or infringement of third-party intellectual property rights and any other rights due to the use of the information described herein.
3. SII Semiconductor Corporation is not responsible for damages caused by the incorrect information described herein.
4. Take care to use the products described herein within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
SII Semiconductor Corporation is not responsible for damages caused by failures and/or accidents, etc. that occur due to the use of products outside their specified ranges.
5. When using the products described herein, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products described herein, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products described herein must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. SII Semiconductor Corporation is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products described herein are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not use those products without the prior written permission of SII Semiconductor Corporation. Especially, the products described herein cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.
Prior consultation with our sales office is required when considering the above uses.
SII Semiconductor Corporation is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
The user of these products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products described herein are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products described herein do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Take care when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products described herein, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of SII Semiconductor Corporation.
The information described herein does not convey any license under any intellectual property rights or any other rights belonging to SII Semiconductor Corporation or a third party. Reproduction or copying of the information described herein for the purpose of disclosing it to a third-party without the express permission of SII Semiconductor Corporation is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

1.0-2016.01

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Seiko Instruments:

[S-8213AAJ-M6T1U](#) [S-8213AAE-M6T1U](#) [S-8213AAK-I6T1U](#) [S-8213AAJ-I6T1U](#) [S-8213AAI-I6T1U](#) [S-8213AAB-I6T1U](#) [S-8213AAE-I6T1U](#) [S-8213AAC-M6T1U](#) [S-8213AAG-I6T1U](#) [S-8213AAD-I6T1U](#) [S-8213AAI-M6T1U](#) [S-8213AAG-M6T1U](#) [S-8213AAF-M6T1U](#) [S-8213AAD-M6T1U](#) [S-8213AAB-M6T1U](#) [S-8213AAC-I6T1U](#) [S-8213AAF-I6T1U](#) [S-8213AAK-M6T1U](#) [S-8213AAH-I6T1U](#) [S-8213AAH-M6T1U](#)