HAMAMATSU

NEW

CCD image sensors

S11071/S10420 series

Improved etaloning characteristics, High-speed type and low noise type available

The S11071/S10420 series are back-thinned CCD image sensors designed for spectrometers. Two types consisting of a high-speed type (S11071 series) and low noise type (S10420 series) are available with improved etaloning characteristics. The S11071/S10420 series offer nearly flat spectral response characteristics with high quantum efficiency from the UV to near infrared region.

Features

- **Improved etaloning characteristics**
- **High sensitivity over a wide spectral range and nealy flat spectral response characteristics**
- **High CCD node sensitivity: 8 μV/e⁻ (S11071 series) 6.5 μV/e⁻ (S10420 series)**
- **High full well capacity and wide dynamic range (with anti-blooming function)**
- **Pixel size: 14 × 14 μm**

Applications

- **Spectrometers, etc.**

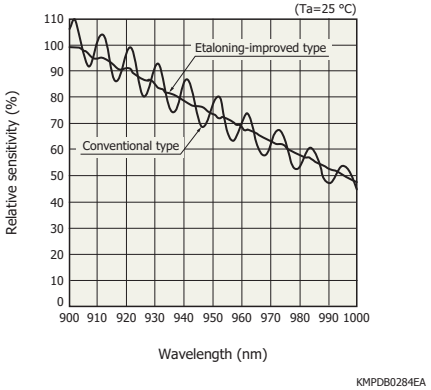
Selection guide

Type No.	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Readout speed max. (MHz)	Applicable driver circuit
S11071-1004	1044 × 22	1024 × 16	14.336 × 0.224	10	C11288
S11071-1006	1044 × 70	1024 × 64	14.336 × 0.896		
S11071-1104	2068 × 22	2048 × 16	28.672 × 0.224		
S11071-1106	2068 × 70	2048 × 64	28.672 × 0.896		
S10420-1004-01	1044 × 22	1024 × 16	14.336 × 0.224	0.5	C11287
S10420-1006-01	1044 × 70	1024 × 64	14.336 × 0.896		
S10420-1104-01	2068 × 22	2048 × 16	28.672 × 0.224		
S10420-1106-01	2068 × 70	2048 × 64	28.672 × 0.896		

Improved etaloning characteristics

Etaloning is an interference phenomenon that occurs when the light incident on a CCD repeatedly reflects between the front and back surfaces of the CCD while being attenuated, and causes alternately high and low sensitivity. When long-wavelength light enters a back-thinned CCD, etaloning occurs due to the relationship between the silicon substrate thickness and the absorption length. The S11071/S10420 series back-thinned CCDs have achieved a significant improvement in etaloning by using a unique structure that is unlikely to cause interference.

Etaloning characteristics (typical example)



General ratings

Parameter	S11071 series	S10420 series
Pixel size	14 (H) × 14 (V) µm	
Vertical clock phase	2-phase	
Horizontal clock phase	4-phase	
Output circuit	Two-stage MOSFET source follower	One-stage MOSFET source follower
Package	24-pin ceramic DIP (refer to dimensional outline)	
Window*1	Quartz glass	

*1: Temporary window type (ex: S11071-1106N, S10420-1106-01N) is available upon request.

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2		Topr	-50	-	+50	°C
Storage temperature		Tstg	-50	-	+70	°C
OD voltage	S11071 series	V_{OD}	-0.5	-	+25	V
	S10420 series		-0.5	-	+30	
RD voltage		V_{RD}	-0.5	-	+18	V
Vret voltage		Vret	-0.5	-	+18	V
OFD voltage		V_{OFD}	-0.5	-	+18	V
ISV/ISH voltage		V_{ISV}, V_{ISH}	-0.5	-	+18	V
OFG voltage		V_{OFG}	-10	-	+15	V
IGV voltage		V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage		V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage		V_{SG}	-10	-	+15	V
OG voltage		V_{OG}	-10	-	+15	V
RG voltage		V_{RG}	-10	-	+15	V
TG voltage		V_{TG}	-10	-	+15	V
Vertical clock voltage		V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage		V_{P1H}, V_{P2H} V_{P3H}, V_{P4H}	-10	-	+15	V

*2: Chip temperature

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	S11071 series			S10420 series			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output transistor drain voltage			V_{OD}	12	15	18	23	24	25	V
Reset drain voltage			V_{RD}	14	15	16	11	12	13	V
Over flow drain voltage			V_{OFD}	11	12	13	11	12	13	V
Over flow gate voltage			V_{OFG}	0	13	14	0	12	13	V
Output gate voltage			V_{OG}	4	5	6	4	5	6	V
Substrate voltage			V_{SS}	-	0	-	-	0	-	V
Output amplifier return voltage			Vret	-	1	2				V
Test point	Input source		V_{ISV}, V_{ISH}	-	V_{RD}	-	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	-9	-8	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	-9	-8	-	V
Vertical shift register clock voltage		High	V_{P1VH}, V_{P2VH}	4	6	8	4	6	8	V
		Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH} V_{P3HH}, V_{P4HH}	4	6	8	4	6	8	V
		Low	V_{P1HL}, V_{P2HL} V_{P3HL}, V_{P4HL}	-6	-5	-4	-6	-5	-4	
Summing gate voltage		High	V_{SGH}	4	6	8	4	6	8	V
		Low	V_{SGL}	-6	-5	-4	-6	-5	-4	
Reset gate voltage		High	V_{RGH}	4	6	8	4	6	8	V
		Low	V_{RGL}	-6	-5	-4	-6	-5	-4	
Transfer gate voltage		High	V_{TGH}	4	6	8	4	6	8	V
		Low	V_{TGL}	-9	-8	-7	-9	-8	-7	
External load resistance			R_L	2.0	2.2	2.4	90	100	110	kΩ

Electrical characteristics (Ta=25 °C)

Parameter		Symbol	S11071 series			S10420 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Signal output frequency*3		fc	-	5	10	-	0.25	0.5	MHz
Vertical shift register capacitance	-1004(-01)	C_{P1V}, C_{P2V}	-	200	-	-	200	-	pF
	-1006(-01)		-	600	-	-	600	-	
	-1104(-01)		-	400	-	-	400	-	
	-1106(-01)		-	1200	-	-	1200	-	
Horizontal shift register capacitance	-1004(-01)/-1006(-01)	C_{P1H}, C_{P2H} C_{P3H}, C_{P4H}	-	80	-	-	80	-	pF
	-1104(-01)/-1106(-01)		-	160	-	-	160	-	
Summing gate capacitance		C_{SG}	-	10	-	-	10	-	pF
Reset gate capacitance		C_{RG}	-	10	-	-	10	-	pF
Transfer gate capacitance	-1004(-01)/-1006(-01)	C_{TG}	-	30	-	-	30	-	pF
	-1104(-01)/-1106(-01)		-	60	-	-	60	-	
Charge transfer efficiency*4		CTE	0.99995	0.99999	-	0.99995	0.99999	-	-
DC output level*3		Vout	-	8 (TBD)	-	17	18	19	V
Output impedance*3		Zo	-	0.3 (TBD)	-	-	10	-	kΩ
Power consumption*3, *5		P	-	75	-	-	4	-	mW

*3: The values depend on the load resistance. (S11071 series: V_{OD}=15 V, R_L=2.2 kΩ, S10420 series: V_{OD}=24 V, R_L=100 kΩ)
*4: Charge transfer efficiency per pixel, measured at half of the full well capacity
*5: Power consumption of the on-chip amplifier plus load resistance

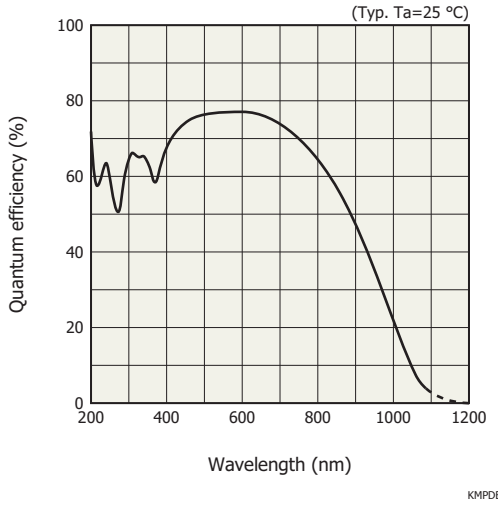
Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	S11071 series			S10420 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Saturation output voltage		Vsat	-	Fw × Sv	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	50	60	-	50	60	-	ke⁻
	Horizontal		150	200	-	250	300	-	
CCD node sensitivity*6		Sv	-	8 (TBD)	-	5.5	6.5	7.5	μV/e⁻
Dark current*7		DS	-	50	500	-	50	500	e⁻/pixel/s
Readout noise*8		Nr	-	23	28	-	6	15	e⁻ rms
Dynamic range*9	Line binning	DR	6520	8700	-	41700	50000	-	-
Spectral response range		λ	-	200 to 1100	-	-	200 to 1100	-	nm
Photo response non-uniformity*10		PRNU	-	±3	±10	-	±3	±10	%

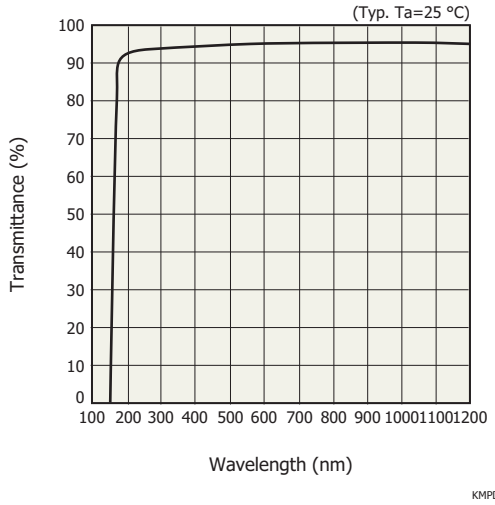
*6: The values depend on the load resistance. (S11071 series: V_{OD}=15 V, R_L=2.2 kΩ, S10420 series: V_{OD}=24 V, R_L=100 kΩ)
*7: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*8: S11071 series: readout frequency 2 MHz, S10420 series (temperature: -40 °C): 20 kHz
*9: Dynamic range (DR) = Full well capacity / Readout noise
*10: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

$$\text{Photo response non-uniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \ [\%]$$

Spectral response (without window)*11

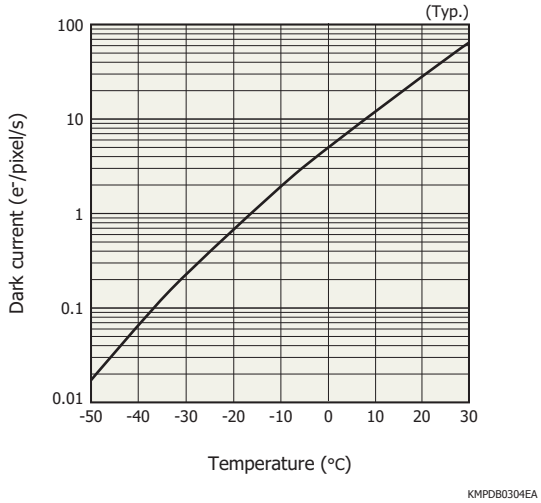


Spectral transmittance characteristic of window material



*11: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

Dark current vs. temperature



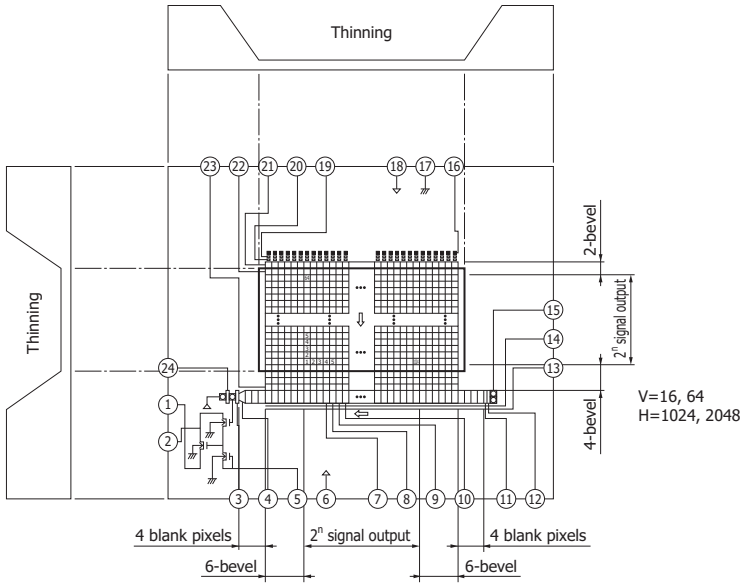
Window material

Type No.	Window material
S10420 series S11071 series	Quartz glass*12 (option: window-less)

*12: Resin sealing

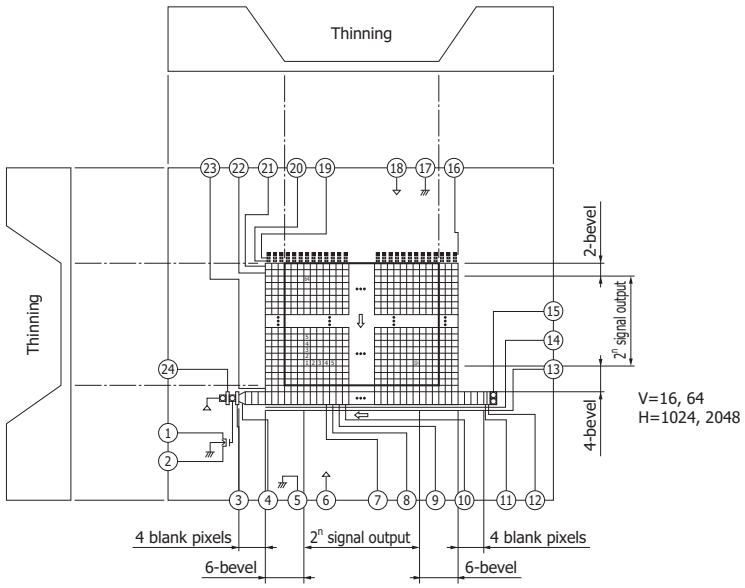
Device structure (conceptual drawing of top view in dimensional outline)

S11071 series



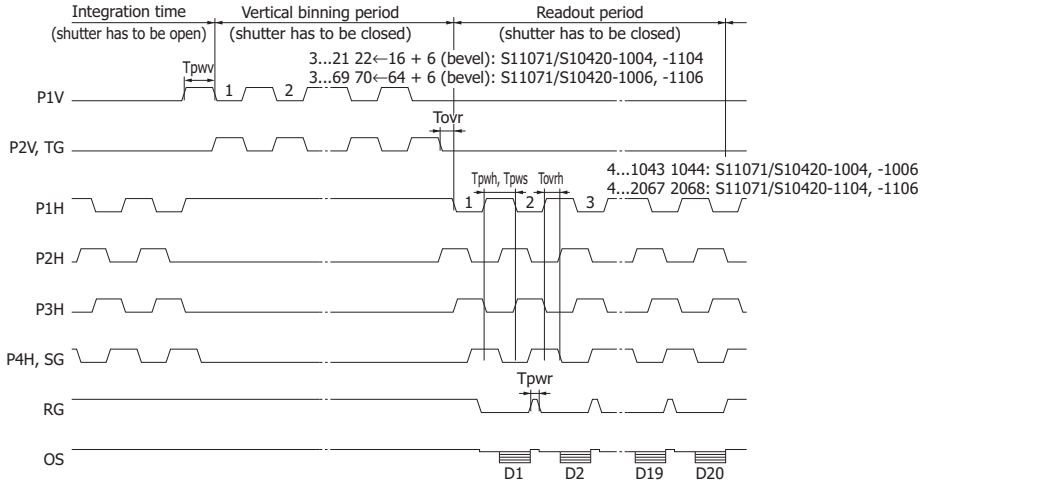
KMPDC0343EA

S10420 series



KMPDC0269EB

Timing chart (line binning)

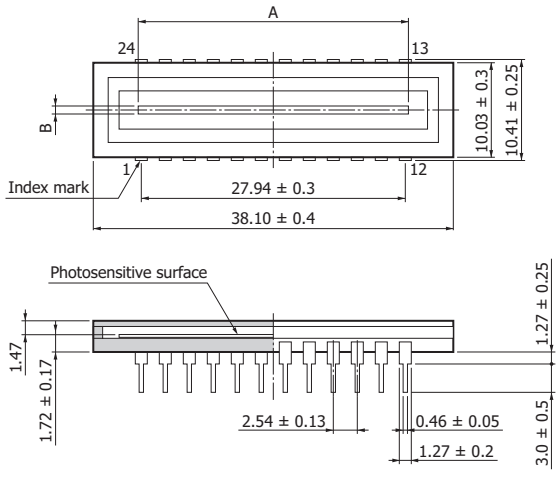


KMPDC0270EC

Parameter		Symbol	S11071 series			S10420 series			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
P1V, P2V, TG	Pulse width *13	Tpwv	6	8	-	6	8	-	µs
	Rise and fall time *13	Tprv, Tpfv	20	-	-	20	-	-	ns
P1H, P2H, P3H, P4H	Pulse width *13	Tpwh	50	100	-	1000	2000	-	ns
	Rise and fall time *13	Tprh, Tpfh	10	-	-	10	-	-	ns
	Pulse overlap time	Tovrh	25	50	-	500	1000	-	ns
	Duty ratio *13	-	40	50	60	40	50	60	%
SG	Pulse width *13	Tpws	50	100	-	1000	2000	-	ns
	Rise and fall time *13	Tprs, Tpfs	10	-	-	10	-	-	ns
	Pulse overlap time	Tovrh	25	50	-	500	1000	-	ns
	Duty ratio *13	-	40	50	60	40	50	60	%
RG	Pulse width	Tpwr	5	50	-	100	1000	-	ns
	Rise and fall time	Tprr, Tpfr	5	-	-	5	-	-	ns
TG-P1H	Overlap time	Tovr	1	2	-	1	2	-	µs

*13: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

Dimensional outline (unit: mm)



Type No.		Active area	
		A	B
S11071/ S10420	-1004(-01)	14.336 (H)	0.224 (V)
	-1006(-01)	14.336 (H)	0.896 (V)
	-1104(-01)	28.672 (H)	0.224 (V)
	-1106(-01)	28.672 (H)	0.896 (V)

KMPDA0223EB

Pin connections

S11071 series

Pin No.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	R_L=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	Vret	Output amplifier return	+1 V
6	RD	Reset drain	+15 V
7	P4H	CCD horizontal register clock-4	
8	P3H	CCD horizontal register clock-3	
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	-8 V
12	IG1H	Test point (horizontal input gate-1)	-8 V
13	OFG	Over flow gate	+13 V
14	OFD	Over flow drain	+12 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	ISV	Test point (vertical input source)	Connect to RD
17	SS	Substrate	GND
18	RD	Reset drain	+15 V
19	IG2V	Test point (vertical input gate-2)	-8 V
20	IG1V	Test point (vertical input gate-1)	-8 V
21	P2V	CCD vertical register clock-2	
22	P1V	CCD vertical register clock-1	
23	TG	Transfer gate	Same pulse as P2V
24	RG	Reset gate	

S10420 series

Pin No.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	R_L=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	P4H	CCD horizontal register clock-4	
8	P3H	CCD horizontal register clock-3	
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	-8 V
12	IG1H	Test point (horizontal input gate-1)	-8 V
13	OFG	Over flow gate	+12 V
14	OFD	Over flow drain	+12 V
15	ISH	Test point (horizontal input source)	Connect to RD
16	ISV	Test point (vertical input source)	Connect to RD
17	SS	Substrate	GND
18	RD	Reset drain	+12 V
19	IG2V	Test point (vertical input gate-2)	-8 V
20	IG1V	Test point (vertical input gate-1)	-8 V
21	P2V	CCD vertical register clock-2	
22	P1V	CCD vertical register clock-1	
23	TG	Transfer gate	Same pulse as P2V
24	RG	Reset gate	

Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Driver circuits for CCD image sensor (S10420/S11071 series) C11287/C11288 [sold separately]

The C11287, C11288 are driver circuits designed for HAMAMATSU CCD image sensors S10420/S11071 series. The C11287, C11288 can be used in spectrometers, etc. when combined with the CCD image sensor.

Features

- **Built-in 14-bit A/D converter**
- **Interface to computer: USB 2.0**
- **Power supply: USB bus power operation (C11287)**
  DC+5 V operation (C11288)

C11287

C11288

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