SaRonix™
A PERICOM® COMPANY

S1703 Series

3.3V CMOS SMD Crystal Clock Oscillator (XO)

Actual Size = 7 x 5mm

Product Features

- 3.3V CMOS compatible logic levels
- Pin-compatible with standard 7x5mm packages
- Designed for standard reflow and washing techniques
- Pb-free and RoHS/Green compliant available (seam seal package only)

Product Description

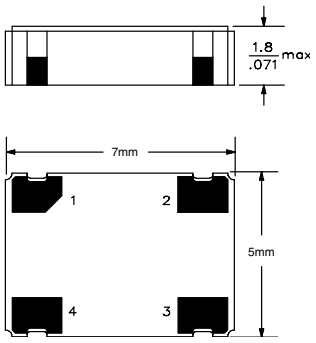
The S1703 Series is a 3.3V crystal clock oscillator. The output clock signal is compatible with CMOS logic levels. The device, available on tape and reel, is contained in a 7x5mm surface-mount ceramic package.

Applications

The S1703 Series is an ideal reference clock for SMT applications including:

- PC, notebook/palmtop computers
- Portable Applications
- PCMCIA cards and HDD

Packaging Outline



Pin Functions

Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V_{DD}

Common Frequencies

Contact SaRonix for additional frequencies

3.6864 MHz	24.5760 MHz	48.0000 MHz
8.0000 MHz	25.0000 MHz	50.0000 MHz
10.0000 MHz	32.0000 MHz	60.0000 MHz
14.3181 MHz	32.7680 MHz	66.0000 MHz
16.0000 MHz	33.0000 MHz	66.6667 MHz
18.4320 MHz	35.3280 MHz	75.0000 MHz
20.0000 MHz	40.0000 MHz	

Ordering Information

S 1703 B - 25.0000 (T) -G

- **SaRonix**
- **Product Series**
- **Frequency Stability**
  - B = ±50 ppM (0 to 70 °C)
  - C = ±100 ppM (0 to +70°C)
- **Output Frequency** (MHz)
- **Packaging**
  - (T) = Tape & Reel full reel increments
  - Blank = Bulk packaged
- G = Glass-frit package, limited availability.
  Blank = Standard seam-seal package as depicted.*

*Note: Legacy glass frit package may continue to ship until inventory is depleted. See S1613 series to guarantee seam seal package.

Electrical Performance

Parameter		Min.	Typ.	Max.	Units	Notes
Output frequency		1.8432		80	MHz	As specified
Supply voltage		+2.97	+3.3	+3.63	V DC	
Supply current, output enabled				15	mA	1.8432 to 34.0 MHz
				25		> 34 to 50.0 MHz
				40		> 50 to 80.0 MHz
Supply current, standby mode				10	µA	Output Hi-Z
Frequency stability				±50 to ±100	ppM	See Note 1 below
Operating temperature		0		+70	°C	
Output logic 0, VOL				10% V_{DD}	V	
Output logic 1, VOH		90% V_{DD}			V	
Output load				30	pF	
Duty cycle		45		55	%	0 to +70°C measured 50%VDD
Rise and fall time	1.8432 to 64.0000 MHz			10	ns	measured 20/80% of waveform
	64.0001 to 66.667 MHz			6		
	66.667 to 80.0000 MHz			5		
Jitter, Phase				1.5	PS RMS (1 - σ)	10kHz ~ 20MHz Frequency Band
Jitter, Accumulated				5	PS RMS (1 - σ)	20,000 adjacent periods
Jitter, Total				50	PS pK - pK	100,000 periods

Notes:
1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

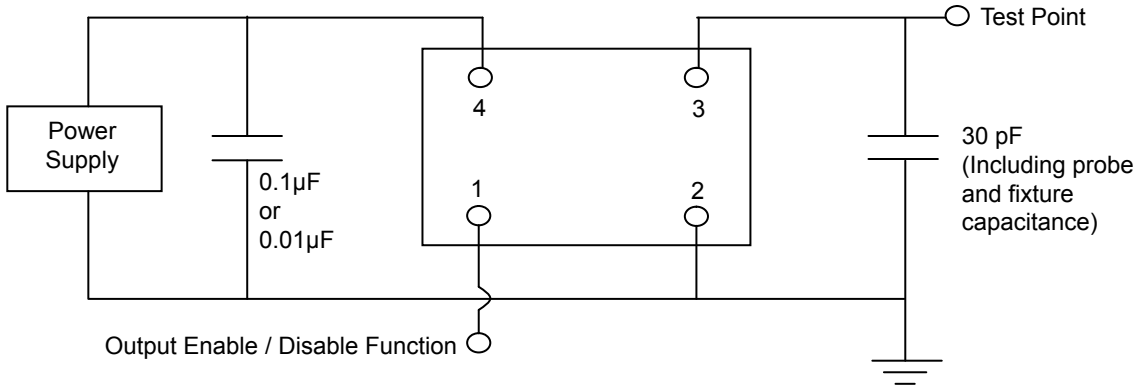
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	2.2			V	or open
Input voltage (pin 1), Output Disable (low power standby)			0.5	V	Output is Hi-Z
Internal pullup resistance	50			kΩ	
Output disable delay			150	ns	
Output enable delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

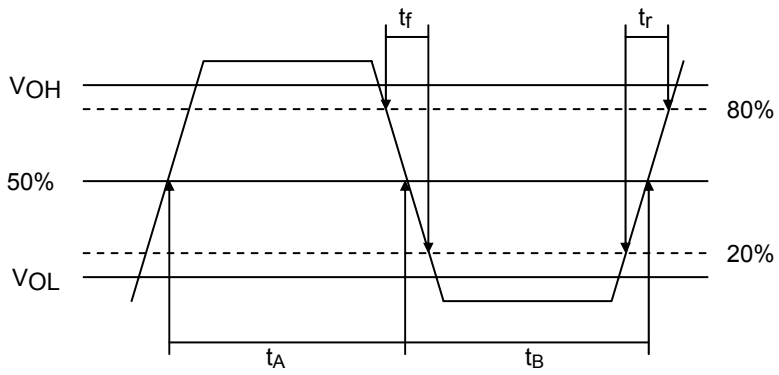


Reliability Test Ratings

This product is rated to meet the following test conditions (Applies to seam-seal package only):

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2x10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

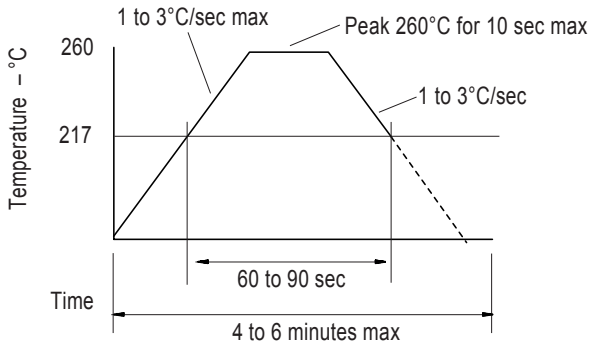
Output Waveform



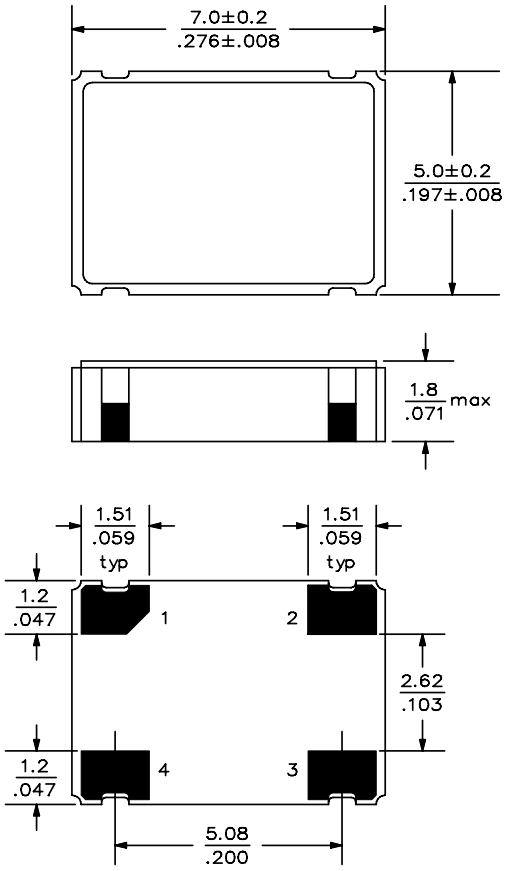
Duty cycle = 100% × (t_A) / (t_A + t_B)

Reflow Soldering Profile

As per IPC/JEDEC J-STD-020C

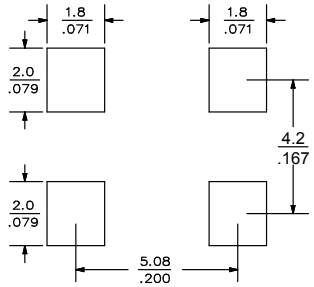


Mechanical Drawings



Note: Seam seal package is depicted. Legacy glass-frit package has limited availability, please inquire if needed.

Recommended Land Pattern*



*External high-frequency power decoupling is recommended.(see test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions are in mm/inches.

Marking LINE 1: **S3X YY WWX** **(SaRonix, Model, Stability, Year, Week, Origin)**
Marking LINE 2: **Frequency**

**Exact location of markings may vary.