

TLC5925 Low-Power 16-Channel Constant-Current LED Sink Driver

1 Features

- 16 Constant-Current Output Channels
- Constant Output Current Invariant to Load Voltage Change
- Excellent Output Current Accuracy:
 - Between Channels: $< \pm 4\%$ (Max)
 - Between ICs: $< \pm 6\%$ (Max)
- Constant Output Current Range: 3 mA to 45 mA
- Output Current Adjusted By External Resistor
- Fast Response of Output Current, $\overline{OE}$ (Min): 100 ns
- 30-MHz Clock Frequency
- Schmitt-Trigger Inputs
- 3.3-V to 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection
- ESD Performance: 1-kV HBM

2 Applications

- Gaming Machine and Entertainment
- General LED Applications
- LED Display Systems
- Signs LED Lighting
- White Goods

3 Description

The TLC5925 is designed for LED displays and LED lighting applications. The TLC5925 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5925 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (such as, LED panels), the TLC5925 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, R_{EXT} , which gives flexibility in controlling the light intensity of LEDs. TLC5925 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The serial data is transferred into TLC5925 via SDI, shifted in the shift register, and transferred out via SDO. LE can latch the serial data in the shift register to the output latch. $\overline{OE}$ enables the output drivers to sink current.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5925	SSOP (24)	8.65 mm × 3.90 mm
	SOIC (24)	15.40 mm × 7.50 mm
	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

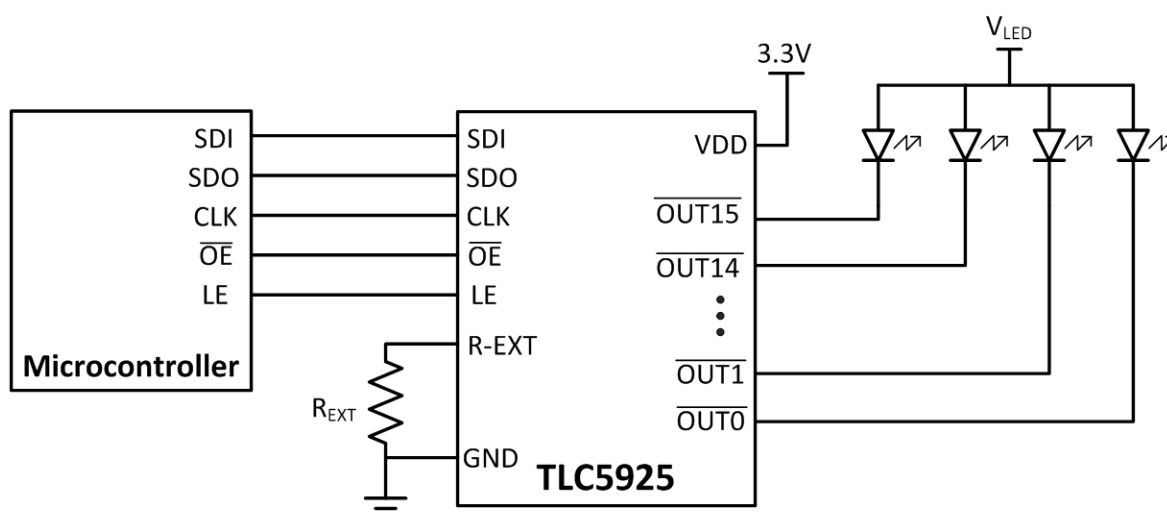


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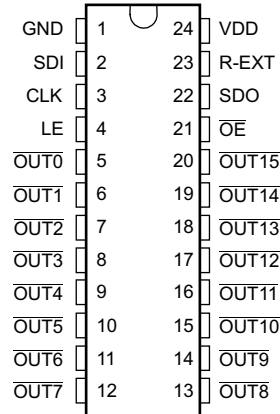
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B	Page
Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Pin Configuration and Functions

**DBQ, DW, or PWP Package
24-Pin SSOP, SOIC, or TSSOP
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK	3	I	Clock input for data shift on rising edge
GND	1	—	Ground for control logic and current sink
LE	4	I	Data strobe input Serial data is transferred to the respective latch when LE is high. The data is latched when LE goes low. LE has an internal pull-down resistor.
$\overline{OE}$	21	I	Output enable When $\overline{OE}$ is active (low), the output drivers are enabled. When $\overline{OE}$ is high, all output drivers are turned OFF (blanked). $\overline{OE}$ has an internal pullup resistor.
$\overline{OUT0}$	5	O	Constant-current outputs
$\overline{OUT1}$	6		
$\overline{OUT2}$	7		
$\overline{OUT3}$	8		
$\overline{OUT4}$	9		
$\overline{OUT5}$	10		
$\overline{OUT6}$	11		
$\overline{OUT7}$	12		
$\overline{OUT8}$	13		
$\overline{OUT9}$	14		
$\overline{OUT10}$	15		
$\overline{OUT11}$	16		
$\overline{OUT12}$	17		
$\overline{OUT13}$	18		
$\overline{OUT14}$	19		
$\overline{OUT15}$	20		
R-EXT	23	I	Input used to connect an external resistor (R_{ext}) for setting output currents
SDI	2	I	Serial-data input to the Shift register
SDO	22	O	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	24	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	0	7	V
V _I	Input voltage	−0.4	V _{DD} + 0.4	V
V _O	Output voltage	−0.5	20	V
I _{OUT}	Output current		45	mA
I _{GND}	GND terminal current		750	mA
T _A	Free-air operating temperature range	−40	125	°C
T _J	Operating junction temperature range	−40	150	°C
T _{stg}	Storage temperature range	−55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{DD}	Supply voltage		3	5.5	V
V _O	Output voltage	OUT0 to OUT15		17	V
I _O	Output current	DC test circuit	V _O ≥ 0.6 V	3	mA
			V _O ≥ 1 V	45	
I _{OH}	High-level output current	SDO	−1		mA
I _{OL}	Low-level output current	SDO	1		mA
V _{IH}	High-level input voltage	CLK, $\overline{\text{OE}}$, LE, and SDI	0.7 × V _{DD}	V _{DD}	V
V _{IL}	Low-level input voltage	CLK, $\overline{\text{OE}}$, LE, and SDI	GND	0.3 × V _{DD}	V
t _R	Rise Time	CLK		500	ns
t _F	Fall Time	CLK		500	ns

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾			TLC5925			UNIT
			DBQ (SSOP)	DW (SOIC)	PW (TSSOP)	
			24 PINS	24 PINS	24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	Mounted on JEDEC 1-layer board (JESD 51-3), No airflow	99.8	80.5	118.8	°C/W
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow	61	45.5	87.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance		52.9	45.0	44.9	°C/W
R _{θJB}	Junction-to-board thermal resistance		41.5	44.8	52.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter		16.4	21.7	6.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter		41.2	44.4	52.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance		n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{DD}	Input voltage		3		5.5	V
V _O	Output voltage				17	V
I _O	Output current	V _O ≥ 0.6 V	3			mA
		V _O ≥ 1 V			45	
I _{OH}	High-level output current, source		-1			mA
I _{OL}	Low-level output current, sink		1			
V _{IH}	High-level input voltage		0.7 × V _{DD}		V _{DD}	V
V _{IL}	Low-level input voltage		GND		0.3 × V _{DD}	
I _{leak}	Output leakage current	V _{OH} = 17 V	T _J = 25°C		0.5	μA
			T _J = 125°C		2	
V _{OH}	High-level output voltage	SDO, I _{OL} = –1 mA	V _{DD} – 0.4			V
V _{OL}	Low-level output voltage	SDO, I _{OH} = 1 mA			0.4	V
I _{O(1)}	Output current 1	V _{OUT} = 0.6 V, R _{ext} = 1680 Ω	13			mA
	Output current error, die-die	I _{OL} = 13 mA, V _O = 0.6 V, R _{ext} = 1680 Ω, T _J = 25°C	±3%		±6%	
	Output current error, channel-to-channel	I _{OL} = 13 mA, V _O = 0.6 V, R _{ext} = 1680 Ω, T _J = 25°C	±1.5%		±4%	
I _{O(2)}	Output current 2	V _O = 0.8 V, R _{ext} = 840 Ω	26			mA
	Output current error, die-die	I _{OL} = 26 mA, V _O = 0.8 V, R _{ext} = 840 Ω, T _J = 25°C	±3%		±6%	
	Output current error, channel-to-channel	I _{OL} = 26 mA, V _O = 0.8 V, R _{ext} = 840 Ω, T _J = 25°C	±1.5%		±4%	
I _{OUT} vs V _{OUT}	Output current vs output voltage regulation	V _O = 1 V to 3 V, I _O = 13 mA	±0.1			%V
		V _{DD} = 3.0 V to 5.5 V, I _O = 13 mA to 45 mA	±1			
	Pullup resistance	$\overline{\text{OE}}$	500			kΩ
	Pulldown resistance	LE	500			kΩ
T _{sd}	Overtemperature shutdown ⁽¹⁾		150	175	200	°C
T _{hys}	Restart temperature hysteresis		15			°C
I _{DD}	Supply current	R _{ext} = Open	7		10	mA
		R _{ext} = 1680 Ω	9		12	
		R _{ext} = 840 Ω	11		13	
C _{IN}	Input capacitance	V _I = V _{DD} or GND, CLK, SDI, SDO, $\overline{\text{OE}}$			10	pF

(1) Specified by design

6.6 Electrical Characteristics: $V_{DD} = 5.5\text{ V}$

 $V_{DD} = 5.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input voltage		3		5.5	V
V_O	Output voltage				17	V
I_O	Output current	$V_O \geq 0.6\text{ V}$	3			mA
		$V_O \geq 1\text{ V}$			45	
I_{OH}	High-level output current, source		-1			mA
I_{OL}	Low-level output current, sink		1			
V_{IH}	High-level input voltage		$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage		GND		$0.3 \times V_{DD}$	
I_{leak}	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	μA
			$T_J = 125^\circ\text{C}$		2	
V_{OH}	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V
V_{OL}	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$, $R_{ext} = 1680\ \Omega$	13			mA
	Output current error, die-die	$I_{OL} = 13\text{ mA}$, $V_O = 0.6\text{ V}$, $R_{ext} = 1680\ \Omega$, $T_J = 25^\circ\text{C}$	$\pm 3\%$		$\pm 6\%$	
	Output current error, channel-to-channel	$I_{OL} = 13\text{ mA}$, $V_O = 0.6\text{ V}$, $R_{ext} = 1680\ \Omega$, $T_J = 25^\circ\text{C}$	$\pm 1.5\%$		$\pm 4\%$	
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$, $R_{ext} = 840\ \Omega$	26			mA
	Output current error, die-die	$I_{OL} = 26\text{ mA}$, $V_O = 0.8\text{ V}$, $R_{ext} = 840\ \Omega$, $T_J = 25^\circ\text{C}$	$\pm 3\%$		$\pm 6\%$	
	Output current error, channel-to-channel	$I_{OL} = 26\text{ mA}$, $V_O = 0.8\text{ V}$, $R_{ext} = 840\ \Omega$, $T_J = 25^\circ\text{C}$	$\pm 1.5\%$		$\pm 4\%$	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to 3 V , $I_O = 26\text{ mA}$	± 0.1			%V
		$V_{DD} = 3.0\text{ V}$ to 5.5 V , $I_O = 13\text{ mA}$ to 45 mA	± 1			
	Pullup resistance	$\overline{OE}$	500			k Ω
	Pulldown resistance	LE	500			k Ω
T_{sd}	Overtemperature shutdown ⁽¹⁾		150	175	200	$^\circ\text{C}$
T_{hys}	Restart temperature hysteresis		15			$^\circ\text{C}$
I_{DD}	Supply current	$R_{ext} = \text{Open}$	9		11	mA
		$R_{ext} = 1680\ \Omega$	12		14	
		$R_{ext} = 840\ \Omega$	14		16	
C_{IN}	Input capacitance	$V_I = V_{DD}$ or GND, CLK, SDI, SDO, $\overline{OE}$			10	pF

(1) Specified by design

6.7 Power Dissipation and Thermal Impedance

			MIN	MAX	UNIT
P_D	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, $T_A = 25^\circ\text{C}$, $T_J = 125^\circ\text{C}$	DBQ package	1.6	W
			DW package	2.2	
			PW package	1.1	

6.8 Timing Requirements

 $V_{DD} = 3\text{ V to }5.5\text{ V}$ (unless otherwise noted)

		MIN	MAX	UNIT
$t_{w(L)}$	LE pulse duration	15		ns
$t_{w(CLK)}$	CLK pulse duration	15		ns
$t_{w(OE)}$	$\overline{OE}$ pulse duration	300		ns
$t_{su(D)}$	Setup time for SDI	3		ns
$t_{h(D)}$	Hold time for SDI	2		ns
$t_{su(L)}$	Setup time for LE	5		ns
$t_{h(L)}$	Hold time for LE	5		ns
f_{CLK}	Clock frequency, Cascade operation		30	MHz

6.9 Switching Characteristics: $V_{DD} = 3\text{ V}$

 $V_{DD} = 3\text{ V}$, $T_J = -40^\circ\text{C to }125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	30	45	60	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$	30	45	60	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$	30	45	60	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		30	40	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$	40	65	100	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$	40	65	100	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$	40	65	100	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		30	40	ns
$t_{w(CLK)}$	Pulse duration, CLK	15			ns
$t_{w(L)}$	Pulse duration, LE	15			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$	300			ns
$t_{h(D)}$	Hold time, SDI	2			ns
$t_{su(D)}$	Setup time, SDI	3			ns
$t_{h(L)}$	Hold time, LE	5			ns
$t_{su(L)}$	Setup time, LE	5			ns
t_r	Rise time, CLK ⁽¹⁾			500	ns
t_f	Fall time, CLK ⁽¹⁾			500	ns
t_{or}	Rise time, outputs (off)	35	50	70	ns
t_{of}	Rise time, outputs (on)	15	50	120	ns
f_{CLK}	Clock frequency			30	MHz

 $V_{IH} = V_{DD}$, $V_{IL} = \text{GND}$,
 $R_{ext} = 840\ \Omega$, $V_L = 4\text{ V}$,
 $R_L = 88\ \Omega$, $C_L = 10\text{ pF}$

- (1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

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6.10 Switching Characteristics: $V_{DD} = 5.5\text{ V}$
 $V_{DD} = 5.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	$V_{IH} = V_{DD}$, $V_{IL} = \text{GND}$, $R_{ext} = 840\ \Omega$, $V_L = 4\text{ V}$, $R_L = 88\ \Omega$, $C_L = 10\text{ pF}$	20	35	55	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		20	35	55	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		20	35	55	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		15	28	42	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		15	28	42	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		15	28	42	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(\text{CLK})}$	Pulse duration, CLK		10			ns
$t_{w(L)}$	Pulse duration LE		10			ns
$t_{w(\text{OE})}$	Pulse duration, $\overline{OE}$		200			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK ⁽¹⁾				500	ns
t_f	Fall time, CLK ⁽¹⁾				500	ns
t_{or}	Rise time, outputs (off)		25	45	65	ns
t_{of}	Rise time, outputs (on)		7	12	20	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

- (1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

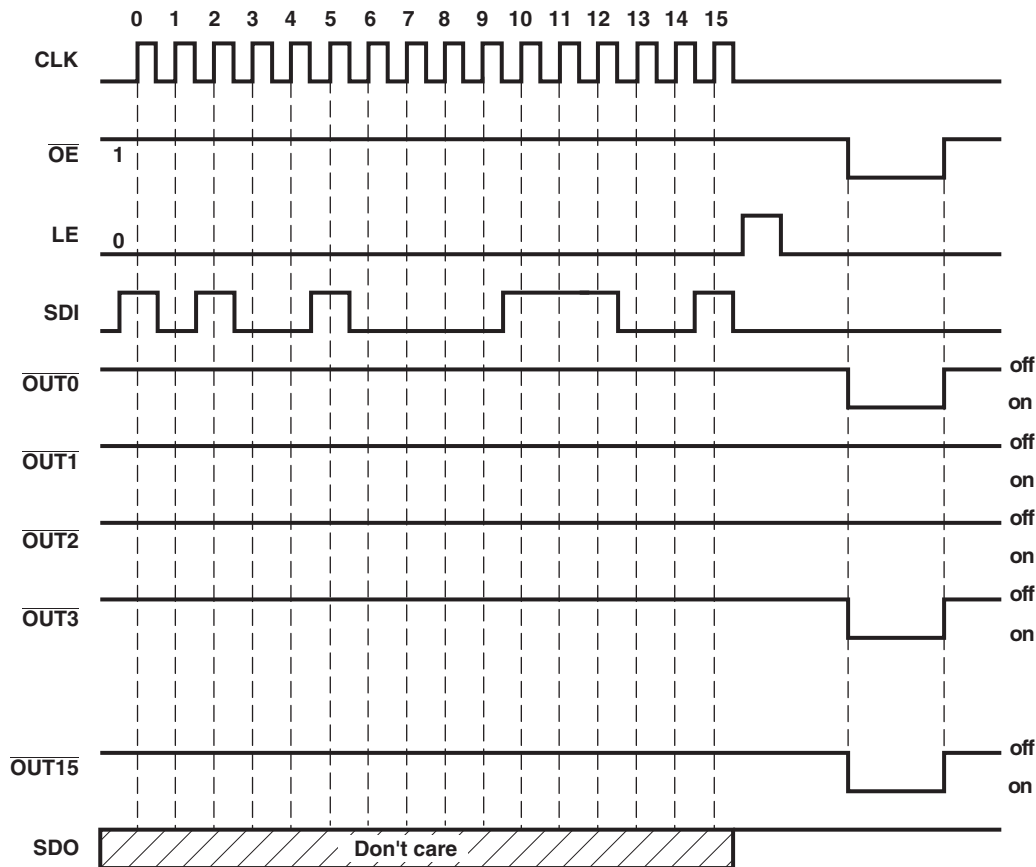


Figure 1. Timing Diagram

6.11 Typical Characteristics

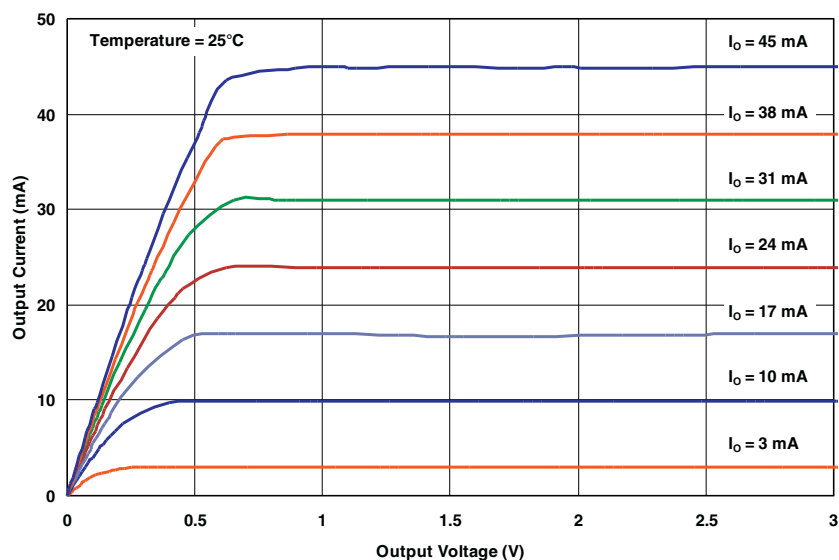


Figure 2. Output Current vs Output Voltage

7 Parameter Measurement Information

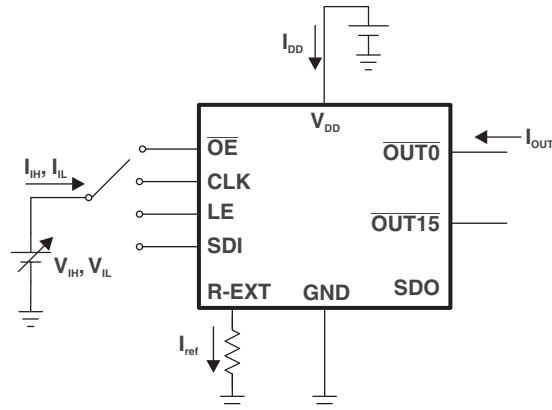


Figure 3. Test Circuit for Electrical Characteristics

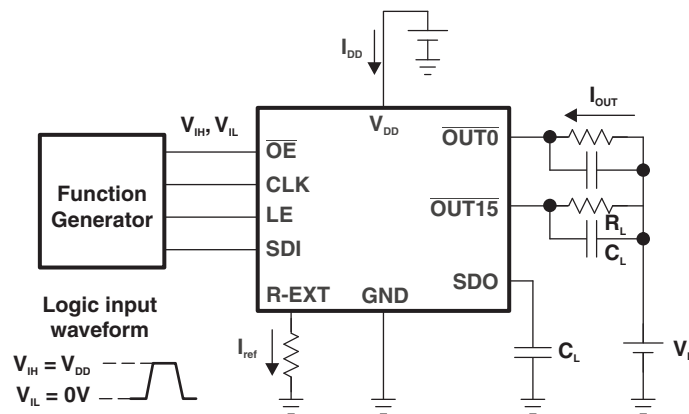


Figure 4. Test Circuit for Switching Characteristics

Parameter Measurement Information (continued)

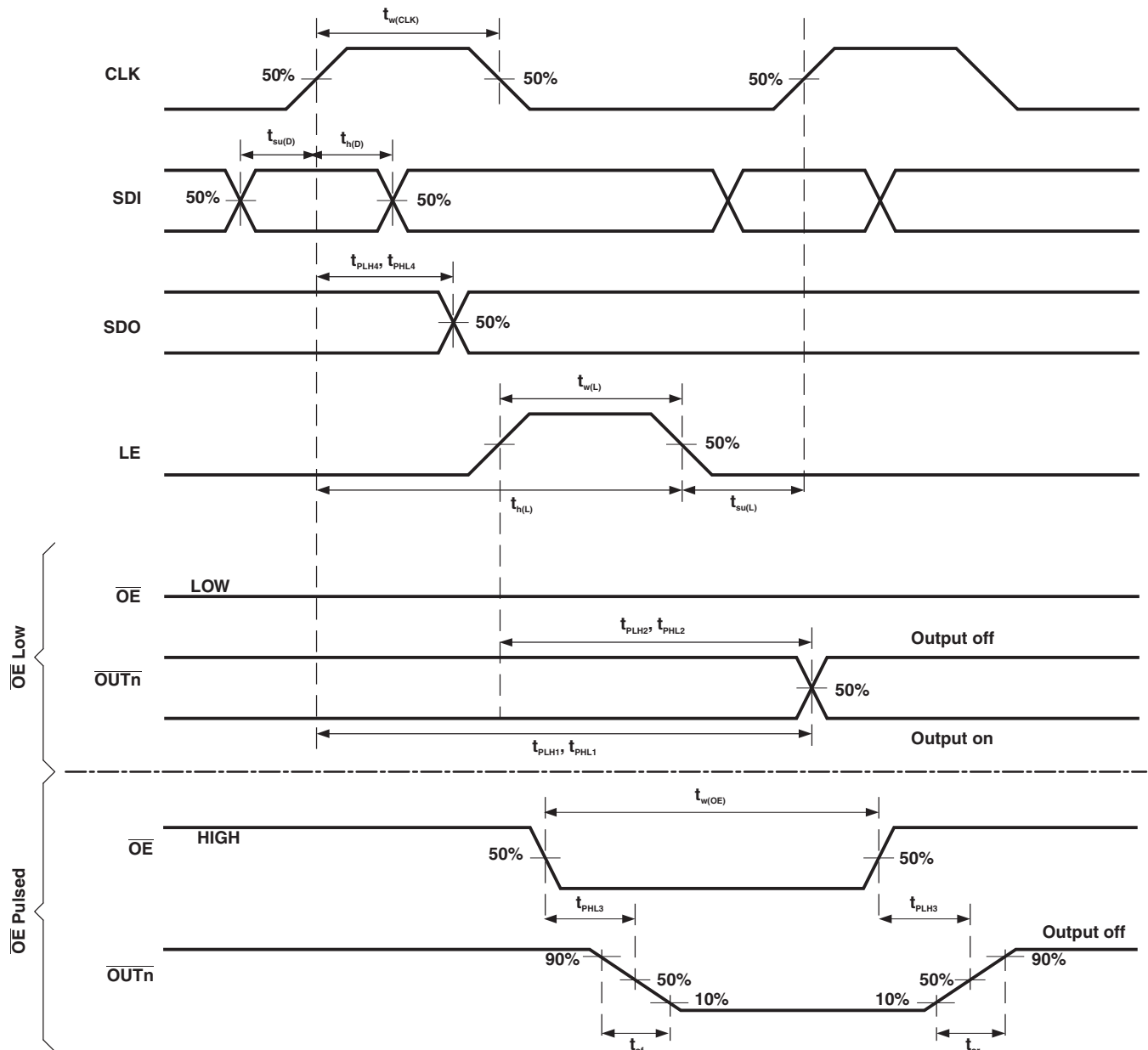


Figure 5. Normal Mode Timing Waveforms

8.4 Device Functional Modes

The table below lists the functional modes for the TLC5925.

Table 1. Truth Table in Normal Operation

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}...\overline{OUT15}...\overline{OUT15}$	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	H	Dn + 3	off	Dn – 13

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Turning on the LEDs

To turn on an LED connected to one of the outputs of the device, the output must be pulled low. To do this, the SDI signal must let the device know which outputs should be activated. Using the rising edge of CLK, the logic level of the SDI signal latches the desired state of each output into the shift register. Once this is complete, the LE signal must be toggled from low to high then back to low. Once /OE is pulled down, the corresponding outputs will be pulled low and the LEDs will be turned on. The below diagram shows outputs 0, 3, 4, 5, 10, 13, and 15 being activated.

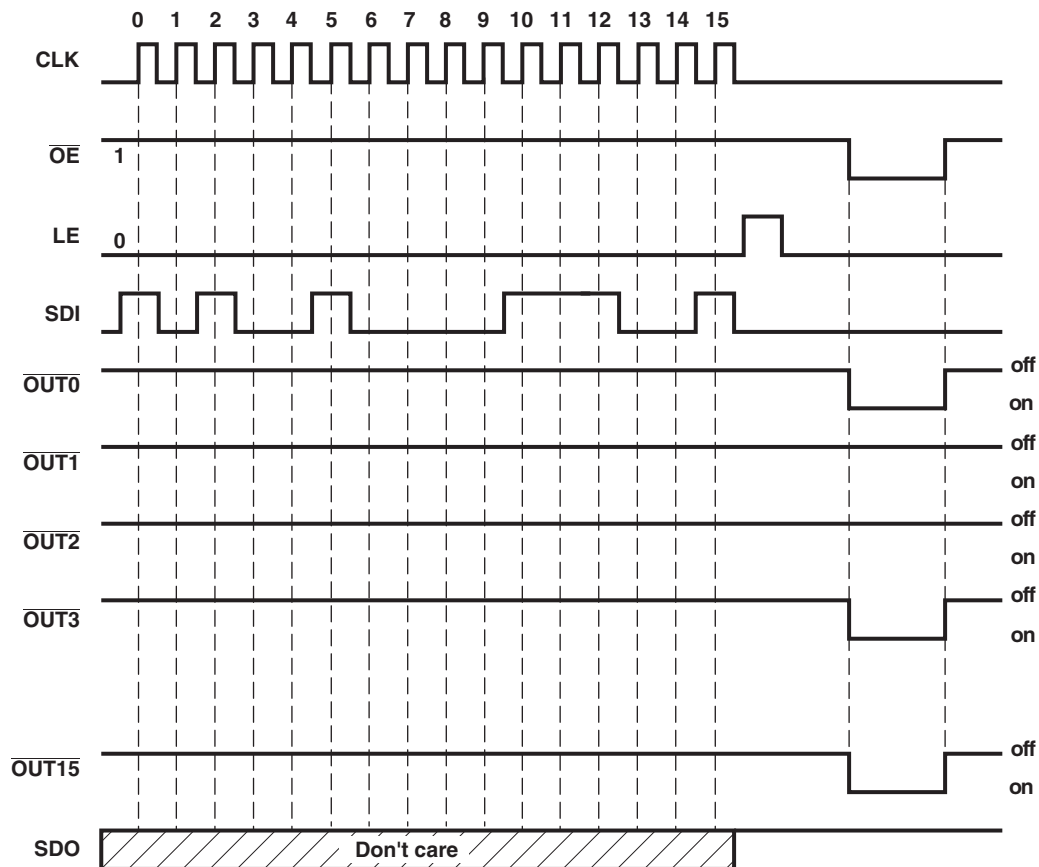


Figure 6. Timing Diagram

Application Information (continued)

9.1.2 Propagation Delay Times

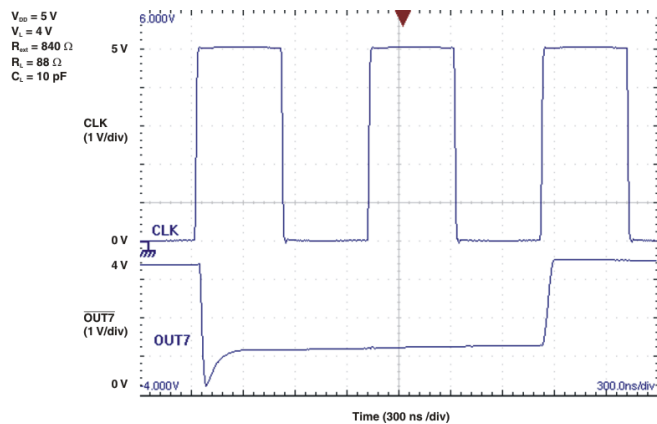


Figure 7. CLK to $\overline{\text{OUT7}}$

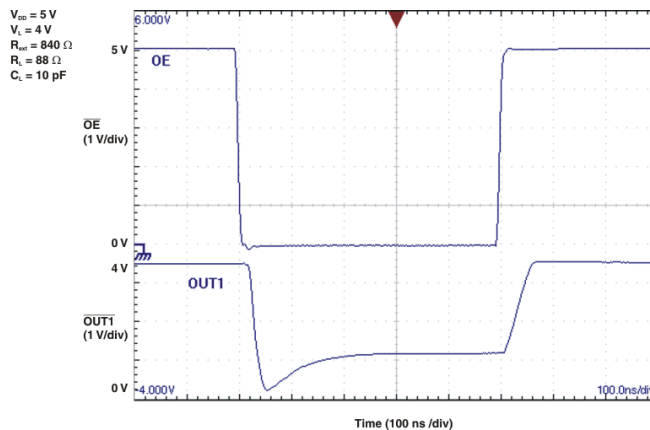


Figure 8. $\overline{\text{OE}}$ to $\overline{\text{OUT1}}$

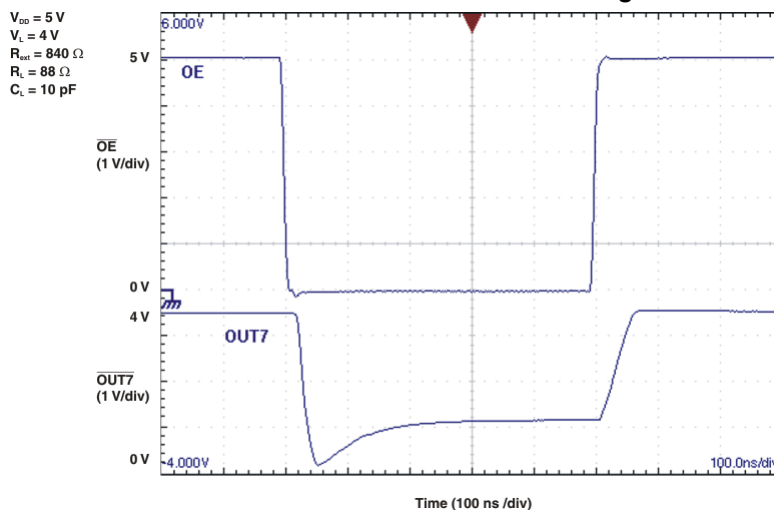
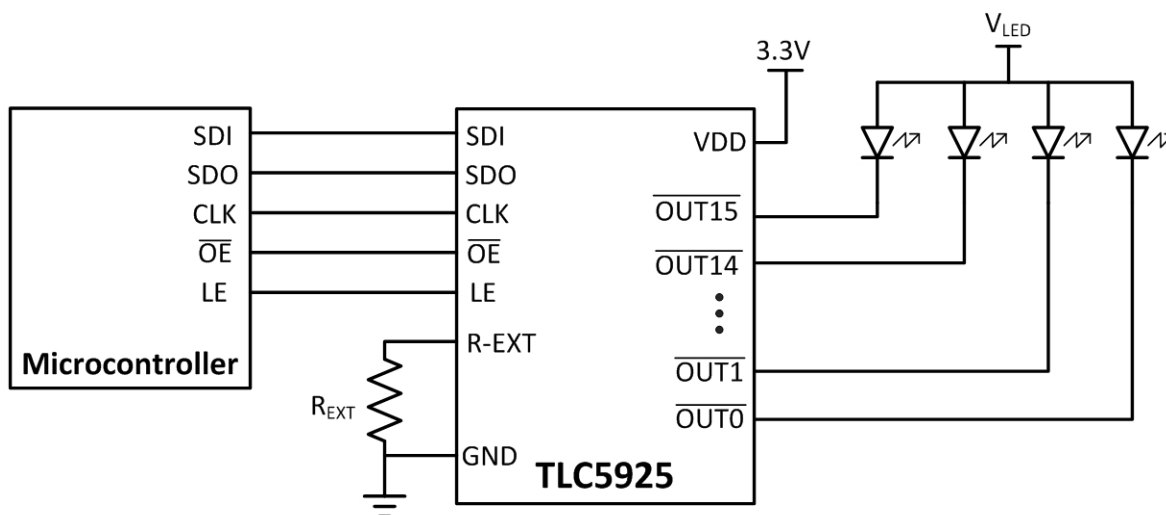


Figure 9. $\overline{\text{OE}}$ to $\overline{\text{OUT7}}$

9.2 Typical Application



Typical Application (continued)

9.2.1 Design Requirements

For the following design procedure, the input voltage (VDD) is between 3 V and 5.5 V.

9.2.2 Detailed Design Procedure

9.2.2.1 Adjusting Output Current

TLC5925 sets I_{OUT} based on the external resistor R_{ext} . Users can follow the below formulas to calculate the target output current $I_{OUT,target}$ in the saturation region:

$I_{OUT,target} = (1.21 \text{ V} / R_{ext}) \times 18$, where R_{ext} is the external resistance connected between R-EXT and GND.

Therefore, the default current is approximately 26 mA at 840 Ω and 13 mA at 1680 Ω .

9.2.3 Application Curve

The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in [Figure 10](#).

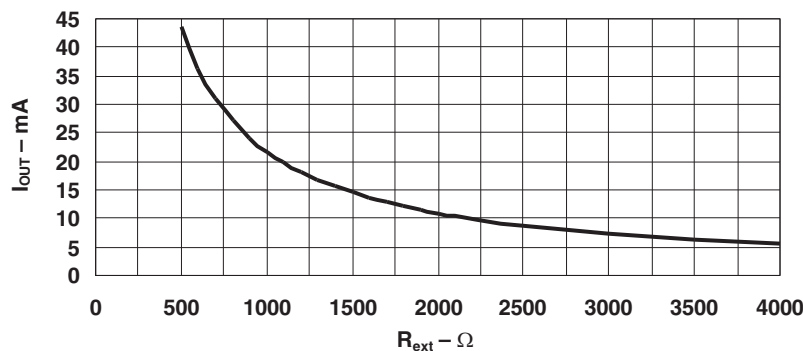


Figure 10. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

10 Power Supply Recommendations

The TLC5925 is designed to operate with a VDD range between 3 V and 5.5 V.

11 Layout

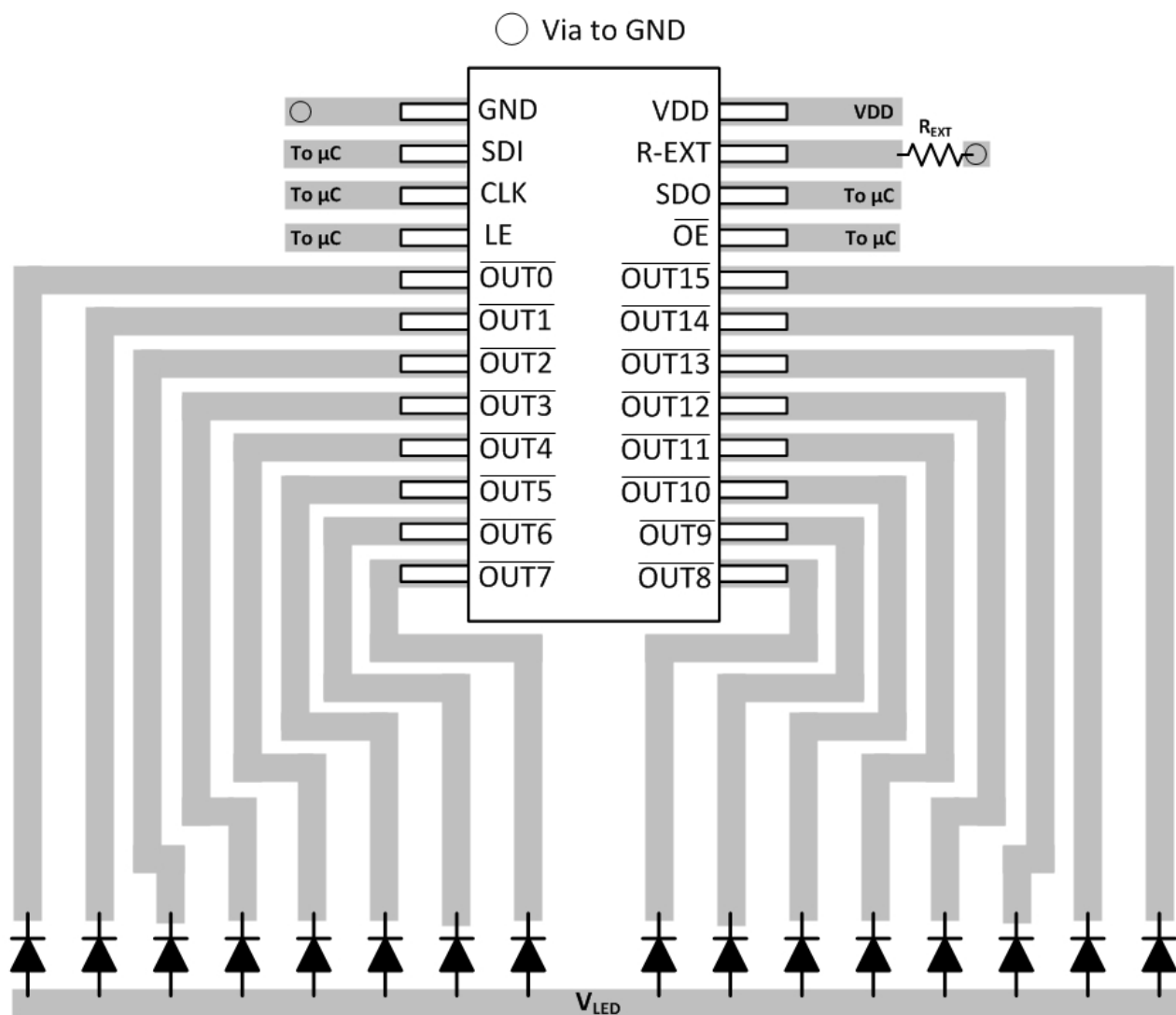
11.1 Layout Guidelines

The SDI, CLK, SDO, LE, and OE signals should all be kept from potential noise sources.

All traces carrying power through the LEDs should be wide enough to handle necessary currents.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground.

11.2 Layout Example



12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
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12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5925IDBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5925I	Samples
TLC5925IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5925I	Samples
TLC5925IDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5925I	Samples
TLC5925IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5925	Samples
TLC5925IPWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5925	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

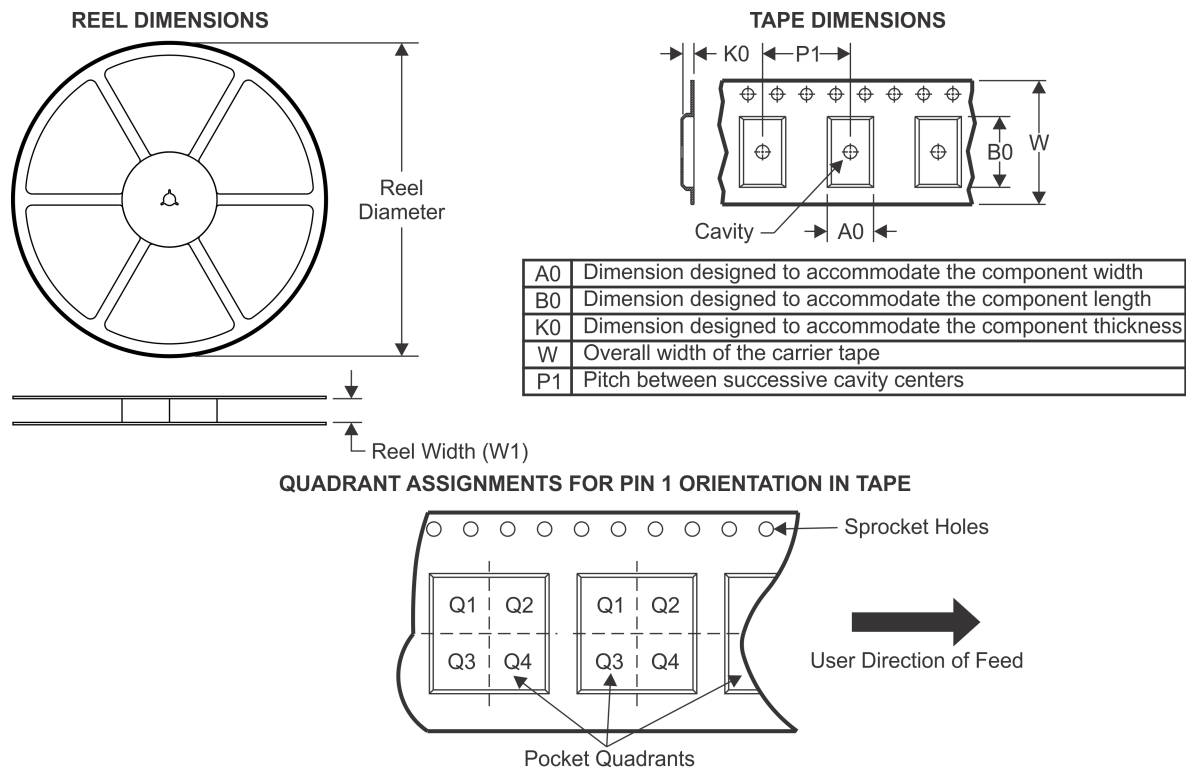
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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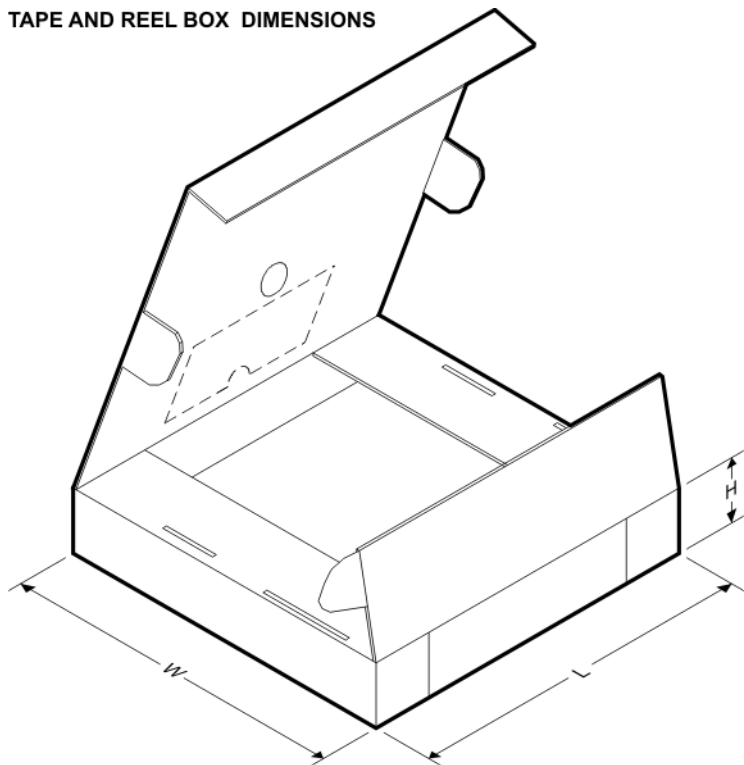
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5925IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5925IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

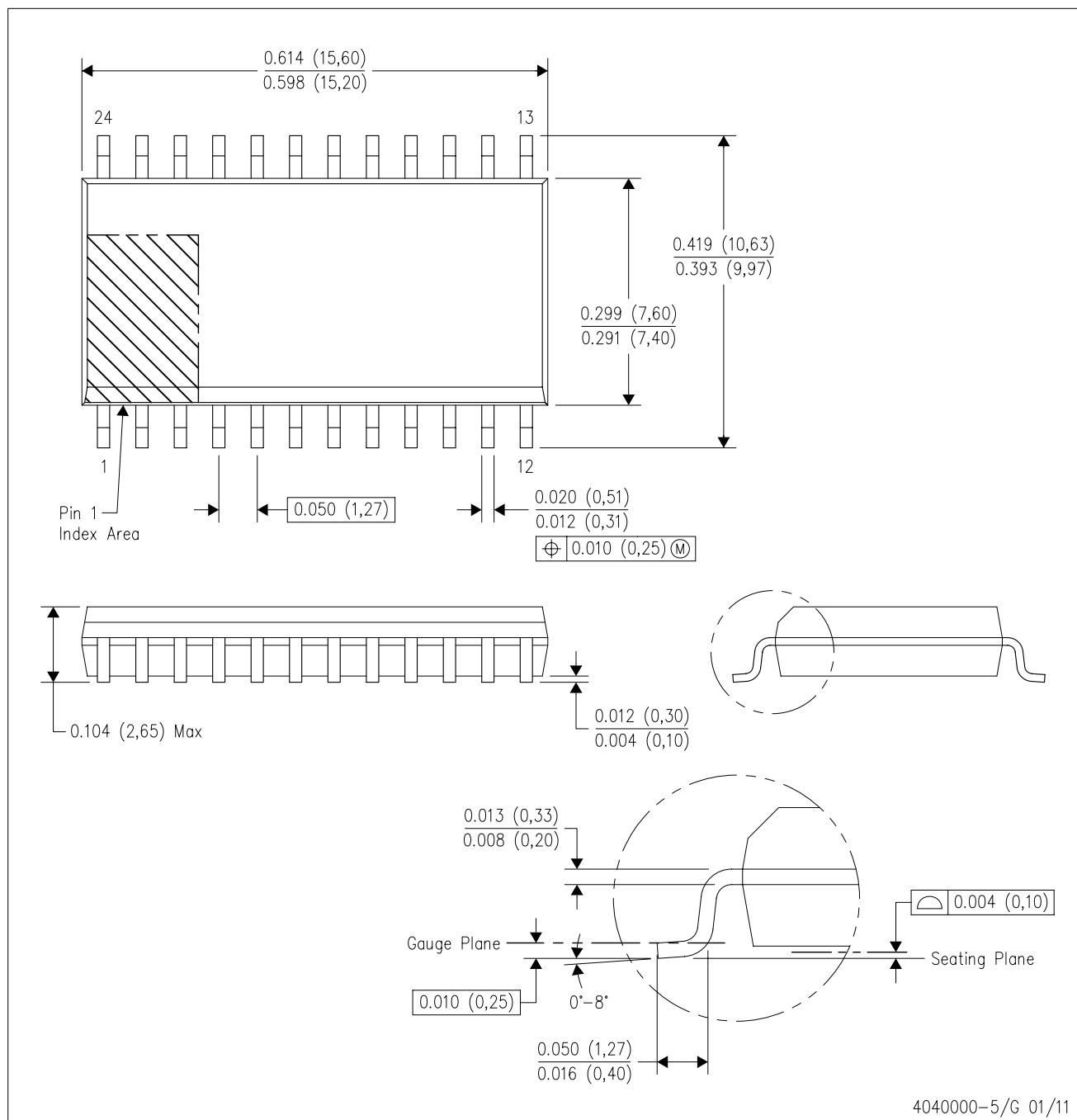


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5925IDBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC5925IDWR	SOIC	DW	24	2000	367.0	367.0	45.0

DW (R-PDSO-G24)

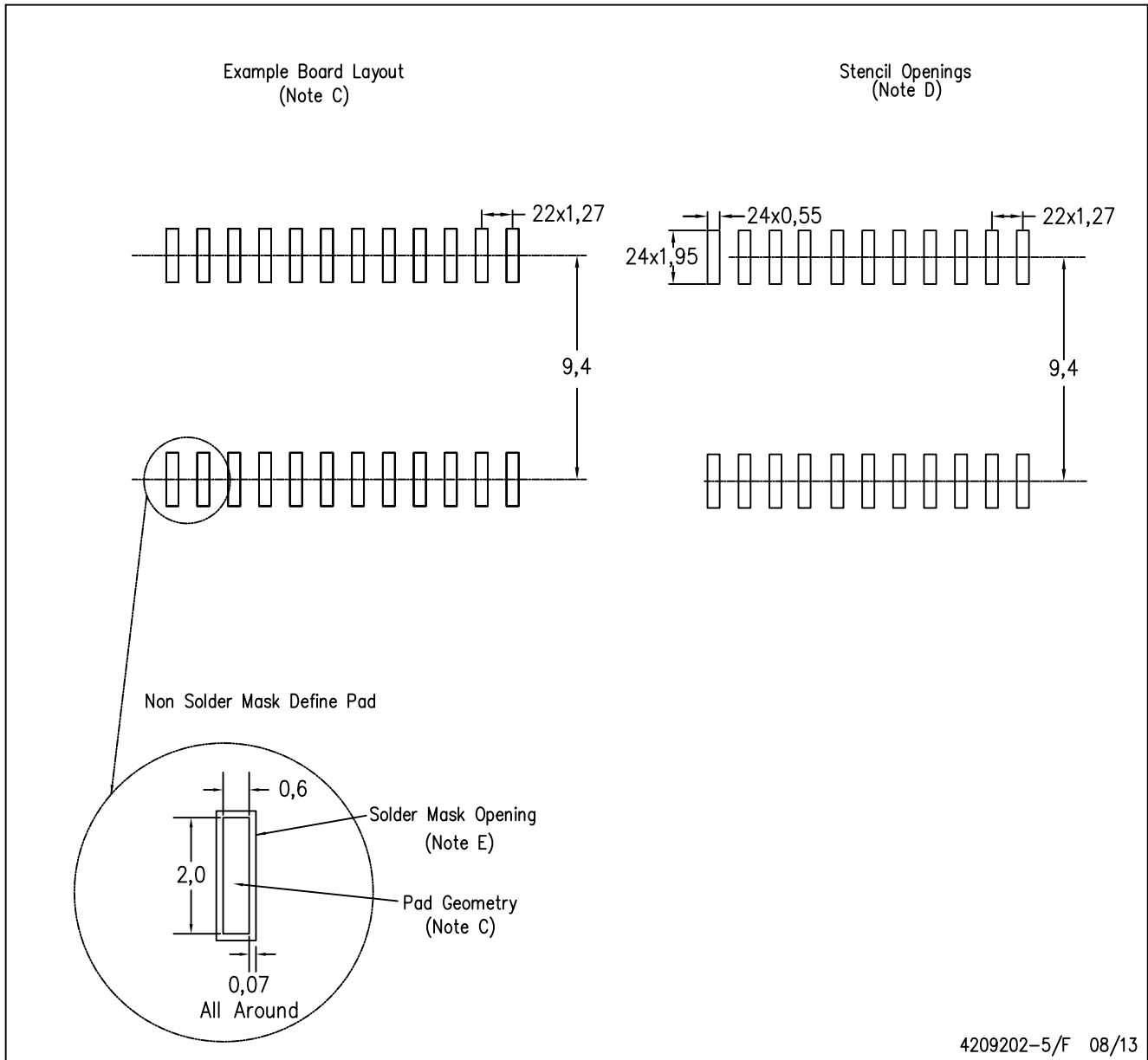
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

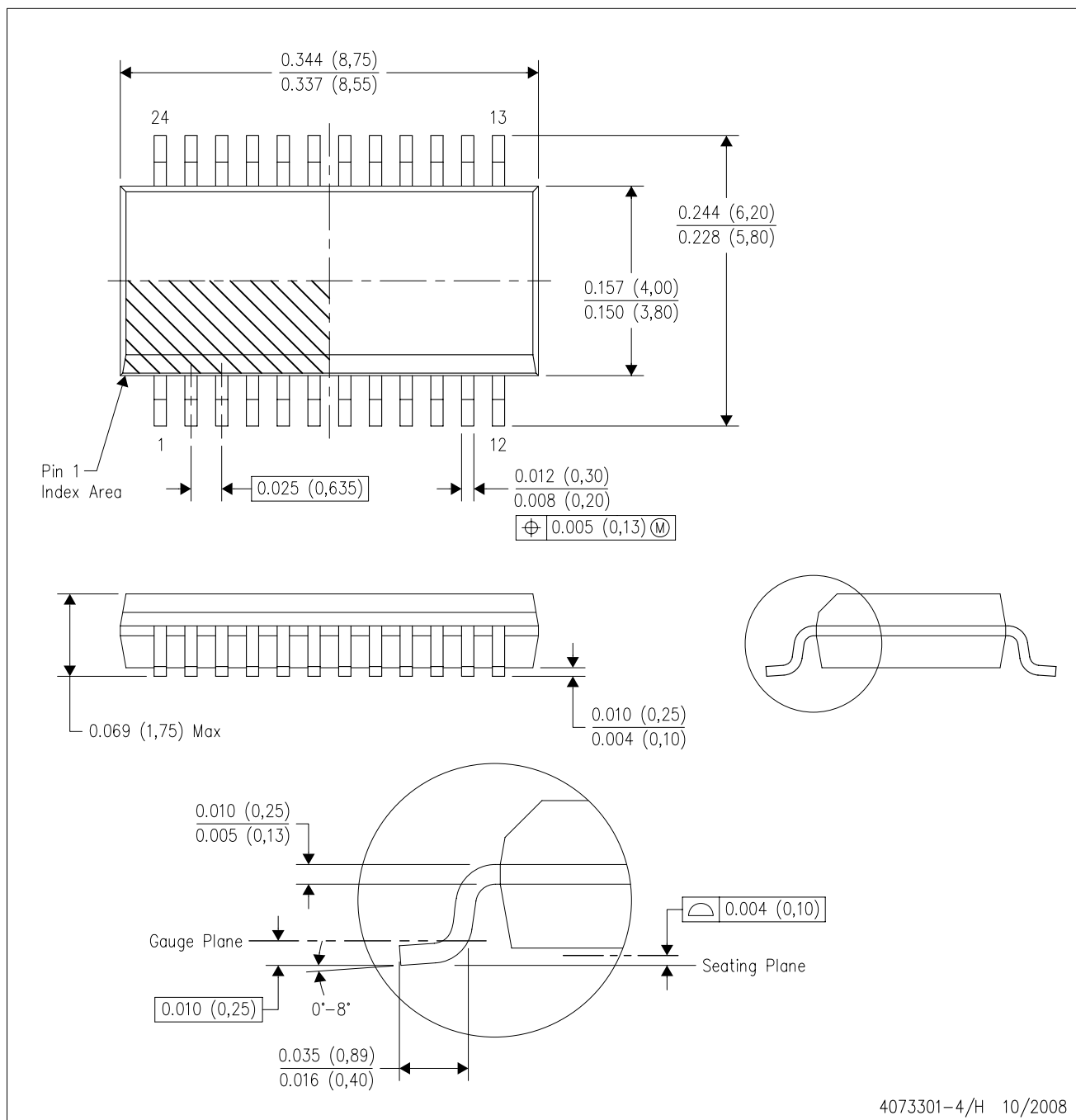


4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G24)

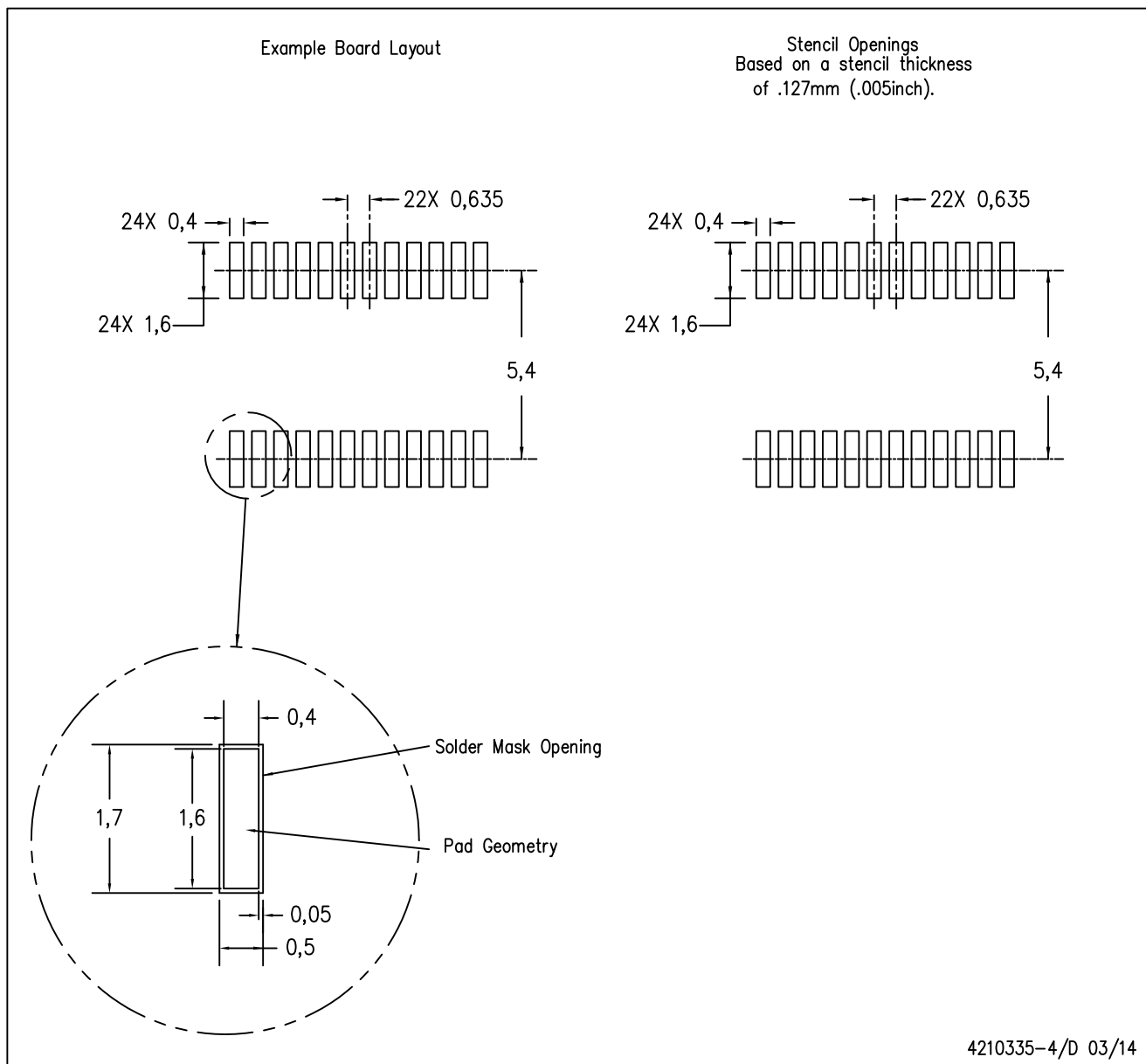
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

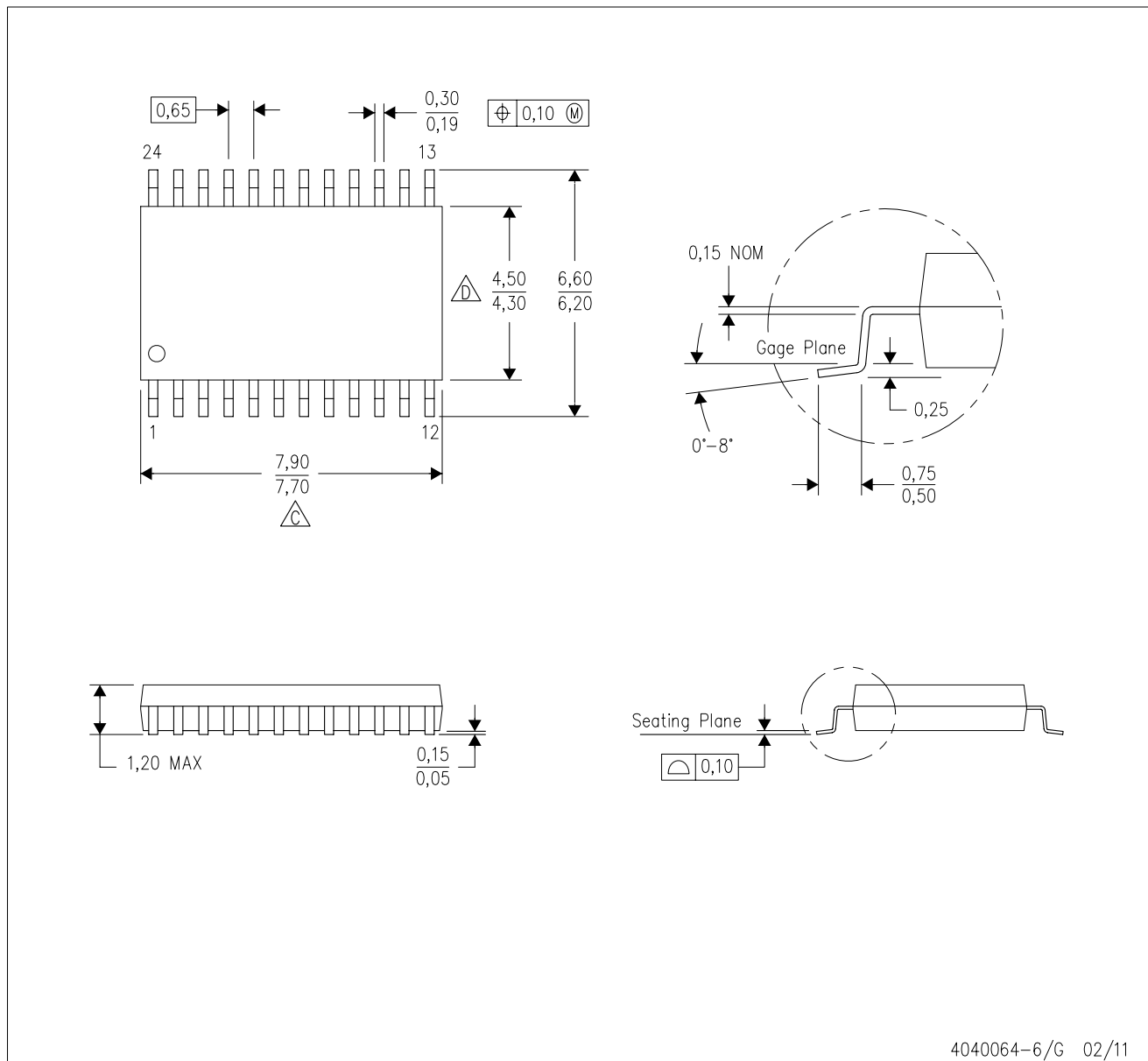
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

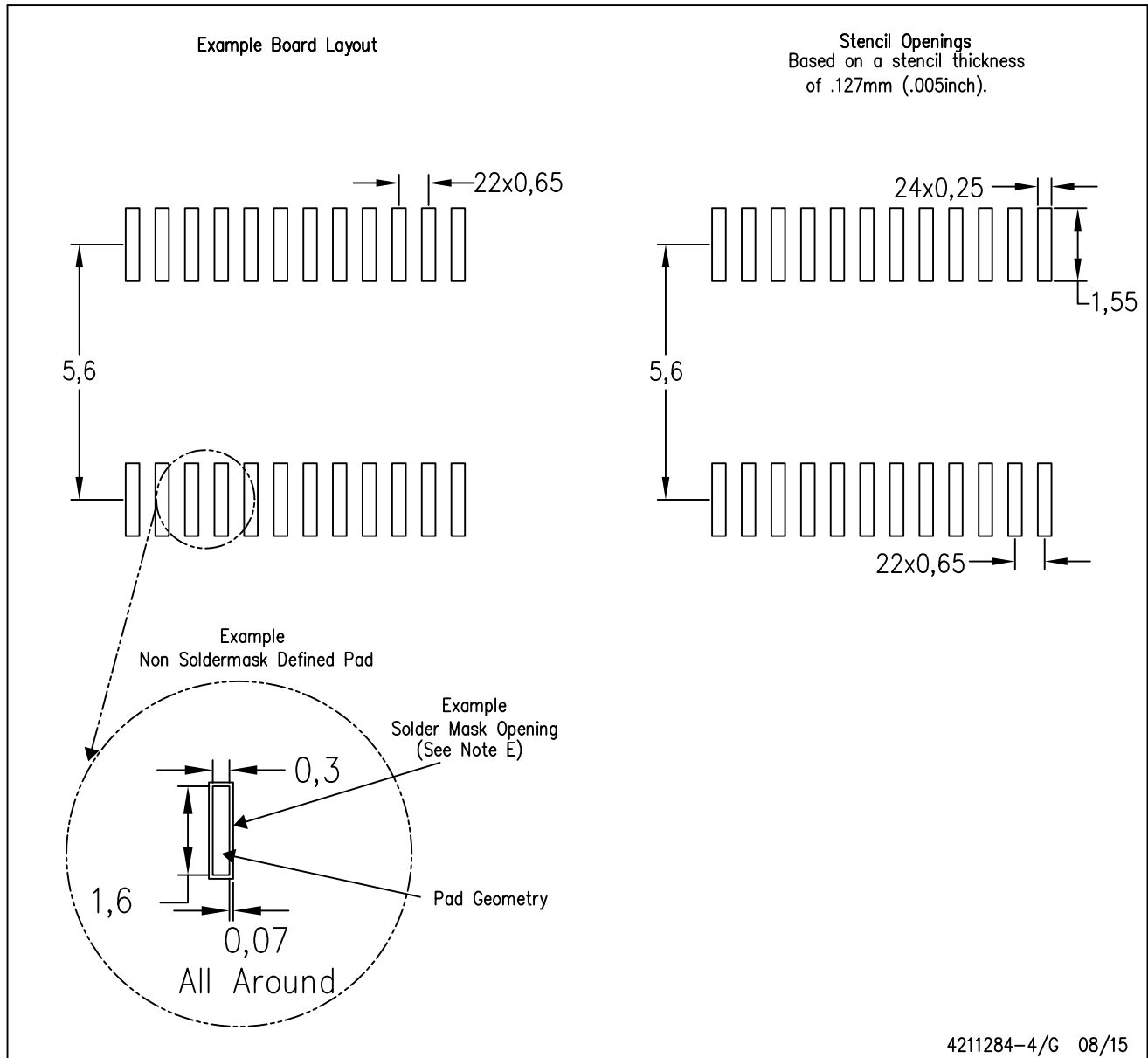


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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