National Semiconductor

August 2005

SCANSTA476
Eight Input IEEE 1149.1 Analog Voltage Monitor

General Description

The SCANSTA476 is a low power, Analog Voltage Monitor used for sampling or monitoring up to 8 analog/mixed-signal input channels. Analog Voltage Monitors are valuable during product development, environmental test, production, and field service for verifying and monitoring power supply and reference voltages. In a supervisory role, the 'STA476 is useful for card or system-level health monitoring and prognostics applications.

Instead of requiring an external microcontroller with a GPIO interface, the 'STA476 features a common IEEE 1149.1 (JTAG) interface to select the analog input, initiate a measurement, and access the results - further extending the capabilities of an existing JTAG infrastructure.

The SCANSTA476 uses the V_{REF} input as a reference. This enables the SCANSTA476 to operate with a full-scale input range of 0 to V_{DD}, which can range from +2.7V to +5.5V.

The SCANSTA476 is packaged in a 16-lead non-pullback LLP package that provides an extremely small footprint for applications where space is a critical consideration. This product operates over the industrial temperature range of −40˚C to +85˚C.

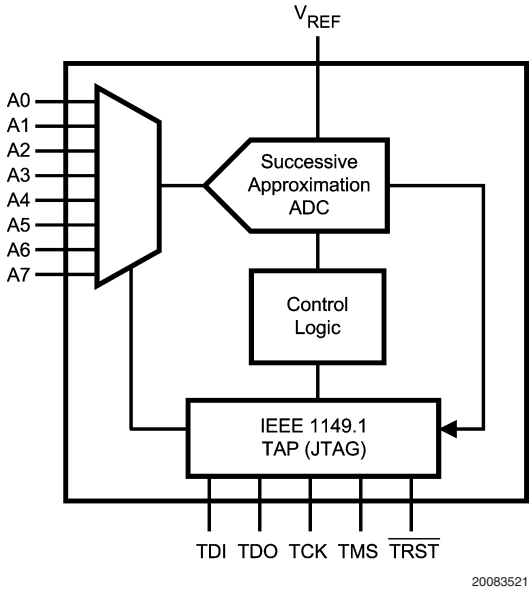
Features

- Eight selectable Analog input channels
- Analog full-scale input range 0V to V_{DD}
- Typical accuracy of 2 mV at maximum V_{DD}
- Very low power operation
- Small package footprint in 16-lead, 5 x 5 x 0.8 mm LLP
- Single +2.7V to +5.5V supply operation
- IEEE 1149.1 (JTAG) compliant interface

Applications

- Measurement of Point Voltages
- Real-time Signal Monitoring
- System Health Monitoring and Prognostics
- Debug, Environmental Test, Production Test, Field Service
- Supplement In-Circuit Tester (ICT) access
- Vital in Servers, Computing, Telecommunication and Industrial equipment
- Essential in Medical, Data Storage, and Networking equipment

Block Diagram



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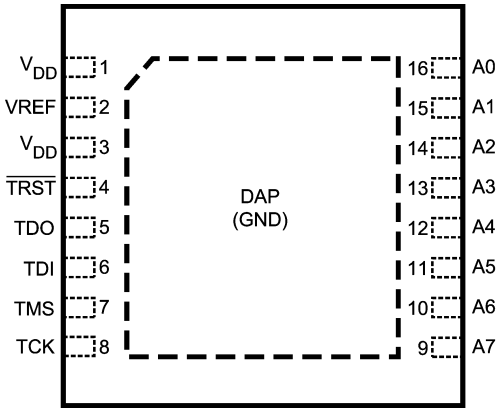
Connection Diagram



DAP = GND
(Top View)

Pin Descriptions

Pin No.	Symbol	Description
ANALOG I/O		
16	A0	Analog input 0. This signal can range from 0V to V_{REF}.
15	A1	Analog input 1. This signal can range from 0V to V_{REF}.
14	A2	Analog input 2. This signal can range from 0V to V_{REF}.
13	A3	Analog input 3. This signal can range from 0V to V_{REF}.
12	A4	Analog input 4. This signal can range from 0V to V_{REF}.
11	A5	Analog input 5. This signal can range from 0V to V_{REF}.
10	A6	Analog input 6. This signal can range from 0V to V_{REF}.
9	A7	Analog input 7. This signal can range from 0V to V_{REF}.
2	V_{REF}	Analog reference voltage input. V_{REF} must be ≤ V_{DD}. This pin should be connected to a quiet source (not directly to V_{DD}) and bypassed to GND with 0.1 µF and 1 µF monolithic capacitors located within 1 cm of the V_{REF} pin.
DIGITAL I/O		
6	TDI	Test Data Input to support IEEE 1149.1 features
5	TDO	Test Data Ouput to support IEEE 1149.1 features
7	TMS	Test Mode Select to support IEEE 1149.1 features
8	TCK	Test Clock to support IEEE 1149.1 features
4	$\overline{TRST}$	Test Reset to support IEEE 1149.1 features
POWER SUPPLY		
1,3	V_{DD}	Positive supply pin. These pins should be connected to a quiet +2.7V to +5.5V source and bypassed to GND with 0.1 µF and 1 µF monolithic capacitors located within 1 cm of the power pin.
(Note 1)	GND	Ground reference for CMOS circuitry. DAP is the exposed metal contact at the bottom of the LLP package. The DAP is used as the primary GND connection to the device. It should be connected to the ground plane with at least 4 vias for optimal low-noise and thermal performance.

Note 1: Note that GND is not an actual pin on the package, the GND is connected thru the DAP on the back side of the LLP package.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{DD}	−0.3V to +6.5V
Voltage on Any Analog Pin to GND	−0.3V to V_{DD}+0.3V
Voltage on Any Digital Pin to GND	-0.3V to V_{DD}+0.3V
Input Current at Any Pin (Note 4)	±10 mA
ESD Susceptibility	
Human Body Model	8000V
Machine Model	>250V
Soldering Temperature	Refer to AN-1187
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Thermal Resistance, θ_{JA}	42˚C/W
Thermal Resistance, θ_{JC}	14.3˚C/W

Recommended Operating Conditions

Operating Temperature Range	$-40˚C \le T_A \le +85˚C$
V_{DD} Supply Voltage	+2.7V to +5.5V
Digital Input Pins Voltage Range	+0V to V_{DD}
Analog Input Pins Voltage Range (Note 5)	+0V to V_{REF}

SCANSTA476 Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.5V, f_{TCK} = 20 MHz, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
POWER SUPPLY CHARACTERISTICS					
V_{DD}	Supply Voltage	$-40˚C \le T_A \le 85˚C$		2.7 5.5	V (min) V (max)
I_{DD}	Normal Mode (Static)	V_{DD} = +2.7V to +5.5V,	3.5	5.0	mA
	Normal Mode (Operational)	V_{DD} = +2.7V to +5.5V, f_{TCK} = 1 MSPS		5.0	mA (max)
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5.5V, f_{TCK} = 1 MSPS		27.5	mW (max)
ANALOG INPUT CHARACTERISTICS (A0-A7)					
V_{IN}	Analog Input Range	$V_{REF} \le V_{DD}$		0 to V_{REF}	V
V_{REF}	Reference Voltage Range			V_{DD}	V
I_{DCL}	DC Leakage Current		0.1	±10	µA (max)
V_{MEAS}	Analog Input Measurement Accuracy	V_{DD} = +2.7V	1	7.5	mV
		V_{DD} = +5.5V	2	15	
DIGITAL INPUT CHARACTERISTICS (TDI, TMS, TCK, $\overline{TRST}$)					
V_{IH}	Input High Voltage	V_{DD} = +2.7V to +3.6V		2.0	V (min)
		V_{DD} = +5.5V		2.1	
V_{IL}	Input Low Voltage	V_{DD} = +5V		0.8	V (max)
V_{CL}	Input Clamp Voltage	I_{CL} = -18mA	-0.8	-1.5	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_{DD}	0.2	±10	µA (max)
I_{ILR}	Input Current	$\overline{TRST}$, TDI, TMS only		-300	µA (max)
DIGITAL OUTPUT CHARACTERISTICS (TDO)					
V_{OH}	Output High Voltage	I_{OH} = -100 µA, 2.7V ≤ V_{DD} ≤ 5.5V		V_{DD} −0.2	V (min)
		I_{OH} = -4 mA, 3.0V ≤ V_{DD} ≤ 5.5V		2.4	V (min)
		I_{OH} = -4 mA, V_{DD} = 2.7V		2.2	V (min)
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, 2.7V ≤ V_{DD} ≤ 5.5V		0.2	V (max)
		I_{OL} = 4 mA, 2.7V ≤ V_{DD} ≤ 5.5V		0.4	V (max)
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, V_{DD} = 5.5V		-85	mA (max)
I_{OZ}	TRI-STATE Leakage Current			±10	µA (max)
	Output Coding		Straight (Natural) Binary		

SCANSTA476 Electrical Characteristics (Continued)

The following specifications apply for V_{DD} = +2.7V to 5.5V, f_{TCK} = 20 MHz, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
AC ELECTRICAL CHARACTERISTICS					
F_{MAX}	Throughput Rate	TCK = 20MHz		1	MSPS (max)
INPUT TIMING CHARACTERISTICS					
t_{SET}	TDI to TCK (H/L)	(Note 3)		2.0	ns (min)
t_{HOLD}	TDI to TCK (H/L)	(Note 3)		1.5	ns (min)
t_{SET}	TMS to TCK (H/L)	(Note 3)		2.0	ns (min)
t_{HOLD}	TMS to TCK (H/L)	(Note 3)		2.0	ns (min)
t_W	TCK Pulse Width (H/L)	(Note 3)		10.0	ns (min)
t_{REC}	Recovery TIme $\overline{TRST}$ to TCK	(Note 3)		2.0	ns (min)
t_W	TRST Pulse Width (L)	(Note 3)		2.5	ns (min)
F_{MAX}	TCK			20	MHz (min)

Note 2: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not implied. Exposure to maximum ratings for extended periods may affect device reliability.

Note 3: Data sheet min/max specification limits are guaranteed by design or statistical analysis.

Note 4: Except power supply pins.

Note 5: For valid measurements, the analog $V_{IN} < V_{REF} \leq V_{DD}$.

Applications Information

POWER-UP TIMING

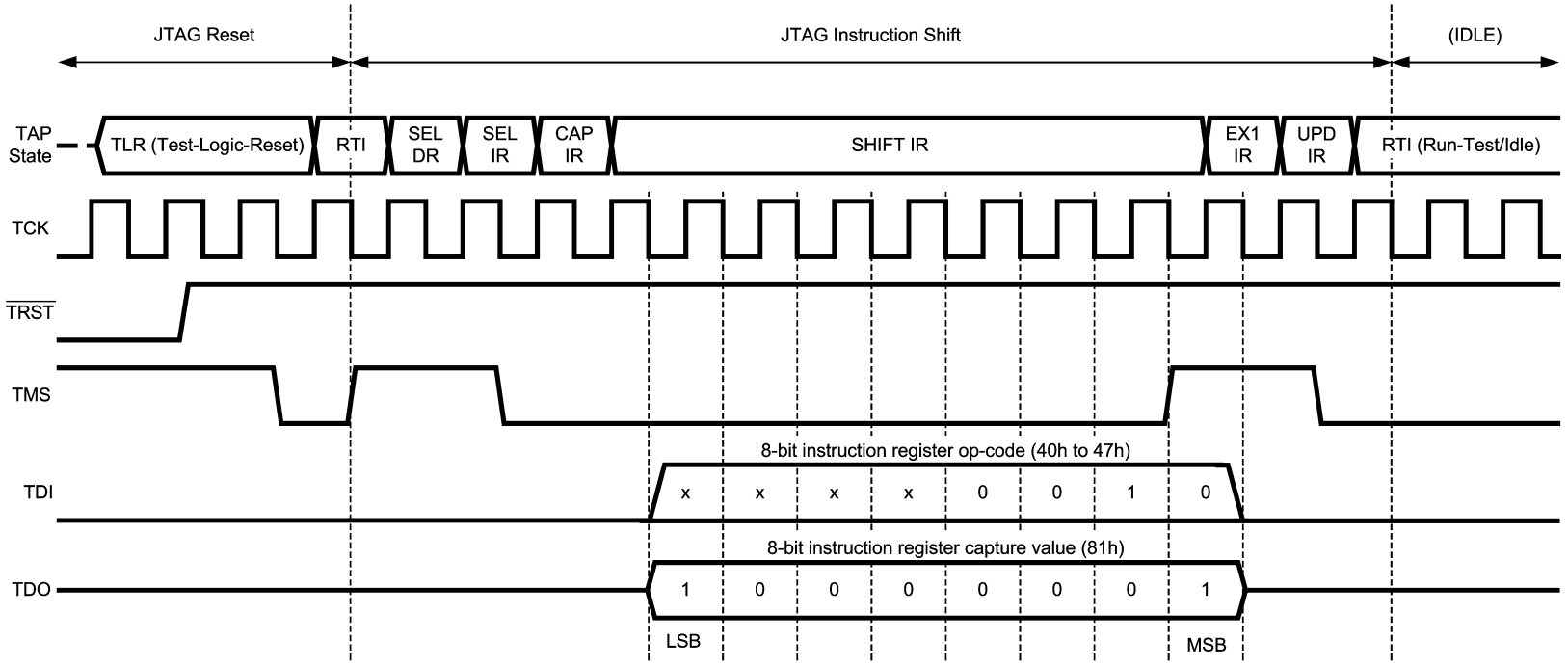
The SCANSTA476 typically requires 1 µs to power up , either after first applying V_{DD}, or after an incomplete conversion shift. To return to normal, one "dummy" conversion must be fully completed. After this first dummy conversion, the SCANSTA476 will perform conversions properly.

STARTUP MODE

When the V_{DD} supply is first applied, the SCANSTA476 requires one dummy conversion after start-up.

Timing Diagrams

Instruction Shift (Channel Select)



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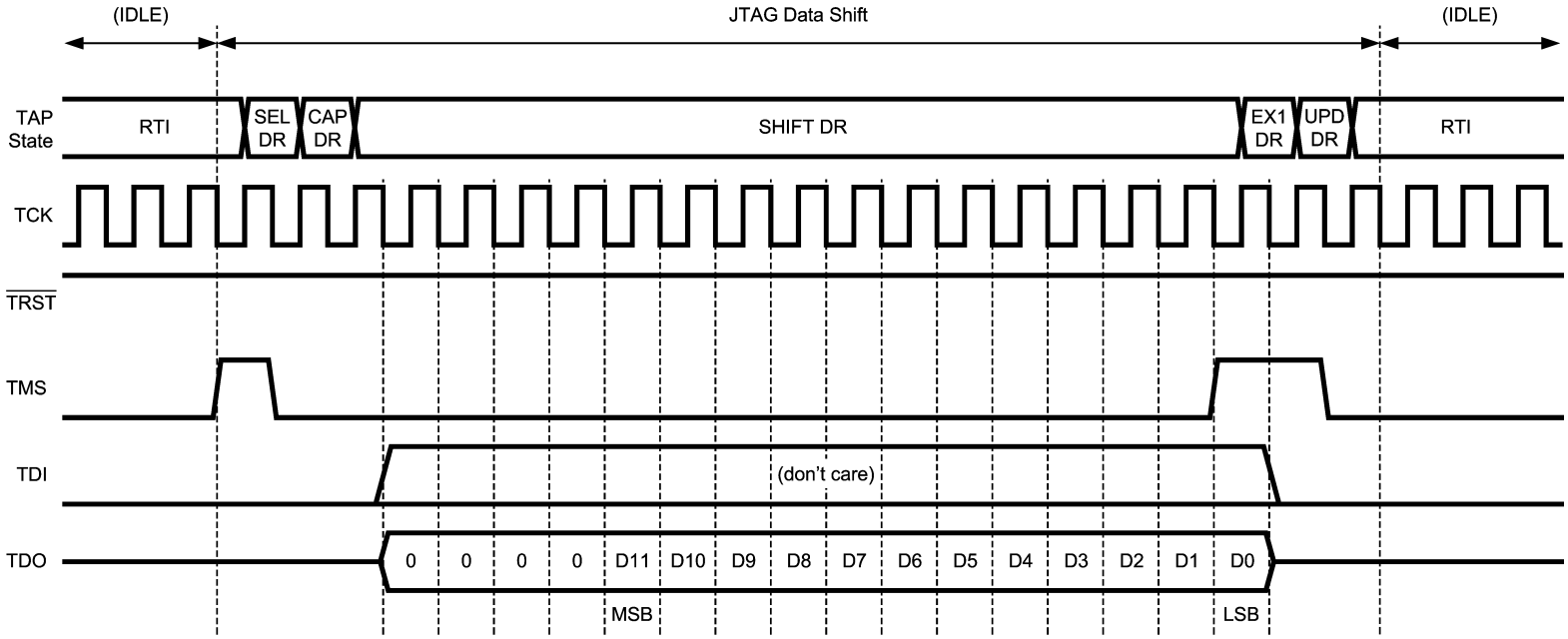
Op-codes 40h to 47h select pins A0 to A7 respectively.

Note the JTAG reset preamble places the JTAG TAP controller in a stable state (RTI). Both the instruction and data shifts start in - and return to - the RTI state.

Timing Diagrams (Continued)

Data Shift (A/D Sample)



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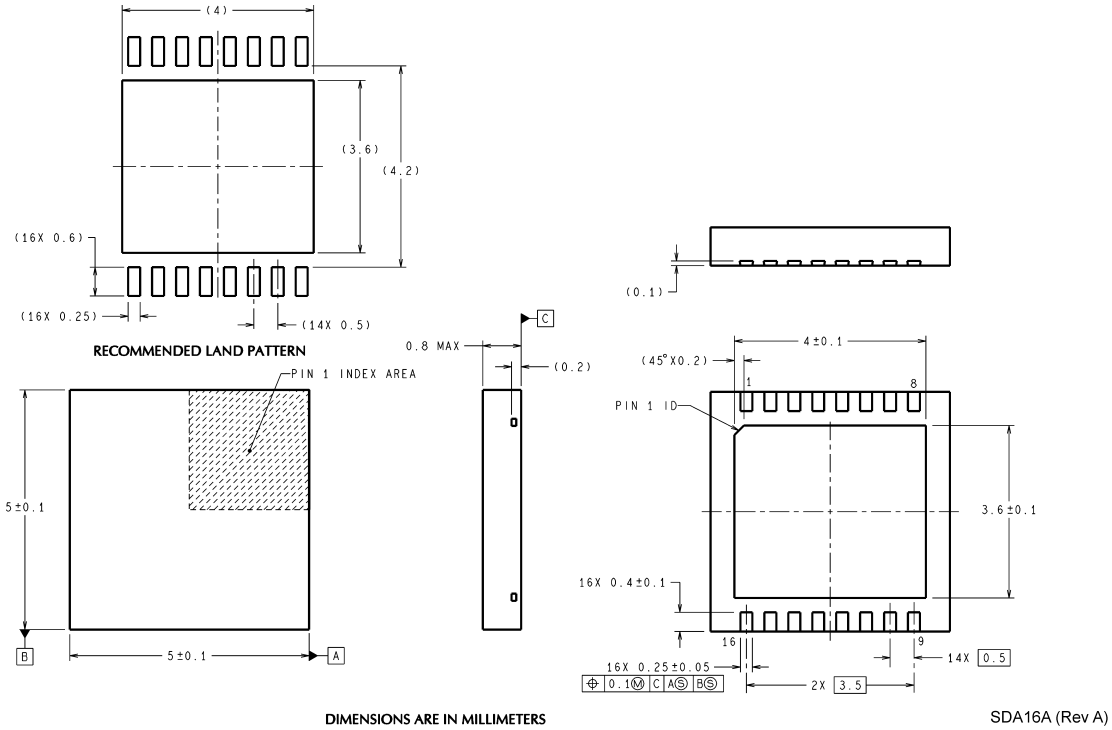
D11 through D0 correspond to the 12-bit sample from the ADC Core.

Note that Data shifts can be run back-to-back for continous sampling of a single channel, or can be interleaved with instruction shifts for rippling through all 8 channels.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

SDA16A (Rev A)

LLP, Plastic, Dual
Order Number SCANSTA476TSD,
NS Package Number SDA16A

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560