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# **SCB15H1G800AF**

# **SCB15H1G160AF**

**1Gbit DDR3 SDRAM**  
**EU RoHS Compliant Products**

## **Data Sheet**

**Rev. E**

Revision History:		
Date	Revision	Subjects (major changes since last revision)
2014-07	A	Initialized version
2015-01	B	Updated BGA ball out figure
2016-03	C	Change to UniIC Format
2016-09	D	Add the "1" grade product
2017-12	E	Add the "A1", "A2" & "A3" grade product

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# 1 Overview

This chapter gives an overview of the 1Gbit Double-Data-Rate-Three (DDR3) SDRAM component product and describes its main characteristics.

## 1.1 Features






The 1Gbit DDR3 SDRAM offers the following key features:

- 1.5 V  $\pm$  0.075 V supply voltage for  $V_{DD}$  and  $V_{DDQ}$
- Data rate: 1066Mbps/1333Mbps/1600Mbps
- SDRAM configurations with  $\times 8$  data in/outputs
  - Page Size: 1 KByte page size
  - Row address: A0 to A13
  - Column address: A0 to A9
- SDRAM configurations with  $\times 16$  data in/outputs
  - Page Size: 2 KByte page size
  - Row address: A0 to A12
  - Column address: A0 to A9
- Asynchronous RESET#
- Auto-Precharge operation for read and write commands
- Refresh, Self-Refresh and power saving Power-down modes; Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Operating temperature range:
  - Commercial, (0 °C to 95 °C)
  - Industrial, I (-40 °C to 95 °C)
  - Automotive, A1 (-40 °C to 125 °C)
  - Automotive, A2 (-40 °C to 105 °C)
  - Automotive, A3 (-40 °C to 95 °C)
- Data mask function for write operation
- Average Refresh Period 7.8  $\mu$ s at a TCASE lower than 105°C, 3.9  $\mu$ s above 105°C
- Commands can be entered on each positive clock edge
- Data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- CAS latency (CL): 5, 6, 7, 8, 9, 10, 11
- Posted CAS with programmable additive latency (AL = 0, CL-1 and CL-2) for improved command, address and data bus efficiency
- Read Latency RL = AL + CL
- Programmable CAS Write Latency (CWL) per operating frequency: 5, 6, 7, 8
- Write Latency WL = AL + CWL
- Burst length 8 (BL8) and burst chop 4(BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or sequential
- Multi-purpose register (MPR) for readout of non-memory related information
- System level timing calibration support via write leveling and MPR read pattern
- Differential clock inputs (CK and CK#)
- Bi-directional, differential data strobe pair (DQS and DQS#) is transmitted / received with data. Edge aligned with read data and center-aligned with write data
- DLL aligns transmitted read data and strobe pair transition with clock
- Programmable on-die termination (ODT) for data, data mask and differential strobe pairs
- Dynamic ODT mode for improved signal integrity and pre-selectable termination impedances during writes
- ZQ Calibration for output driver and on-die termination using external reference resistor to ground
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240  $\Omega$ )
- Lead and halogen free packages:
  - PG-TFBGA-78 for x8 component
  - PG-TFBGA-96 for x16 component

## 1.2 Product List

**Table 1** shows all possible products within the 1Gbit DDR3 SDRAM component generation. Availability depends on application needs. For UnilC part number nomenclatures see **Chapter 6**.

**Table 1 - Ordering Information for 1Gbit DDR3 Components**

Product Type <sup>1)</sup>	Org.	Speed	CAS-RCD-RP Latencies <sup>2)3)4)</sup>	Clock (MHz)	Package	Note <sup>5)</sup>
<b>Commercial Temperature Range (0 °C~ +95 °C)</b>						
SCB15H1G800AF-13K	×8	DDR3-1600K	11-11-11	800	PG-TFBGA-78	
SCB15H1G160AF-13K	×16	DDR3-1600K	11-11-11	800	PG-TFBGA-96	
SCB15H1G800AF-15H	×8	DDR3-1333H	9-9-9	667	PG-TFBGA-78	
SCB15H1G160AF-15H	×16	DDR3-1333H	9-9-9	667	PG-TFBGA-96	
SCB15H1G800AF-19F	×8	DDR3-1066F	7-7-7	533	PG-TFBGA-78	
SCB15H1G160AF-19F	×16	DDR3-1066F	7-7-7	533	PG-TFBGA-96	
<b>Industrial Temperature Range (-40 °C~ +95 °C)</b>						
SCB15H1G800AF-13KI	×8	DDR3-1600K	11-11-11	800	PG-TFBGA-78	
SCB15H1G160AF-13KI	×16	DDR3-1600K	11-11-11	800	PG-TFBGA-96	
SCB15H1G800AF-15HI	×8	DDR3-1333H	9-9-9	667	PG-TFBGA-78	
SCB15H1G160AF-15HI	×16	DDR3-1333H	9-9-9	667	PG-TFBGA-96	
SCB15H1G800AF-19FI	×8	DDR3-1066F	7-7-7	533	PG-TFBGA-78	
SCB15H1G160AF-19FI	×16	DDR3-1066F	7-7-7	533	PG-TFBGA-96	
<b>Automotive A2 Temperature Range (-40 °C~ +125 °C)</b>						
SCB15H1G800AF-13KA1	×8	DDR3-1600K	11-11-11	800	PG-TFBGA-78	
SCB15H1G160AF-13KA1	×16	DDR3-1600K	11-11-11	800	PG-TFBGA-96	
SCB15H1G800AF-15HA1	×8	DDR3-1333H	9-9-9	667	PG-TFBGA-78	
SCB15H1G160AF-15HA1	×16	DDR3-1333H	9-9-9	667	PG-TFBGA-96	
SCB15H1G800AF-19FA1	×8	DDR3-1066F	7-7-7	533	PG-TFBGA-78	
SCB15H1G160AF-19FA1	×16	DDR3-1066F	7-7-7	533	PG-TFBGA-96	
<b>Automotive A2 Temperature Range (-40 °C~ +105 °C)</b>						
SCB15H1G800AF-13KA2	×8	DDR3-1600K	11-11-11	800	PG-TFBGA-78	
SCB15H1G160AF-13KA2	×16	DDR3-1600K	11-11-11	800	PG-TFBGA-96	
SCB15H1G800AF-15HA2	×8	DDR3-1333H	9-9-9	667	PG-TFBGA-78	
SCB15H1G160AF-15HA2	×16	DDR3-1333H	9-9-9	667	PG-TFBGA-96	
SCB15H1G800AF-19FA2	×8	DDR3-1066F	7-7-7	533	PG-TFBGA-78	
SCB15H1G160AF-19FA2	×16	DDR3-1066F	7-7-7	533	PG-TFBGA-96	
<b>Automotive A3 Temperature Range (-40 °C~ +95 °C)</b>						
SCB15H1G800AF-13KA3	×8	DDR3-1600K	11-11-11	800	PG-TFBGA-78	
SCB15H1G160AF-13KA3	×16	DDR3-1600K	11-11-11	800	PG-TFBGA-96	
SCB15H1G800AF-15HA3	×8	DDR3-1333H	9-9-9	667	PG-TFBGA-78	
SCB15H1G160AF-15HA3	×16	DDR3-1333H	9-9-9	667	PG-TFBGA-96	
SCB15H1G800AF-19FA3	×8	DDR3-1066F	7-7-7	533	PG-TFBGA-78	
SCB15H1G160AF-19FA3	×16	DDR3-1066F	7-7-7	533	PG-TFBGA-96	

- 1) For detailed information regarding product type of UnilC please see chapter "Product Nomenclature" of this data sheet.
- 2) CAS: Column Address Strobe.
- 3) RCD: Row Column Delay.
- 4) RP: Row Precharge.
- 5) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit <http://www.unisemicon.com/>

## 1.3 DDR3 SDRAM Addressing

**Table 2 - 1Gbit DDR3 SDRAM Addressing**

Configuration	128Mb × 8	64Mb × 16	Note
Number of Banks	8	8	
Bank Address	BA[2:0]	BA[2:0]	
Row Address	A[13:0]	A[12:0]	
Column Address	A[9:0]	A[9:0]	
Page Size	1KB	2KB	<sup>1)</sup>
Auto-Precharge	A10   AP	A10   AP	
Burst length on-the-fly bit	A12   BC#	A12   BC#	

- 1) Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per memory bank and calculated as follows: Page Size =  $2^{\text{COLBITS}} \times \text{ORG}/8$ , where COLBITS is the number of column address bits and ORG is the number of DQ bits for a given SDRAM configuration (×8 or ×16).

## 1.4 Package Ballout

### 1.4.1 Ballout for 128 Mb x 8 Components

Figure 1 - Ballout for 128 Mb x8 Components (PG-TFBGA-78 Top View)

1	2	3	4	5	6	7	8	9
V <sub>SS</sub>	V <sub>DD</sub>	NC		<b>A</b>		NU /TDQS	V <sub>SS</sub>	V <sub>DD</sub>
V <sub>SS</sub>	V <sub>SSQ</sub>	DQ0		<b>B</b>		DM TDQS	V <sub>SSQ</sub>	V <sub>DDQ</sub>
V <sub>DDQ</sub>	DQ2	DQS		<b>C</b>		DQ1	DQ3	V <sub>SSQ</sub>
V <sub>SSQ</sub>	DQ6	/DQS		<b>D</b>		V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SSQ</sub>
V <sub>REFDQ</sub>	V <sub>DDQ</sub>	DQ4		<b>E</b>		DQ7	DQ5	V <sub>DDQ</sub>
NC	V <sub>SS</sub>	/RAS		<b>F</b>		CK	V <sub>SS</sub>	NC
ODT	V <sub>DD</sub>	/CAS		<b>G</b>		/CK	V <sub>DD</sub>	CKE
NC	/CS	/WE		<b>H</b>		A10 AP	ZQ	NC
V <sub>SS</sub>	BA0	BA2		<b>J</b>		NC	V <sub>REFCA</sub>	V <sub>SS</sub>
V <sub>DD</sub>	A3	A0		<b>K</b>		A12 /BC	BA1	V <sub>DD</sub>
V <sub>SS</sub>	A5	A2		<b>L</b>		A1	A4	V <sub>SS</sub>
V <sub>DD</sub>	A7	A9		<b>M</b>		A11	A6	V <sub>DD</sub>
V <sub>SS</sub>	/RESET	A13		<b>N</b>		NC	A8	V <sub>SS</sub>

## 1.4.2 Input / Output Signal Functional Description

**Table 3 - Input / Output Signal Functional Description for x8 component**

Symbol	Type	Function
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	<b>Clock Enable:</b> CKE High activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (active row in any bank). CKE is asynchronous for Self-Refresh exit. After $V_{REFCA}$ and $V_{REFDQ}$ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained High throughout read and write accesses. Input buffers, excluding CK, CK#, ODT, CKE and RESET# are disabled during Power-down. Input buffers, excluding CKE and RESET are disabled during self refresh.
CS#	Input	<b>Chip Select:</b> All commands are masked when CS# is registered High. CS# provides for external Rank selection on systems with multiple ranks. CS# is considered part of the command code.
RAS#, CAS#, WE#	Input	<b>Command Inputs:</b> RAS#, CAS# and WE# (along with CS#) define the command being entered.
ODT	Input	<b>On-Die Termination:</b> ODT (registered High) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# signal for x8 configurations. The ODT signal will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and during Self Refresh.
DM	Input	<b>Input Data Mask :</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
TDQS/TDQS#	input	<b>Termination Data Strobe:</b> TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used.
BA0 - BA2	Input	<b>Bank Address Inputs:</b> Define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a mode register set cycle.
A0 - A13	Input	<b>Address Inputs:</b> Provides the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10   AP and A12   BC# have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands. For numbers of addresses used on this assembly see <a href="#">Table 2</a> .

Symbol	Type	Function
A10   AP	Input	<b>Auto-Precharge:</b> A10   AP is sampled during Read/Write commands to determine whether Auto-Precharge should be performed to the accessed bank after the Read/Write operation. (High: Auto-Precharge, Low: no Auto-Precharge). A10   AP is sampled during Precharge command to determine whether the Precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by bank addresses.
A12   BC#	Input	<b>Burst Chop:</b> A12   BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (High: no burst chop, Low: burst chopped). See <b>“Command Truth Table” on Page 10</b> for details.
DQ0~7	Input/ Output	<b>Data Input/Output:</b> Bi-directional data bus.
DQS,DQS#	Input/ Output	<b>Data Strobe:</b> Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signal DQS#, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
RESET#	Input	<b>Active Low Asynchronous Reset:</b> Reset is active when RESET# is Low, and inactive when RESET# is High. RESET# must be High during normal operation. RESET# is a CMOS rail to rail signal with DC High and Low are 80% and 20% of $V_{DD}$ , RESET# active is destructive to data contents.
NC	—	<b>No Connect:</b> no internal electrical connection is present
$V_{DDQ}$	Supply	<b>DQ Power Supply:</b> 1.5 V $\pm$ 0.075 V
$V_{SSQ}$	Supply	<b>DQ Ground</b>
$V_{DD}$	Supply	<b>Power Supply:</b> 1.5 V $\pm$ 0.075 V
$V_{SS}$	Supply	<b>Ground</b>
$V_{REFDQ}$	Supply	<b>Reference Voltage for DQ</b>
$V_{REFCA}$	Supply	<b>Reference Voltage for Command and Address inputs</b>
ZQ	Supply	Reference ball for ZQ calibration

Note: Input only pins (BA0-BA2, A0-A13, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.

### 1.4.3 Ballout for 64 Mb × 16 Components

Figure 2 - Ballout for 64 Mb ×16 Components (PG-TFBGA-96 Top View)

1	2	3	4	5	6	7	8	9
V <sub>DDQ</sub>	DQU5	DQU7		A		DQU4	V <sub>DDQ</sub>	V <sub>SS</sub>
V <sub>SSQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>		B		/DQSU	DQU6	V <sub>SSQ</sub>
V <sub>DDQ</sub>	DQU3	DQU1		C		DQSU	DQU2	V <sub>DDQ</sub>
V <sub>SSQ</sub>	V <sub>DDQ</sub>	DMU		D		DQU0	V <sub>SSQ</sub>	V <sub>DD</sub>
V <sub>SS</sub>	V <sub>SSQ</sub>	DQL0		E		DML	V <sub>SSQ</sub>	V <sub>DDQ</sub>
V <sub>DDQ</sub>	DQL2	DQSL		F		DQL1	DQL3	V <sub>SSQ</sub>
V <sub>SSQ</sub>	DQL6	/DQSL		G		V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SSQ</sub>
V <sub>REFDQ</sub>	V <sub>DDQ</sub>	DQL4		H		DQL7	DQL5	V <sub>DDQ</sub>
NC	V <sub>SS</sub>	/RAS		J		CK	V <sub>SS</sub>	NC
ODT	V <sub>DD</sub>	/CAS		K		/CK	V <sub>DD</sub>	CKE
NC	/CS	/WE		L		A10 AP	ZQ	NC
V <sub>SS</sub>	BA0	BA2		M		NC	V <sub>REFCA</sub>	V <sub>SS</sub>
V <sub>DD</sub>	A3	A0		N		A12 /BC	BA1	V <sub>DD</sub>
V <sub>SS</sub>	A5	A2		P		A1	A4	V <sub>SS</sub>
V <sub>DD</sub>	A7	A9		R		A11	A6	V <sub>DD</sub>
V <sub>SS</sub>	/RESET	NC		T		NC	A8	V <sub>SS</sub>

## 1.4.4 Input / Output Signal Functional Description

Table 4 - Input / Output Signal Functional Description for x16 component

Symbol	Type	Function
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE	Input	<b>Clock Enable:</b> CKE High activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (active row in any bank). CKE is asynchronous for Self-Refresh exit. After $V_{REFCA}$ and $V_{REFDQ}$ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained High throughout read and write accesses. Input buffers, excluding CK, CK#, ODT, CKE and RESET# are disabled during Power-down. Input buffers, excluding CKE and RESET are disabled during self refresh.
CS#	Input	<b>Chip Select:</b> All commands are masked when CS# is registered High. CS# provides for external Rank selection on systems with multiple ranks. CS# is considered part of the command code.
RAS#, CAS#, WE#	Input	<b>Command Inputs:</b> RAS#, CAS# and WE# (along with CS#) define the command being entered.
ODT	Input	<b>On-Die Termination:</b> ODT (registered High) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal for x16 configurations. The ODT signal will be ignored if the Mode Register MR1 and MR2 are programmed to disable ODT and during Self Refresh.
DM (DMU), (DML)	Input	<b>Input Data Mask :</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	<b>Bank Address Inputs:</b> Define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a mode register set cycle.
A0 - A12	Input	<b>Address Inputs:</b> Provides the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10   AP and A12   BC# have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands. For numbers of addresses used on this assembly see <a href="#">Table 2</a> .

Symbol	Type	Function
A10   AP	Input	<b>Auto-Precharge:</b> A10   AP is sampled during Read/Write commands to determine whether Auto-Precharge should be performed to the accessed bank after the Read/Write operation. (High: Auto-Precharge, Low: no Auto-Precharge). A10   AP is sampled during Precharge command to determine whether the Precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by bank addresses.
A12   BC#	Input	<b>Burst Chop:</b> A12   BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (High: no burst chop, Low: burst chopped). See “ <b>Command Truth Table</b> ” on Page 10 for details.
DQ(DQL0~7), (DQU0~7)	Input/ Output	<b>Data Input/Output:</b> Bi-directional data bus.
DQSL,DQSL# DQSU, DQSU#	Input/ Output	<b>Data Strobe:</b> Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQSL and DQSU are paired with differential signals DQSL# and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
RESET#	Input	<b>Active Low Asynchronous Reset:</b> Reset is active when RESET# is Low, and inactive when RESET# is High. RESET# must be High during normal operation. RESET# is a CMOS rail to rail signal with DC High and Low are 80% and 20% of $V_{DD}$ , RESET# active is destructive to data contents.
NC	—	<b>No Connect:</b> no internal electrical connection is present
$V_{DDQ}$	Supply	<b>DQ Power Supply:</b> 1.5 V $\pm$ 0.075 V
$V_{SSQ}$	Supply	<b>DQ Ground</b>
$V_{DD}$	Supply	<b>Power Supply:</b> 1.5 V $\pm$ 0.075 V
$V_{SS}$	Supply	<b>Ground</b>
$V_{REFDQ}$	Supply	<b>Reference Voltage for DQ</b>
$V_{REFCA}$	Supply	<b>Reference Voltage for Command and Address inputs</b>
ZQ	Supply	Reference ball for ZQ calibration

Note: Input only pins (BA0-BA2, A0-A12, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.

## 2 Functional Description

### 2.1 Truth Tables

The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the DDR3 SDRAM. **Table 5** lists all valid commands to the DDR3 SDRAM. For a detailed description

of the various power mode entries and exits please refer to **Table 6**. In addition, the DM functionality is described in **Table 7**.

**Table 5 - Command Truth Table**

Function	Abbreviation	CKE		CS	RAS	CAS	WE	BA0 - BA2	A13 - A14	A12 / BC	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7)9)12)
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X
				L	H	H	H	H	V	V	V	V	V
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10)
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11)
ZQ calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6)12)
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6)12)
				H	X	X	X	X	X	X	X	X	

Notes 1) - 4) apply to the entire Command Truth Table.

Note 5) apply to all Read/Write command.

- 1) All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant.
- 2) RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- 3) Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
- 4) "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
- 5) Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS.
- 6) The Power Down Mode does not perform any refresh operations.
- 7) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 8) Self refresh exit is asynchronous.
- 9) VREF(Both VREFDQ and VREFCA) must be maintained during Self Refresh operation. VrefDQ supply may be turned OFF and VREFDQ may take any value between VSS and VDD during Self Refresh operation, provided that VrefDQ is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
- 10) The No Operation command (NOP) should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
- 11) The Deselect command performs the same function as a No Operation command.
- 12) Refer to the CKE Truth Table for more detail with CKE transition.

**Table 6 - Clock Enable (CKE) Truth Table for Synchronous Transitions**

Current State <sup>1)</sup>	CKE(N-1) <sup>2)</sup>	CKE(N) <sup>2)</sup>	Command (N) <sup>3)</sup>	Action (N) <sup>3)</sup>	Note <sup>4)-7)</sup>
	Previous Cycle	Current Cycle	RAS#, CAS#, WE#, CS#		
Power Down	L	L	X	Maintain Power Down	8)9)
	L	H	DES or NOP	Power Down Exit	8)10)
Self Refresh	L	L	X	Maintain Self Refresh	9)11)
	L	H	DES or NOP	Self Refresh Exit	11)12)13)
Bank(s) Active	H	L	DES or NOP	Active Power Down Entry	8)10)14)
Reading	H	L	DES or NOP	Power Down Entry	8)10)14)15)
Writing	H	L	DES or NOP	Power Down Entry	8)10)14)15)
Precharging	H	L	DES or NOP	Power Down Entry	8)10)14)15)
Refreshing	H	L	DES or NOP	Precharge Power Down Entry	10)
All Banks Idle	H	L	DES or NOP	Precharge Power Down Entry	8)10)14)16)
	H	L	REF	Self Refresh Entry	14)16)17)
Any other state	Refer to “ <b>Command Truth Table</b> ” on Page 10 for more detail with all command signals				18)

- 1) Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
- 2) CKE(N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- 3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
- 4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- 5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 6) CKE must be registered with the same value on  $t_{CKE(MIN)}$  consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the  $t_{CKE(MIN)}$  clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + t_{CKE(MIN)} + t_{IH}$ .
- 7) DES and NOP are defined in “**Command Truth Table**” on Page 10.
- 8) The Power Down does not perform any refresh operations
- 9) X means Don't care (including floating around  $V_{REFCA}$ ) in Self Refresh and Power Down. It also applies to address pins.
- 10) Valid commands for Power Down Entry and Exit are NOP and DES only
- 11)  $V_{REF}$  (both  $V_{REFCA}$  and  $V_{REFDQ}$ ) must be maintained during Self Refresh operation.  $V_{refDQ}$  supply may be turned OFF and  $V_{REFDQ}$  may take any value between VSS and VDD during Self Refresh operation, provided that  $V_{refDQ}$  is valid and stable prior to CKE going back High and that first Write operation or first Write Leveling Activity may not occur earlier than 512 nCK after exit from Self Refresh.
- 12) On Self Refresh Exit DES or NOP commands must be issued on every clock edge occurring during the  $t_{XS}$  period. Read, or ODT commands may be issued only after  $t_{XSDLL}$  is satisfied.
- 13) Valid commands for Self Refresh Exit are NOP and DES only.
- 14) Self Refresh can not be entered while Read or Write operations are in progress.
- 15) If all banks are closed at the conclusion of a read, write or precharge command then Precharge Power-down is entered, otherwise Active Power-down is entered.
- 16) 'Idle state' is defined as all banks are closed ( $t_{RP}$ ,  $t_{DAL}$ , etc. satisfied), no data bursts are in progress, CKE is High, and all timings from previous operations are satisfied ( $t_{MRD}$ ,  $t_{MOD}$ ,  $t_{RFC}$ ,  $t_{ZQ.INIT}$ ,  $t_{ZQ.OPER}$ ,  $t_{ZQCS}$ , etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied ( $t_{XS}$ ,  $t_{XP}$ ,  $t_{XPDLL}$ , etc.).
- 17) Self Refresh mode can only be entered from the All Banks Idle state.
- 18) Must be a legal command as defined in “**Command Truth Table**” on Page 10.

**Table 7 - Data Mask (DM) Truth Table**

Name (Function)	DM	DQs
Write Enable	L	Valid
Write Inhibit	H	X

## 2.2 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below  $0.2 \times VDD$ ; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp,  $VDD > VDDQ$  and  $(VDD - VDDQ) < 0.3$  volts.
  - VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
  - Vref tracks  $VDDQ/2$ .

OR

- Apply VDD without any slope reversal before or at the same time as VDDQ.
  - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
  - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET# is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
  3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
  4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT\_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
  5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. ( $tXPR = \max(tXS; 5 \times tCK)$ )
  6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
  7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
  8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
  9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
  10. Issue ZQCL command to starting ZQ calibration.
  11. Wait for both tDLLK and tZQinit completed.
  12. The DDR3 SDRAM is now ready for normal operation.

## 2.3 Mode Register 0 (MR0)

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR (write recovery time for auto-precharge) and DLL control for precharge Power-Down, which includes various vendor

specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting Low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to [Table 8](#).

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0 <sup>1)</sup>	PPD	WR			DLL	TM	CL			RBT	CL	BL	

**Table 8 - MR0 Mode register Definition (BA[2:0]=000B)**

Field	Bits <sup>1)</sup>	Description
BL	A[1:0]	<p><b>Burst Length (BL) and Control Method</b> Number of sequential bits per DQ related to one Read/Write command. <b>BL8MRS</b> mode with fixed burst length of 8. A12   BC# at Read or Write command time is Don't care at read or write command time. <b>BLOTF</b> on-the-fly (OTF) enabled using A12   BC# at Read or Write command time. When A12   BC# is High during Read or Write command time a burst length of 8 is selected (BL8OTF mode). When A12   BC# is Low, a burst chop of 4 is selected (BC4OTF mode). Auto-Precharge can be enabled or disabled. 10<sub>B</sub> <b>BC4MRS</b> mode with fixed burst chop of 4 with <math>t_{CCD} = 4 \times n_{CK}</math>. A12   BC# is Don't care at Read or Write command time. 11<sub>B</sub> <b>TBD</b> Reserved</p>
RBT	A3	<p><b>Read Burst Type</b> 0<sub>B</sub> Nibble Sequential 1<sub>B</sub> Interleaved</p>
CL	A[6:4,2]	<p><b>CAS Latency (CL)</b> CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. <i>For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Speed Bins" on Page 31.</i> <i>Note: All other bit combinations are reserved.</i> 0000<sub>B</sub> Reserved 0010<sub>B</sub> 5 0100<sub>B</sub> 6 0110<sub>B</sub> 7 1000<sub>B</sub> 8 1010<sub>B</sub> 9 1100<sub>B</sub> 10 1110<sub>B</sub> 11</p>

Field	Bits <sup>1)</sup>	Description
TM	A7	<b>Test Mode</b> The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in this table. Programming bit A7 to a 1 places the DDR3 SDRAM into a test mode that is only used by the SDRAM manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1. 0 <sub>B</sub> Normal Mode 1 <sub>B</sub> Vendor specific test mode
DLLres	A8	<b>DLL Reset</b> The internal DLL Reset bit is self-clearing, meaning it returns back to the value of 0 after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, $t_{DLLK}$ must be met before any functions that require the DLL can be used (i.e. Read commands or synchronous ODT operations). 0 <sub>B</sub> No DLL Reset 1 <sub>B</sub> DLL Reset triggered
WR	A[11:9]	<b>Write Recovery for Auto-Precharge</b> Number of clock cycles for write recovery during Auto-Precharge. $WR_{MIN}$ in clock cycles is calculated by dividing $t_{WR(MIN)}$ (in ns) by the actual $t_{CK(AVG)}$ (in ns) and rounding up to the next integer: $WR_{MIN} [n_{CK}] = \text{Roundup}(t_{WR(MIN)}[ns] / t_{CK(AVG)}[ns])$ . The WR value in the mode register must be programmed to be equal or larger than $WR_{MIN}$ . The resulting WR value is also used with $t_{RP}$ to determine $t_{DAL}$ . Since WR of 9 and 11 is not implemented in DDR3 and the above formula results in these values, higher values have to be programmed. 000 <sub>B</sub> Reserved 001 <sub>B</sub> 5 010 <sub>B</sub> 6 011 <sub>B</sub> 7 100 <sub>B</sub> 8 101 <sub>B</sub> 10 110 <sub>B</sub> 12 111 <sub>B</sub> Reserved
PPD	A12	<b>Precharge Power-Down DLL Control</b> Active Power-Down will always be with DLL-on. Bit A12 will have no effect in this case. For Precharge Power-Down, bit A12 in MR0 is used to select the DLL usage as shown below. <b>Slow Exit.</b> DLL is frozen during precharge Power-down. Read and synchronous ODT commands are only allowed after $t_{XPDLL}$ . <b>Fast Exit.</b> DLL remains on during precharge Power-down. Any command can be applied after $t_{XP}$ , provided that other timing parameters are satisfied.

1) A13 - even if not available on a specific device - must be programmed to 0<sub>B</sub>.

## 2.4 Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength,  $R_{TT\_Nom}$  impedance, additive latency (AL), Write leveling enable and Qoff (output disable). The Mode Register MR1 is written by

asserting Low on CS#, RAS#, CAS#, WE#, High on BA0 and Low on BA1 and BA2, while controlling the states of address pins according to [Table 9](#).

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0 <sup>1)</sup>	Qoff	TDQS	0 <sup>1)</sup>	RTT <sub>nom</sub>	0 <sup>1)</sup>	Level	RTT <sub>nom</sub>	DIC	AL		RTT <sub>nom</sub>	DIC	DLL

**Table 9 - MR1 Mode Register Definition (BA[2:0]=001B)**

Field	Bits <sup>1)</sup>	Description
DLLdis	A0	<p><b>DLL Disable</b></p> <p>The DLL must be enabled for normal operation. DLL enable is required during power up initialization, after reset and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is enabled, a DLL reset must be issued afterwards. Any time the DLL is reset, <math>t_{DLLK}</math> clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the <math>t_{DQSQ}</math>, <math>t_{AON}</math>, <math>t_{AOF}</math> or <math>t_{ADC}</math> parameters. During <math>t_{DLLK}</math>, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation.</p> <p>0<sub>B</sub>    DLL is enabled 1<sub>B</sub>    DLL is disabled</p>
DIC	A[5, 1]	<p><b>Output Driver Impedance Control</b></p> <p><i>Note: All other bit combinations are reserved.</i></p> <p>00:    RZQ/6 01<sub>B</sub>    RQZ/7 (nominal 34.3 <math>\Omega</math>, with nominal RZQ = 240 <math>\Omega</math>)</p>
$R_{TT\_NOM}$	A[9, 6, 2]	<p><b>Nominal Termination Resistance of ODT</b></p> <p><b>Notes</b></p> <ol style="list-style-type: none"> <li>If <math>R_{TT\_NOM}</math> is used during Writes, only the values <math>R_{ZQ}/2</math>, <math>R_{ZQ}/4</math> and <math>R_{ZQ}/6</math> are allowed.</li> <li>In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all <math>R_{TT\_Nom}</math> settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only <math>R_{TT\_NOM}</math> settings of <math>R_{ZQ}/2</math>, <math>R_{ZQ}/4</math> and <math>R_{ZQ}/6</math> are allowed.</li> <li>All other bit combinations are reserved.</li> </ol> <p>000<sub>B</sub>    ODT disabled, <math>R_{TT\_NOM}</math> = off 001<sub>B</sub>    RTT60 = RZQ / 4 (nominal 60 <math>\Omega</math> with nominal RZQ = 240 <math>\Omega</math>) 010<sub>B</sub>    RTT120 = RZQ / 2 (nominal 120 <math>\Omega</math> with nominal RZQ = 240 <math>\Omega</math>) 011<sub>B</sub>    RTT40 = RZQ / 6 (nominal 40 <math>\Omega</math> with nominal RZQ = 240 <math>\Omega</math>) 100<sub>B</sub>    RTT20 = RZQ / 12 (nominal 20 <math>\Omega</math> with nominal RZQ = 240 <math>\Omega</math>) 101<sub>B</sub>    RTT30 = RZQ / 8 (nominal 30 <math>\Omega</math> with nominal RZQ = 240 <math>\Omega</math>)</p>

Field	Bits <sup>1)</sup>	Description
AL	A[4, 3]	<p><b>Additive Latency (AL)</b> Any read or write command is held for the time of Additive Latency (AL) before it is issued as internal read or write command.</p> <p><b>Notes</b></p> <p>1. AL has a value of CL - 1 or CL - 2 as per the CL value programmed in the MR0 register.</p> <p>00<sub>B</sub> AL = 0 (AL disabled) 01<sub>B</sub> AL = CL - 1 10<sub>B</sub> AL = CL - 2 11<sub>B</sub> Reserved</p>
Write Leveling enable	A7	<p><b>Write Leveling Mode</b></p> <p>0<sub>B</sub> <b>Write Leveling Mode</b> Disabled, Normal operation mode 1<sub>B</sub> <b>Write Leveling Mode</b> Enabled</p>
TDQS enable	A11	<p>0<sub>B</sub>: Disabled 1<sub>B</sub>: Enabled</p>
Qoff	A12	<p><b>Output Disable</b> Under normal operation, the SDRAM outputs are enabled during read operation and write leveling for driving data (Qoff bit in the MR1 is set to 0<sub>B</sub>). When the Qoff bit is set to 1<sub>B</sub>, the SDRAM outputs (DQ, DQS, DQS#) will be disabled - also during write leveling. Disabling the SDRAM outputs allows users to run write leveling on multiple ranks and to measure <math>I_{DD}</math> currents during Read operations, without including the output.</p> <p>0<sub>B</sub> Output buffer enabled 1<sub>B</sub> Output buffer disabled</p>

1) A13 - even if not available on a specific device - must be programmed to 0<sub>B</sub>.

## 2.5 Mode Register 2 (MR2)

The Mode Register MR2 stores the data for controlling refresh related features,  $R_{TT\_WR}$  impedance, and CAS write latency. The Mode Register MR2 is written by asserting Low

on CS#, RAS#, CAS#, WE#, High on BA1 and Low on BA0 and BA2, while controlling the states of address signals according to [Table 10](#).

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	Rtt_WR		0 <sup>1)</sup>	SRT	ASR	CWL			PASR		

**Table 10 - MR2 Mode Register Definition (BA[2:0]=010B)**

Field	Bits <sup>1)</sup>	Description
PASR	A[2:0]	<p><b>Partial Array Self Refresh (PASR)</b> If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified self refresh location may get lost if self refresh is entered. During non-self-refresh operation, data integrity will be maintained if <math>t_{REFI}</math> conditions are met.</p> <p>000<sub>B</sub> Full array (Banks 000<sub>B</sub> - 111<sub>B</sub>) 001<sub>B</sub> Half Array (Banks 000<sub>B</sub> - 011<sub>B</sub>) 010<sub>B</sub> Quarter Array (Banks 000<sub>B</sub> - 001<sub>B</sub>) 011<sub>B</sub> 1/8th array (Banks 000<sub>B</sub>) 100<sub>B</sub> 3/4 array (Banks 010<sub>B</sub> - 111<sub>B</sub>) 101<sub>B</sub> Half array (Banks 100<sub>B</sub> - 111<sub>B</sub>) 110<sub>B</sub> Quarter array (Banks 110<sub>B</sub> - 111<sub>B</sub>) 111<sub>B</sub> 1/8th array (Banks 111<sub>B</sub>)</p>
CWL	A[5:3]	<p><b>CAS Write Latency (CWL)</b> Number of clock cycles from internal write command to first write data in. <i>Note: All other bit combinations are reserved.</i></p> <p>000<sub>B</sub> 5 (<math>t_{CK,AVG} \geq 2.5</math> ns) 001<sub>B</sub> 6 (<math>2.5</math> ns &gt; <math>t_{CK,AVG} \geq 1.875</math> ns) 010<sub>B</sub> 7 (<math>1.875</math> ns &gt; <math>t_{CK,AVG} \geq 1.5</math> ns) 011<sub>B</sub> 8 (<math>1.5</math> ns &gt; <math>t_{CK,AVG} \geq 1.25</math> ns)</p> <p><i>Besides CWL limitations on <math>t_{CK(AVG)}</math>, there are also <math>t_{AA(MIN/MAX)}</math> restrictions that need to be observed. For details, please refer to <a href="#">Chapter 4.1 Speed Bins</a>.</i></p>
ASR	A6	<p><b>Auto Self-Refresh (ASR)</b> When enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values.</p> <p>0<sub>B</sub> Manual SR reference (SRT) 1<sub>B</sub> ASR enable</p>
SRT	A7	<p><b>Self-Refresh Temperature Range (SRT)</b> The SRT bit must be programmed to indicate <math>T_{OPER} &gt; 85^{\circ}C</math> during subsequent self refresh operation.</p> <p>0<sub>B</sub> Normal operating temperature range 1<sub>B</sub> Extended operating temperature range</p>
$R_{TT\_WR}$	A[10:9]	<p><b>Dynamic ODT mode and <math>R_{TT\_WR}</math> Pre-selection</b></p> <p><b>Notes</b></p> <p>1. All other bit combinations are reserved. The <math>R_{TT\_WR}</math> value can be applied during writes even when <math>R_{TT\_NOM}</math> is disabled. During write leveling, Dynamic ODT is not available.</p> <p>00<sub>B</sub> Dynamic ODT mode disabled 01<sub>B</sub> Dynamic ODT mode enabled with <math>R_{TT\_WR} = RZQ/4 = 60 \Omega</math> 10<sub>B</sub> Dynamic ODT mode enabled with <math>R_{TT\_WR} = RZQ/2 = 120 \Omega</math></p>

1) A13 - even if not available on a specific device - must be programmed to 0<sub>B</sub>.

## 2.6 Mode Register 3 (MR3)

The Mode Register MR3 controls Multipurpose registers and optional On-die thermal sensor (ODTS) feature. The Mode Register MR3 is written by asserting Low on CS#, RAS#, CAS#,

WE#, High on BA1 and BA0, and Low on BA2 while controlling the states of address signals according to [Table 11](#).

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	0 <sup>1)</sup>	MPR	MPR loc	

**Table 11 - MR3 Mode Register Definition (BA[2:0]=011B)**

Field	Bits <sup>1)</sup>	Description
MPR loc	A[1:0]	<b>Multi Purpose Register Location</b> 00 <sub>B</sub> Pre-defined data pattern for read synchronization 01 <sub>B</sub> RFU 10 <sub>B</sub> RFU 11 <sub>B</sub> ODTS On-Die Thermal sensor readout (optional)
MPR	A2	<b>Multi Purpose Register Enable</b> <i>Note: When MPR is disabled, MR3 A[1:0] will be ignored.</i> 0 <sub>B</sub> MPR disabled, normal memory operation 1 <sub>B</sub> Dataflow from the Multi Purpose register MPR

1) A13 - even if not available on a specific device - must be programmed to 0<sub>B</sub>.

## 2.7 Burst Order

Accesses within a given burst may be interleaved or nibble sequential depending on the programmed bit A3 in the mode register MR0.

Regarding read commands, the lower 3 column address bits CA[2:0] at read command time determine the start address for the read burst.

Regarding write commands, the burst order is always fixed. For writes with a burst length of 8, the inputs on the lower 3

column address bits CA[2:0] are ignored during the write command. For writes with a burst being chopped to 4, the input on column address 2 (CA[2]) determines if the lower or upper four burst bits are selected. In this case, the inputs on the lower 2 column address bits CA[1:0] are ignored during the write command. The following table shows burst order versus burst start address for reads and writes of bursts of 8 as well as of bursts of 4 operation (burst chop).

Table 12 - Bit Order during Burst

Burst Length	Command	Column Address 2:0			Interleaved Burst Sequence								Nibble Sequential Burst Sequence								Note	
					Bit Order within Burst								Bit Order within Burst									
		CA2	CA1	CA0	1.	2.	3.	4.	5.	6.	7.	8.	1.	2.	3.	4.	5.	6.	7.	8.		
8	READ	0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	1)	
		0	0	1	1	0	3	2	5	4	7	6	1	2	3	0	5	6	7	4	1)	
		0	1	0	2	3	0	1	6	7	4	5	2	3	0	1	6	7	4	5	1)	
		0	1	1	3	2	1	0	7	6	5	4	3	0	1	2	7	4	5	6	1)	
		1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	1)	
		1	0	1	5	4	7	6	1	0	3	2	5	6	7	4	1	2	3	0	1)	
		1	1	0	6	7	4	5	2	3	0	1	6	7	4	5	2	3	0	1	1)	
		1	1	1	7	6	5	4	3	2	1	0	7	4	5	6	3	0	1	2	1)	
		WRITE	V	V	V	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	1)2)
4 (Burst Chop Mode)	READ	0	0	0	0	1	2	3	T	T	T	T	0	1	2	3	T	T	T	T	1)3)4)	
		0	0	1	1	0	3	2	T	T	T	T	1	2	3	0	T	T	T	T	1)3)4)	
		0	1	0	2	3	0	1	T	T	T	T	2	3	0	1	T	T	T	T	1)3)4)	
		0	1	1	3	2	1	0	T	T	T	T	3	0	1	2	T	T	T	T	1)3)4)	
		1	0	0	4	5	6	7	T	T	T	T	4	5	6	7	T	T	T	T	1)3)4)	
		1	0	1	5	4	7	6	T	T	T	T	5	6	7	4	T	T	T	T	1)3)4)	
		1	1	0	6	7	4	5	T	T	T	T	6	7	4	5	T	T	T	T	1)3)4)	
		1	1	1	7	6	5	4	T	T	T	T	7	4	5	6	T	T	T	T	1)3)4)	
		WRITE	0	V	V	0	1	2	3	X	X	X	X	0	1	2	3	X	X	X	X	1)2)4)5)
	1		V	V	4	5	6	7	X	X	X	X	4	5	6	7	X	X	X	X	1)2)4)5)	

- 1) 0..7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
- 2) V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
- 3) T: output drivers for data and strobe are in high impedance.
- 4) In case of BC4MRS (burst length being fixed to 4 by MR0 setting), the internal write operation starts two clock cycles earlier than for the BL8 modes. This means that the starting point for  $t_{WR}$  and  $t_{WTR}$  will be pulled in by two clocks. In case of BC4OTF mode (burst length being selected on-the-fly via A12 | BC#), the internal write operation starts at the same point in time as a burst of 8 write operation. This means that during on-the-fly control, the starting point for  $t_{WR}$  and  $t_{WTR}$  will not be pulled in by two clocks.
- 5) X: Don't Care.

# 3 Operating Conditions and Interface Specification

## 3.1 Absolute Maximum Ratings

Table 13 - Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on $V_{DD}$ ball relative to $V_{SS}$	$V_{DD}$	-0.4	+1.975	V	1)2)
Voltage on $V_{DDQ}$ ball relative to $V_{SS}$	$V_{DDQ}$	-0.4	+1.975	V	1)2)
Voltage on any ball relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.4	+1.975	V	1)
Storage Temperature	$T_{STG}$	-55	+150	°C	1)3)

- 1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2)  $V_{DD}$  and  $V_{DDQ}$  must be within 300mV of each other at all times.  $V_{REFDQ}$  and  $V_{REFCA}$  must not be greater than  $0.6 \times V_{DDQ}$ . When  $V_{DD}$  and  $V_{DDQ}$  are less than 500 mV,  $V_{REFDQ}$  and  $V_{REFCA}$  may be equal or less than 300 mV.
- 3) Storage Temperature is the case surface temperature on the center/top side of the SDRAM. For the measurement conditions, please refer to JEDEC51-2 standard.

## 3.2 Operating Conditions

Table 14 - SDRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note <sup>1)-4)</sup>
		Min.	Max.		
$T_{OPER}$	Operating Temperature	0	+95	°C	Commercial Temperature
		-40	+95	°C	Industrial Temperature
		-40	+125	°C	Automotive A1 Temperature
		-40	+105	°C	Automotive A2 Temperature
		-40	+95	°C	Automotive A3 Temperature

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature range are the temperatures where all DRAM specification will be supported.
- 3) Above 105 °C the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$ .
- 4) When operating this product in the 105°C to 125°C  $T_{CASE}$  temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to 1. When the High Temperature Self Refresh is enabled there is an increase of  $I_{DD6}$  by approximately 50%.

Table 15 - DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	$V_{DD}$	1.425	1.5	1.575	V	1)2)
Supply Voltage for Output	$V_{DDQ}$	1.425	1.5	1.575	V	1)2)
Reference Voltage for DQ, DM inputs	$V_{REFDQ(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3)4)
Reference Voltage for ADD, CMD inputs	$V_{REFCA(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	3)4)
External Calibration Resistor connected from ZQ ball to ground	$R_{ZQ}$	237.6	240.0	242.4	$\Omega$	5)

- 1)  $V_{DDQ}$  tracks with  $V_{DD}$ . AC parameters are measured with  $V_{DD}$  and  $V_{DDQ}$  tied together
- 2) Under all conditions  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- 3) The ac peak noise on  $V_{REF}$  may not allow  $V_{REF}$  to deviate from  $V_{REF,DC}$  by more than  $\pm 1\% V_{DD}$  (for reference: approx.  $\pm 15$  mV).
- 4) For reference: approx.  $V_{DD}/2 \pm 15$  mV.
- 5) The external calibration resistor  $R_{ZQ}$  can be time-shared among DRAMs in multi-rank DIMMs.

Table 16 - Input and Output Leakage Currents

Parameter	Symbol	Condition	Rating		Unit	Note
			Min.	Max.		
Input Leakage Current	$I_L$	Any input $0 V < V_{IN} < V_{DD}$	-2	+2	$\mu A$	1)2)
Output Leakage Current	$I_{OZ}$	$0V < V_{OUT} < V_{DDQ}$	-5	+5	$\mu A$	2)3)

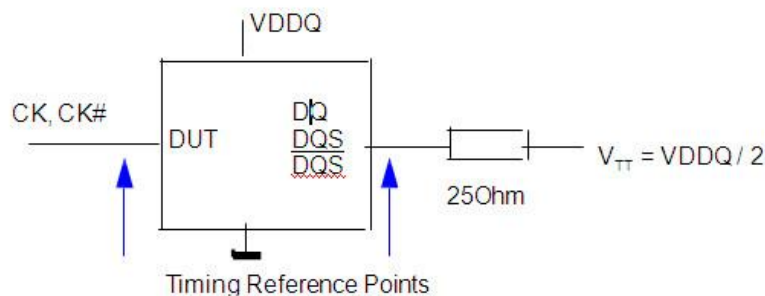
- 1) All other pins not under test = 0 V.
- 2) Values are shown per ball.
- 3) DQ's, DQS, DQS# and ODT are disabled.

### 3.3 Interface Test Conditions

Figure 3 represents the effective reference load of  $25 \Omega$  used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a

production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 3 - Reference Load for AC Timings and Output Slew Rates



The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model.

The output timing reference voltage level for single ended signals is the cross point with  $V_{TT}$ .

The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. DQS#) signal.

## 3.4 Voltage Levels

### 3.4.1 DC and AC Logic Input Levels

#### Single-Ended Signals

Table 17 shows the input levels for single-ended input signals.

Table 17 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals

Parameter	Symbol	DDR3-1066,1333,1600		Unit	Note
		Min.	Max.		
DC input logic high	$V_{IH,CA,DC100}$	$V_{REF} + 0.100$	$V_{DD}$	V	<sup>1)</sup>
DC input logic low	$V_{IL,CA,DC100}$	$V_{SS}$	$V_{REF} - 0.100$	V	<sup>1)</sup>
AC input logic high	$V_{IH,CA,AC175}$	$V_{REF} + 0.175$	See <sup>2)</sup>	V	<sup>1)</sup>
AC input logic low	$V_{IL,CA,AC175}$	See <sup>2)</sup>	$V_{REF} - 0.175$	V	<sup>1)</sup>
AC input logic high	$V_{IH,CA,AC150}$	$V_{REF} + 0.150$	See <sup>2)</sup>	V	<sup>1)</sup>
AC input logic low	$V_{IL,CA,AC150}$	See <sup>2)</sup>	$V_{REF} - 0.150$	V	<sup>1)</sup>
AC input logic high	$V_{IH,CA,AC135}$	-	-	V	<sup>1)</sup>
AC input logic low	$V_{IL,CA,AC135}$	-	-	V	<sup>1)</sup>
AC input logic high	$V_{IH,CA,AC125}$	-	-	V	<sup>1)</sup>
AC input logic low	$V_{IL,CA,AC125}$	-	-	V	<sup>1)</sup>

1) For input only pins except RESET:  $V_{REF} = V_{REF,CA(DC)}$

2) See Chapter 3.9 Overshoot and Undershoot Specification.

Table 18 - DC and AC Input Levels for Single-Ended DQ and DM Signals

Parameter	Symbol	DDR3-1066		DDR3-1333,1600		Unit	Note
		Min.	Max.	Min.	Max.		
DC input logic high	$V_{IH,DQ,DC100}$	$V_{REF} + 0.100$	$V_{DDQ}$	$V_{REF} + 0.100$	$V_{DDQ}$	V	<sup>1)</sup>
DC input logic low	$V_{IL,DQ,DC100}$	$V_{SSQ}$	$V_{REF} - 0.100$	$V_{SSQ}$	$V_{REF} - 0.100$	V	<sup>1)</sup>
AC input logic high	$V_{IH,DQ,AC175}$	$V_{REF} + 0.175$	See <sup>2)</sup>	-	-	V	<sup>1)</sup>
AC input logic low	$V_{IL,DQ,AC175}$	See <sup>2)</sup>	$V_{REF} - 0.175$	-	-	V	<sup>1)</sup>
AC input logic high	$V_{IH,DQ,AC150}$	$V_{REF} + 0.150$	See <sup>2)</sup>	$V_{REF} + 0.150$	See <sup>2)</sup>	V	<sup>1)</sup>
AC input logic low	$V_{IL,DQ,AC150}$	See <sup>2)</sup>	$V_{REF} - 0.150$	See <sup>2)</sup>	$V_{REF} - 0.150$	V	<sup>1)</sup>
AC input logic high	$V_{IH,DQ,AC135}$	-	-	-	-	V	<sup>1)</sup>
AC input logic low	$V_{IL,DQ,AC135}$	-	-	-	-	V	<sup>1)</sup>

1) For DQ and DM:  $V_{REF} = V_{REFDQ(DC)}$

2) See Chapter 3.9 Overshoot and Undershoot Specification.

### Differential Swing Requirement for Differential Signals

Table 19 shows the input levels for differential input signals.

**Table 19 - Differential swing requirement for clock (CK - CK#) and strobe (DQS - DQS#)**

Parameter	Symbol	DDR3-1066, DDR3-1333, DDR3-1600		Unit	Note
		Min.	Max.		
Differential input high	$V_{IH,DIFF}$	+0.200	See <sup>1)</sup>	V	<sup>2)</sup>
Differential input low	$V_{IL,DIFF}$	See <sup>1)</sup>	-0.200	V	<sup>2)</sup>
Differential input high AC	$V_{IH,DIFF,AC}$	$2 \times (V_{IH,AC} - V_{REF})$ <sup>3)</sup>	See <sup>1)</sup>	V	<sup>4)</sup>
Differential input low AC	$V_{IL,DIFF,AC}$	See <sup>1)</sup>	$2 \times (V_{IL,AC} - V_{REF})$ <sup>5)</sup>	V	<sup>4)</sup>

1) These values are not defined, however they single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits ( $V_{IH,DC,MAX}$ ,  $V_{IL,DC,MIN}$ ) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Chapter 3.9.

2) Used to define a differential signal slew-rate.

3) Clock: use  $V_{IH,CA,AC}$  for  $V_{IH,AC}$ . Strobe: use  $V_{IH,DQ,AC}$  for  $V_{IH,AC}$ .

4) For CK - CK# use  $V_{IH}/V_{IL,AC}$  of ADD/CMD and VREFCA; for DQS - DQS# use  $V_{IH}/V_{IL,AC}$  of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

5) Clock: use  $V_{IL,CA,AC}$  for  $V_{IL,AC}$ . Strobe: use  $V_{IL,DQ,AC}$  for  $V_{IL,AC}$ .

**Table 20 - Allowed Time Before Ringback (tDVAC) for CK - CK# and DQS - DQS#**

Slew Rate [V/ns]	DDR3-1066/1333/1600			
	$t_{DVAC}$ [ps] @ $ V_{IH/IL,DIFF,AC}  = 350mV$		$t_{DVAC}$ [ps] @ $ V_{IH/IL,DIFF,AC}  = 300mV$	
	Min.	Max.	Min.	Max.
> 4.0	75	—	175	—
4.0	57	—	170	—
3.0	50	—	167	—
2.0	38	—	119	—
1.8	34	—	102	—
1.6	29	—	81	—
1.4	22	—	54	—
1.2	note	—	19	—
1.0	note	—	note	—
<1.0	note	—	note	—

Note: Rising input differential signal shall become equal to or greater than  $V_{IHdiff}(ac)$  level and Falling input differential signal shall become equal to or less than  $V_{ILdiff}(ac)$  level.

### Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, CK#, DQS#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach  $V_{SEH.MIN} / V_{SEL.MAX}$  (approximately equal to the ac-levels ( $V_{IH.AC} / V_{IL.AC}$ ) for ADD/CMD signals) in every half-cycle. DQS, DQS# have to reach  $V_{SEH.MIN} / V_{SEL.MAX}$  (approximately the ac-levels ( $V_{IH.AC} / V_{IL.AC}$ ) for DQ signals) in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQs might be different per speed-bin etc.

E.g. if  $V_{IH150.AC} / V_{IL150.AC}$  is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and CK#.

Note that while ADD/CMD and DQ signal requirements are with respect to  $V_{ref}$ , the single-ended components of differential signals have a requirement with respect to  $V_{DD}/2$ ; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time.

For single-ended components of differential signals the requirement to reach  $V_{SEL.MAX}, V_{SEH.MIN}$  has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

**Table 21 - Each Single-Ended Levels for CK, DQS, DQS#, CK#**

Parameter	Symbol	DDR3-1066, 1333, 1600		Unit	Note
		Min.	Max.		
Single-ended high-level for strobes	$V_{SEH}$	(VDDQ/2)+0.175	See <sup>1)</sup>	V	2)3)
Single-ended high-level for CK, CK#	$V_{SEH}$	(VDD/2)+0.175	See <sup>1)</sup>	V	
Single-ended low-level for strobes	$V_{SEL}$	See <sup>1)</sup>	(VDDQ/2)-0.175	V	
Single-ended low-level for CK, CK#	$V_{SEL}$	See <sup>1)</sup>	(VDD/2)-0.175	V	

1) These values are not defined, however they single-ended signals CK, CK#, DQS, DQS# need to be within the respective limits ( $V_{IH.DC.MAX}, V_{IL.DC.MIN}$ ) for single-ended signals as well as the limitations for overshoot and undershoot.

2) For CK, CK# use  $V_{IH.AC} / V_{IL.AC}$  of ADD/CMD; for strobes (DQS, DQS#) use  $V_{IH.AC} / V_{IL.AC}$  of DQs.

3)  $V_{IH.AC} / V_{IL.AC}$  for DQs is based on  $V_{REFDQ}$ ;  $V_{IH.AC} / V_{IL.AC}$  for ADD/CMD is based on  $V_{REFCA}$ ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

**Table 22 - Cross Point Voltage for Differential Input Signals (CK, DQS)**

Symbol	Parameter	DDR3-1066, 1333, 1600, 1866		Unit	Note
		Min.	Max.		
$V_{IX}$	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK – CK#	-150	150	mV	2)
		-175	175	mV	1)
$V_{IX}$	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS –DQS#	-150	150	mV	2)

1) Extended range for  $V_{IX}$  is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic, have a single-ended swing  $V_{SEL}/V_{SEH}$  (see [Single-Ended Requirements for Differential Signals](#)) of at least  $V_{DD}/2 \pm 250$  mV and if the differential slew rate of CK - CK# is larger than 3 V/ns.

2) the relation between  $V_{IX}$  min/max and  $V_{SEL}/V_{SEH}$  should satisfy following:  
 $V_{DD}/2 + V_{IX}(min) - V_{SEL} \geq 25$ mv  
 $V_{SEH} - (V_{DD}/2 + V_{IX}(max)) \geq 25$ mv

### 3.4.2 DC and AC Output Measurements Levels

Table 23 - DC and AC Output Levels for Single-Ended Signals

Parameter	Symbol	DDR3-1066,1333,1600	Unit	Note
DC output high measurement level (for IV curve linearity)	$V_{OH.DC}$	$0.8 \times V_{DDQ}$	V	
DC output mid measurement level (for IV curve linearity)	$V_{OM.DC}$	$0.5 \times V_{DDQ}$	V	
DC output low measurement level (for IV curve linearity)	$V_{OL.DC}$	$0.2 \times V_{DDQ}$	V	
AC output high measurement level (for output slew rate)	$V_{OH.AC}$	$V_{TT} + 0.1 \times V_{DDQ}$	V	1)
AC output low measurement level (for output slew rate)	$V_{OL.AC}$	$V_{TT} - 0.1 \times V_{DDQ}$	V	1)

1) Background: the swing of  $\pm 0.1 \times V_{DDQ}$  is based on approximately 50% of the static differential output high or low swing with a driver impedance of  $40 \Omega$  and an effective test load of  $25 \Omega$  to  $V_{TT} = V_{DDQ} / 2$ .

Table 24 - AC Output Levels for Differential Signals

Parameter	Symbol	Value	Unit	Note
AC differential output high measurement level (for output slew rate)	$V_{OH.DIFF.AC}$	$+0.2 \times V_{DDQ}$	V	1)
AC differential output low measurement level (for output slew rate)	$V_{OL.DIFF.AC}$	$-0.2 \times V_{DDQ}$	V	1)
Deviation of the output cross point voltage from the termination voltage	$V_{OX.AC}$	<b>Min.</b>	mV	2)
		$V_{REF} - 150$		
		<b>Max.</b>		
		$V_{REF} - 150$		

1) Background: the swing of  $\pm 0.2 \times V_{DDQ}$  is based on approximately 50% of the static differential output high or low swing with a driver impedance of  $40 \Omega$  and an effective test load of  $25 \Omega$  to  $V_{TT} = V_{DDQ} / 2$  at each of the differential outputs.

2) With an effective test load of  $25 \Omega$  to  $V_{TT} = V_{DDQ} / 2$  at each of the differential outputs (see [Chapter 3.3 Interface Test Conditions](#)).

## 3.5 Output Slew Rates

Table 25 - Output Slew Rates

Parameter	Symbol	DDR3-1066 /-1333 /-1600		Unit	Note
		Min.	Max.		
Single-ended Output Slew Rate	SRQse	2.5	5	V / ns	1)2)
Differential Output Slew Rate	SRQdiff	5	10	V / ns	

1) For  $R_{ON} = R_{ZQ}/7$  settings only.

2) Background for Symbol Nomenclature: SR: Slew Rate; Q: Query Output; se: single-ended; diff: differential.

### 3.6 ODT DC Impedance and Mid-Level Characteristics

Table 26 provides the ODT DC impedance and mid-level characteristics.

Table 26 - ODT DC Impedance and Mid-Level Characteristics

Symbol	Description	V <sub>OUT</sub> Condition	Min.	Nom.	Max.	Unit	Note
R <sub>TT120</sub>	R <sub>TT</sub> effective = 120 Ω	V <sub>IL,AC</sub> and V <sub>IH,AC</sub>	0.9	1.0	1.6	R <sub>ZQ</sub> /2	1)2)3)4)
R <sub>TT60</sub>	R <sub>TT</sub> effective = 60 Ω		0.9	1.0	1.6	R <sub>ZQ</sub> /4	1)2)3)4)
R <sub>TT40</sub>	R <sub>TT</sub> effective = 40 Ω		0.9	1.0	1.6	R <sub>ZQ</sub> /6	1)2)3)4)
R <sub>TT30</sub>	R <sub>TT</sub> effective = 30 Ω		0.9	1.0	1.6	R <sub>ZQ</sub> /8	1)2)3)4)
R <sub>TT20</sub>	R <sub>TT</sub> effective = 20 Ω		0.9	1.0	1.6	R <sub>ZQ</sub> /12	1)2)3)4)
ΔV <sub>M</sub>	Deviation of V <sub>M</sub> with respect to V <sub>DDQ</sub> / 2	floating	-5	—	+5	%	1)2)3)4)5)

- 1) With R<sub>ZQ</sub> = 240 Ω.
- 2) Measurement definition for R<sub>TT</sub> : Apply V<sub>IH,AC</sub> and V<sub>IL,AC</sub> to test ball separately, then measure current I (V<sub>IH,AC</sub>) and I (V<sub>IL,AC</sub>) respectively.  
 $R_{TT} = [V_{IH,AC} - V_{IL,AC}] / [I(V_{IH,AC}) - I(V_{IL,AC})]$
- 3) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the [ODT DC Impedance Sensitivity on Temperature and Voltage Drifts](#).
- 4) The tolerance limits are specified under the condition that V<sub>DDQ</sub> = V<sub>DD</sub> and that V<sub>SSQ</sub> = V<sub>SS</sub>.
- 5) Measurement Definition for ΔV<sub>M</sub>: Measure voltage (V<sub>M</sub>) at test ball (midpoint) with no load: ΔV<sub>M</sub> = (2 × V<sub>M</sub> / V<sub>DDQ</sub> - 1) × 100%.

### 3.7 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts

If temperature and/or voltage change after calibration, the tolerance limits widen for R<sub>TT</sub> according to the following tables.

The following definitions are used:

$$\Delta T = T - T \text{ (at calibration)}$$

$$\Delta V = V_{DDQ} - V_{DDQ} \text{ (at calibration)}$$

$$V_{DD} = V_{DDQ}$$

Table 27 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift

Symbol	Value		Unit	Note
	Min.	Max.		
R <sub>TT</sub>	0.9 - dR <sub>TT</sub> dT x  ΔT  - dR <sub>TT</sub> dV x  ΔV	1.6 + dR <sub>TT</sub> dT x  ΔT  + dR <sub>TT</sub> dV x  ΔV	R <sub>ZQ</sub> / TISF <sub>R<sub>TT</sub></sub>	1)

- 1) TISF<sub>R<sub>TT</sub></sub>: Termination Impedance Scaling Factor for R<sub>TT</sub>:  
 $TISF_{R_{TT}} = 12$  for R<sub>TT020</sub>  
 $TISF_{R_{TT}} = 8$  for R<sub>TT030</sub>  
 $TISF_{R_{TT}} = 6$  for R<sub>TT040</sub>  
 $TISF_{R_{TT}} = 4$  for R<sub>TT060</sub>  
 $TISF_{R_{TT}} = 2$  for R<sub>TT120</sub>

Table 28 - ODT DC Impedance Sensitivity Parameters

Symbol	Value		Unit	Note
	Min.	Max.		
dR <sub>TT</sub> dT	0	1.5	%/°C	1)
dR <sub>TT</sub> dV	0	0.15	%/mV	

- 1) These parameters may not be subject to production test. They are verified by design and characterization.

## 3.8 Interface Capacitance

Definition and values for interface capacitances are provided in the following table.

**Table 29 - Interface Capacitance Values**

Parameter	Signals	Symbol	DDR3–1066		DDR3–1333		DDR3–1600		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Input/Output Capacitance	DQ, DM, DQS, DQS#	$C_{IO}$	1.4	2.7	1.4	2.5	1.4	2.3	pF	1)2)3)
Input Capacitance	CK, CK#	$C_{CK}$	0.8	1.6	0.8	1.4	0.8	1.4	pF	2)3)
Input Capacitance Delta	CK, CK#	$C_{DCK}$	0	0.15	0	0.15	0	0.15	pF	2)3)4)
Input/Output Capacitance delta DQS and DQS#	DQS, DQS#	$C_{DDQS}$	0	0.2	0	0.15	0	0.15	pF	2)3)5)
Input Capacitance	All other input-only pins	$C_I$	0.75	1.35	0.75	1.3	0.75	1.3	pF	2)3)6)
Input Capacitance delta	All CTRL input-only pins	$C_{DL\_CTRL}$	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2)3)7)8)
Input Capacitance delta	All ADD and CMD input-only pins	$C_{DL\_ADD\_CMD}$	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2)3)9)10)
Input/Output Capacitance delta	DQ, DM, DQS, DQS#	$C_{DIO}$	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2)3)11)
ZQ Capacitance	ZQ	$C_{ZQ}$	-	3	-	3	-	3	pF	12)

- 1) Although the DM signal has different function, the loading matches DQ and DQS
- 2) This parameter is not subject to production test. It is verified by design and characterization. Capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  applied and all other balls floating (except the ball under test, CKE, RESET# and ODT as necessary).  $V_{DD} = V_{DDQ} = 1.5\text{ V}$ ,  $V_{BIAS} = V_{DD}/2$  and on-die termination off
- 3) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
- 4) Absolute value of  $C_{CK} - C_{CK\#}$
- 5) Absolute value of  $C_{IO,DQS} - C_{IO,DQS\#}$
- 6)  $C_I$  applies to ODT, CS#, CKE, A[15:0], BA[2:0], RAS#, CAS#, WE#
- 7)  $C_{DL\_CTRL}$  applies to ODT, CS# and CKE
- 8)  $C_{DL\_CTRL} = C_{I,CTRL} - 0.5 \times (C_{I,CK} + C_{I,CK\#})$
- 9)  $C_{DL\_ADD\_CMD}$  applies to A[15:0], BA[2:0], RAS#, CAS# and WE#
- 10)  $C_{DL\_ADD\_CMD} = C_{I,ADD\_CMD} - 0.5 \times (C_{I,CK} + C_{I,CK\#})$
- 11)  $C_{DIO} = C_{IO,DQ,DM} - 0.5 \times (C_{IO,DQS} + C_{IO,DQS\#})$
- 12) Maximum external load capacitance on ZQ signal: 5 pF

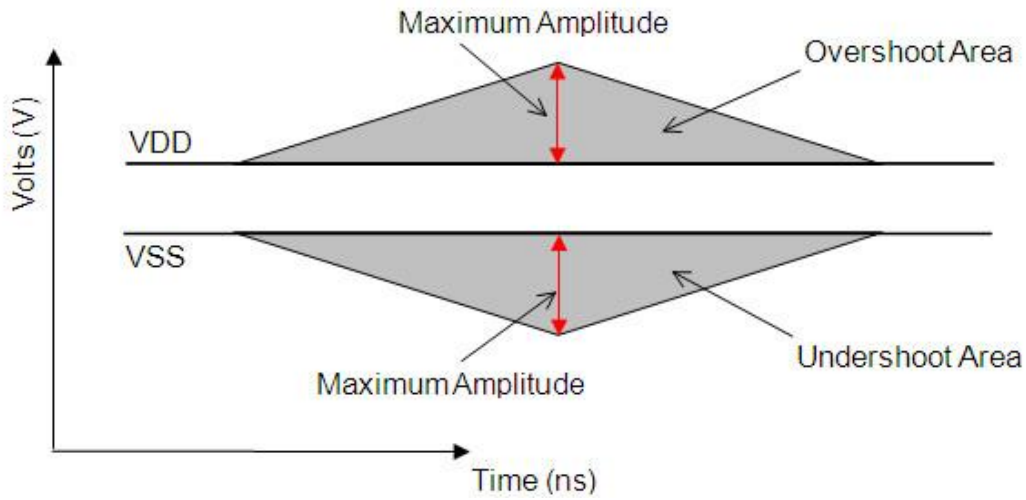
### 3.9 Overshoot and Undershoot Specification

**Table 30 - AC Overshoot / Undershoot Specification for Address and Control Signals**

Parameter	DDR3-1066	DDR3-1333	DDR3-1600	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	V	<sup>1)</sup>
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	V	<sup>1)</sup>
Maximum overshoot area above $V_{DD}$	0.5	0.4	0.33	V × ns	<sup>1)</sup>
Maximum undershoot area below $V_{SS}$	0.5	0.4	0.33	V × ns	<sup>1)</sup>

1) Applies for the following signals: A[14:0], BA[3:0], CS#, RAS#, CAS#, WE#, CKE and ODT

**Figure 4 - AC Overshoot / Undershoot Definitions for Address and Control Signals**

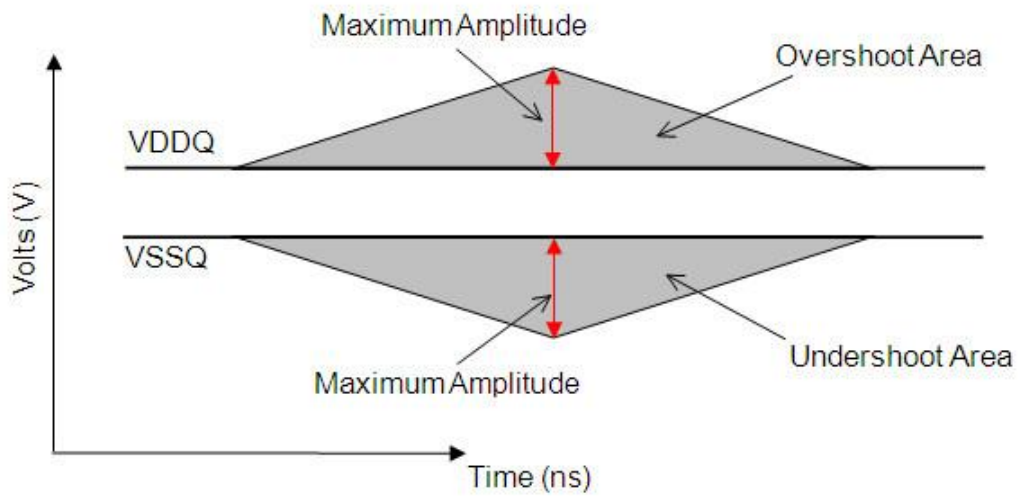


**Table 31 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals**

Parameter	DDR3-1066	DDR3-1333	DDR3-1600	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	V	1)
Maximum overshoot area above $V_{DDQ}$	0.19	0.15	0.13	V × ns	1)
Maximum undershoot area below $V_{SSQ}$	0.19	0.15	0.13	V × ns	1)

1) Applies for CK, CK#, DQ, DQS, DQS# & DM

**Figure 5 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals**



## 4 Speed Bins, AC Timing and IDD

### 4.1 Speed Bins

The following tables show DDR3 speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter. For availability and ordering information of products for a specific speed bin, please see [Table 1](#).

The absolute specification for all speed bins is  $T_{OPER}$  and  $V_{DD} = V_{DDQ} = 1.5 \text{ V} \pm 0.075 \text{ V}$ . In addition the following general notes apply.

**Table 32 - DDR3-1066 Speed Bins**

Speed Bin			DDR3-1066F		Unit	Notes	
CL-nRCD-nRP			7-7-7				
Parameter	Symbol	Min	Max				
Internal read command to first data	tAA	13.125	20	ns			
Active to read or write delay time	tRCD	13.125	-	ns			
Precharge command period	tRP	13.125	-	ns			
Active to active/auto-refresh command time	tRC	50.625	-	ns			
Active to precharge command period	tRAS	37.5	9 * tREFI	ns		9	
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,5
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,5
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3
Supported CL setting			5, 6, 7, 8		nCK		
Supported CWL setting			5, 6		nCK		

Table 33 - DDR3-1333 Speed Bins

Speed Bin			DDR3-1333H		Unit	Notes	
CL-nRCD-nRP			9-9-9				
Parameter	Symbol		Min	Max			
Internal read command to first data	tAA		13.5	20	ns	10	
Active to read or write delay time	tRCD		13.5	-	ns	10	
Precharge command period	tRP		13.5	-	ns	10	
Active to active/auto-refresh command time	tRC		49.5	-	ns	10	
Active to precharge command period	tRAS		36	9 * tREFI	ns	9	
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,6
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,6
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,6
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,6
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3
	Supported CL setting			5, 6, 7, 8, 9, 10		nCK	
	Supported CWL setting			5, 6, 7		nCK	

Table 34 - DDR3-1600 Speed Bins

Speed Bin			DDR3-1600K		Unit	Notes	
CL-nRCD-nRP			11-11-11				
Parameter	Symbol	Min	Max				
Internal read command to first data	tAA	13.75	20	ns	10		
Active to read or write delay time	tRCD	13.75	-	ns	10		
Precharge command period	tRP	13.75	-	ns	10		
Active to active/auto-refresh command time	tRC	48.75	-	ns	10		
Active to precharge command period	tRAS	35	9 * tREFI	ns	9		
Average Clock Cycle Time	CL = 5	CWL = 5	tCK(avg)	3.0	3.3	ns	1,2,3,7
		CWL = 6,7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 6	CWL = 5	tCK(avg)	2.5	3.3	ns	1,2,3,7
		CWL = 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 7	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,7
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 8	CWL = 5	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 6	tCK(avg)	1.875	< 2.5	ns	1,2,3,7
		CWL = 7	tCK(avg)	Reserved	Reserved	ns	4
	CL = 9	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3,7
	CL = 10	CWL = 5, 6	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 7	tCK(avg)	1.5	< 1.875	ns	1,2,3,7
		CWL = 8	tCK(avg)	Reserved	Reserved	ns	4
	CL = 11	CWL = 5, 6,7	tCK(avg)	Reserved	Reserved	ns	4
		CWL = 8	tCK(avg)	1.25	< 1.5	ns	1,2,3
Supported CL setting			5, 6, 7, 8, 9, 10,11		nCK		
Supported CWL setting			5, 6, 7, 8		nCK		

## Note:

1. The CL setting and CWL setting result in tCK(avg) Min and tCK(avg) Max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg) Min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next "Supported CL".
3. tCK(avg) Max limits: Calculate tCK(avg) = tAA Max / CL Selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(avg) Max corresponding to CL selected.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to production tests but verified by design/characterization.
9. tREFI depends on operating case temperature (Tcase).
10. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting downshift to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting downshift to DDR3-1333H or DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns, (tRASmin + tRPmin = 36ns + 13.125ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35ns + 13.125ns) for DDR3-1600K.

## 4.2 AC Timing Characteristics

( VDD =1.5V±0.075V; VDDQ =1.5V±0.075V )

Table 35 - AC Timing parameters

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max	Min	Max		
Average clock cycle time	$t_{CK}(avg)$	Please refer Speed Bins						ps	
Minimum clock cycle time (DLL-off mode)	$t_{CK}$ (DLL-off)	8	-	8	-	8	-	ns	6
Average CK high level width	$t_{CH}(avg)$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK}(avg)$	
Average CK low level width	$t_{CL}(avg)$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK}(avg)$	
Active Bank A to Active Bank B command period	$t_{RRD}$	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-	ns	1KB e
		max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	ns	2KB e
Four activate window(1KB)	$t_{FAW}$	37.5	-	30	-	30	-	ns	e
Four activate window(2KB)	$t_{FAW}$	50	-	45	-	40	-	ns	e
Address and Control input hold time (VIH/VIL (DC100) levels)	$t_{IH}(base)$ DC100	200	-	140	-	120	-	ps	16,b
Address and Control input setup time (VIH/VIL (AC175) levels)	$t_{IS}(base)$ AC175	125	-	65	-	45	-	ps	16,b
Address and Control input setup time (VIH/VIL (AC150) levels)	$t_{IS}(base)$ AC150	275	-	190	-	170	-	ps	16,24,b
DQ and DM input hold time (VIH/VIL (DC100) levels)	$t_{DH}(base)$ DC100	100	-	65	-	45	-	ps	17,d
DQ and DM input setup time (VIH/VIL (AC175) levels)	$t_{DS}(base)$ AC175	25	-	-	-	-	-	ps	17,d
DQ and DM input setup time (VIH/VIL (AC150) levels)	$t_{DS}(base)$ AC150	75	-	30	-	10	-	ps	17,d
Control and Address Input pulse width for each input	$t_{IPW}$	780	-	620	-	560	-	ps	25
DQ and DM Input pulse width for each input	$t_{DIPW}$	490	-	400	-	360	-	ps	25
DQ high impedance time	$t_{HZ}(DQ)$	-	300	-	250	-	225	ps	13,14,f
DQ low impedance time	$t_{LZ}(DQ)$	-600	300	-500	250	-450	225	ps	13,14,f
DQS, DQS# high impedance time (RL + BL/2 reference)	$t_{HZ}(DQS)$	-	300	-	250	-	225	ps	13,14,f
DQS, DQS# low impedance time (RL - 1 reference)	$t_{LZ}(DQS)$	-600	300	-500	250	-450	225	ps	13,14,f
DQS, DQS# to DQ Skew, per group, per access	$t_{DQSQ}$	-	150	-	125	-	100	ps	12,13
CAS# to CAS# command delay	$t_{CCD}$	4	-	4	-	4	-	nCK	
DQ output hold time from DQS, DQS#	$t_{QH}$	0.38	-	0.38	-	0.38	-	$t_{CK}(avg)$	12,13,g
DQS, DQS# rising edge output access time from rising CK, CK#	$t_{DQSCK}$	-300	300	-255	255	-225	225	ps	12,13,f
DQS latching rising transitions to associated clock edges	$t_{DQSS}$	-0.25	0.25	-0.25	0.25	-0.27	0.27	$t_{CK}(avg)$	c
DQS falling edge hold time from rising CK	$t_{DSH}$	0.2	-	0.2	-	0.18	-	$t_{CK}(avg)$	29,c

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQS falling edge setup time to rising CK	t <sub>DSS</sub>	0.2	-	0.2	-	0.18	-	t <sub>CK</sub> (avg)	29,c
DQS input high pulse width	t <sub>DQSH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub> (avg)	27,28
DQS input low pulse width	t <sub>DQSL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub> (avg)	26,28
DQS output high time	t <sub>QSH</sub>	0.38	-	0.40	-	0.40	-	t <sub>CK</sub> (avg)	12,13,g
DQS output low time	t <sub>QSL</sub>	0.38	-	0.40	-	0.40	-	t <sub>CK</sub> (avg)	12,13,g
Mode register set command cycle time	t <sub>MRD</sub>	4	-	4	-	4	-	nCK	
Mode register set command update delay	t <sub>MOD</sub>	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	ns	
Read preamble time	t <sub>RPRE</sub>	0.9	-	0.9	-	0.9	-	t <sub>CK</sub> (avg)	13,19,g
Read postamble time	t <sub>RPST</sub>	0.3	-	0.3	-	0.3	-	t <sub>CK</sub> (avg)	11,13,g
Write preamble time	t <sub>WPRE</sub>	0.9	-	0.9	-	0.9	-	t <sub>CK</sub> (avg)	1
Write postamble time	t <sub>WPST</sub>	0.3	-	0.3	-	0.3	-	t <sub>CK</sub> (avg)	1
Write recovery time	t <sub>WR</sub>	15	-	15	-	15	-	ns	18,e
Auto precharge write recovery + Precharge time	t <sub>DAL</sub> (min)	WR + roundup [t <sub>RP</sub> / t <sub>CK</sub> (avg)]						nCK	
Multi-purpose register recovery time	t <sub>MRR</sub>	1	-	1	-	1	-	nCK	22
Internal write to read command delay	t <sub>WTR</sub>	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	ns	18,e
Internal read to precharge command delay	t <sub>RTP</sub>	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	ns	e
Minimum CKE low width for Self-refresh entry to exit timing	t <sub>CKESR</sub>	t <sub>CKE</sub> (min) + 1nCK	-	t <sub>CKE</sub> (min) + 1nCK	-	t <sub>CKE</sub> (min) + 1nCK	-	ns	
Valid clock requirement after Self- refresh entry or Power-down entry	t <sub>CKSRE</sub>	max(5nCK, 10 ns)	-	max(5nCK, 10 ns)	-	max(5nCK, 10 ns)	-	ns	
Valid clock requirement before Self- refresh exit or Power-down exit	t <sub>CKSRX</sub>	max(5nCK, 10 ns)	-	max(5nCK, 10 ns)	-	max(5nCK, 10 ns)	-	ns	
Exit Self-refresh to commands not requiring a locked DLL	t <sub>Xs</sub>	max(5nCK, t <sub>RFC</sub> (min) + 10ns)	-	max(5nCK, t <sub>RFC</sub> (min) + 10ns)	-	max(5nCK, t <sub>RFC</sub> (min) + 10ns)	-	ns	
Exit Self-refresh to commands requiring a locked DLL	t <sub>XSDLL</sub>	t <sub>DLLK</sub> (min)	-	t <sub>DLLK</sub> (min)	-	t <sub>DLLK</sub> (min)	-	nCK	
Auto-refresh to Active/Auto-refresh command time	t <sub>RFC</sub>	110	-	110	-	110	-	ns	
Average Periodic Refresh Interval -40°C ≤ T <sub>c</sub> < +85°C	t <sub>REFI</sub>	-	7.8	-	7.8	-	7.8	μs	
Average Periodic Refresh Interval +85°C < T <sub>c</sub> ≤ +95°C	t <sub>REFI</sub>	-	3.9	-	3.9	-	3.9	μs	
CKE minimum high and low pulse width	t <sub>CKE</sub>	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	max(3nCK, 5ns)	-	ns	

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max	Min	Max		
Exit reset from CKE high to a valid command	$t_{XPR}$	$\max(5nCK, t_{RFC}(\min)+10ns)$	-	$\max(5nCK, t_{RFC}(\min)+10ns)$	-	$\max(5nCK, t_{RFC}(\min)+10ns)$	-	ns	
DLL locking time	$t_{DLLK}$	512	-	512	-	512	-	nCK	
Power-down entry to exit time	$t_{PD}$	$t_{CKE}(\min)$	$9 \cdot t_{REFI}$	$t_{CKE}(\min)$	$9 \cdot t_{REFI}$	$t_{CKE}(\min)$	$9 \cdot t_{REFI}$		15
Exit precharge power-down with DLL frozen to commands requiring a locked DLL	$t_{XPDLL}$	$\max(10nCK, 24ns)$	-	$\max(10nCK, 24ns)$	-	$\max(10nCK, 24ns)$	-	ns	2
Exit power-down with DLL on to any valid command; Exit precharge power-down with DLL frozen to commands not requiring a locked DLL	$t_{XP}$	$\max(3nCK, 7.5ns)$	-	$\max(3nCK, 6ns)$	-	$\max(3nCK, 6ns)$	-	ns	
Command pass disable delay	$t_{CPDED}$	1	-	1	-	1	-	nCK	
Timing of ACT command to Power-down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power-down entry	$t_{PRPDEN}$	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power-down entry	$t_{RDPDEN}$	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRPDEN}$	WL + 4 + [tWR/tCK( avg)]	-	WL + 4 + [tWR/tCK( avg)]	-	WL + 4 + [tWR/tCK( avg)]	-	nCK	9
Timing of WR command to Power-down entry (BC4MRS)	$t_{WRPDEN}$	WL + 2 + [tWR/tCK( avg)]	-	WL + 2 + [tWR/tCK( avg)]	-	WL + 2 + [tWR/tCK( avg)]	-	nCK	9
Timing of WRA command to Power-down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL+4 +WR+1	-	WL+4 +WR+1	-	WL+4 +WR+1	-	nCK	10
Timing of WRA command to Power-down entry (BC4MRS)	$t_{WRAPDEN}$	WL+2 +WR+1	-	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK	10
Timing of REF command to Power-down entry	$t_{REFPDEN}$	1	-	1	-	1	-	nCK	20,21
Timing of MRS command to Power-down entry	$t_{MRSPDEN}$	$t_{MOD}(\min)$	-	$t_{MOD}(\min)$	-	$t_{MOD}(\min)$	-		
RTT turn-on	$t_{AON}$	-300	300	-250	250	-225	225	ps	7,f
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	$t_{AONPD}$	2	8.5	2	8.5	2	8.5	ns	
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	$t_{AOF}$	0.3	0.7	0.3	0.7	0.3	0.7	tck(avg)	8,f
Asynchronous RTT turn-off delay (Power-down with DLL frozen)	$t_{AOFPD}$	2	8.5	2	8.5	2	8.5	ns	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
RTT dynamic change skew	$t_{ADC}$	0.3	0.7	0.3	0.7	0.3	0.7	tck(avg)	f

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Unit	Note
		Min	Max	Min	Max	Min	Max		
Power-up and reset calibration time	$t_{ZQinit}$	max(512nCK,640ns)	-	max(512nCK,640ns)	-	max(512nCK,640ns)	-	ns	
Normal operation full calibration time	$t_{ZQoper}$	max(256nCK,320ns)	-	max(256nCK,320ns)	-	max(256nCK,320ns)	-	ns	
Normal operation short calibration time	$t_{ZQCS}$	max(64nCK,80ns)	-	max(64nCK,80ns)	-	max(64nCK,80ns)	-	ns	23
First DQS pulse rising edge after write leveling mode is programmed	$t_{WLMRD}$	40	-	40	-	40	-	nCK	3
DQS, DQS# delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	$t_{WLS}$	245	-	195	-	165	-	ps	
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	$t_{WLH}$	245	-	195	-	165	-	ps	
Write leveling output delay	$t_{WLO}$	0	9	0	9	0	7.5	ns	
Write leveling output error	$t_{WLOE}$	0	2	0	2	0	2	ns	
Absolute clock period	$t_{CK(abs)}$	$t_{CK(avg)min} + t_{JIT(per)min}$	$t_{CK(avg)max} + t_{JIT(per)max}$	$t_{CK(avg)min} + t_{JIT(per)min}$	$t_{CK(avg)max} + t_{JIT(per)max}$	$t_{CK(avg)min} + t_{JIT(per)min}$	$t_{CK(avg)max} + t_{JIT(per)max}$	ps	
Absolute clock high pulse width	$t_{CH(abs)}$	0.43	-	0.43	-	0.43	-	$t_{CK(avg)}$	30
Absolute clock low pulse width	$t_{CL(abs)}$	0.43	-	0.43	-	0.43	-	$t_{CK(avg)}$	31
Clock period jitter	$t_{JIT(per)}$	-90	90	-80	80	-70	70	ps	
Clock period jitter during DLL locking period	$t_{JIT(per,lck)}$	-80	80	-70	70	-60	60	ps	
Cycle to cycle period jitter	$t_{JIT(cc)}$	-	180	-	160	-	140	ps	
Cycle to cycle period jitter during DLL locking period	$t_{JIT(cc,lck)}$	-	160	-	140	-	120	ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	-132	132	-118	118	-103	103	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	-157	157	-140	140	-122	122	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	-175	175	-155	155	-136	136	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	-188	188	-168	168	-147	147	ps	
Cumulative error across 6 cycles	$t_{ERR(6per)}$	-200	200	-177	177	-155	155	ps	
Cumulative error across 7 cycles	$t_{ERR(7per)}$	-209	209	-186	186	-163	163	ps	
Cumulative error across 8 cycles	$t_{ERR(8per)}$	-217	217	-193	193	-169	169	ps	
Cumulative error across 9 cycles	$t_{ERR(9per)}$	-224	224	-200	200	-175	175	ps	
Cumulative error across 10 cycles	$t_{ERR(10per)}$	-231	231	-205	205	-180	180	ps	
Cumulative error across 11 cycles	$t_{ERR(11per)}$	-237	237	-210	210	-184	184	ps	
Cumulative error across 12 cycles	$t_{ERR(12per)}$	-242	242	-215	215	-188	188	ps	
Cumulative error across n = 13,14,...49,50 cycles	$t_{ERR(nper)}$	$t_{ERR(nper)min} = (1 + 0.68\ln(n)) * t_{JIT(per)min}$ $t_{ERR(nper)max} = (1 + 0.68\ln(n)) * t_{JIT(per)max}$						ps	32

## Notes for AC Electrical Characteristics

### Jitter Notes

**Specific Note a:** Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD = 4[nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.

**Specific Note b:** These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

**Specific Note c:** These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

**Specific Note d:** These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing.

**Specific Note e:** For these parameters, the DDR3 SDRAM device supports tPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

**Specific Note f:** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 ≤ m ≤ 12. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!) Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 ≤ n ≤ 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 ≤ n ≤ 12.

**Specific Note g:** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

### NOTE:

- Actual value dependent upon measurement level definitions.
- Commands requiring a locked DLL are: READ (and READA) and synchronous ODT commands.
- The max values are system dependent.
- WR as programmed in mode register.
- Value must be rounded-up to next higher integer value.
- There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
- ODT turn on time (min.) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time (max.) is when the ODT resistance is fully on. Both are measured from ODTLon.
- ODT turn-off time (min.) is when the device starts to turn-off ODT resistance. ODT turn-off time (max.) is when the bus is in high impedance. Both are measured from ODTLoff.
- tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
- WR in clock cycles as programmed in MR0.
- The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
- Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
- Value is only valid for RON34.
- Single ended signal parameter. Refer to the section of tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Notes for definition and measurement method.
- tREFI depends on temperature (Tc).
- tIS(base) and tIH(base) values are for 1V/ns command/address single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET#, VREF(DC) = VREFCA(DC). See Address / Command Setup, Hold and Derating section.
- tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VREFDQ(DC). For input only pins except RESET, VREF(DC) = VREFCA(DC). See Data Setup, Hold and Slew Rate Derating section.
- Start of internal write transaction is defined as follows ;  
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.  
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.

19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operation.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the "Output Driver Voltage and Temperature Sensitivity" and "ODT Voltage and Temperature Sensitivity" tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

24. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns].
25. Pulse width of a input signal is defined as the width between the first crossing of VREF(DC) and the consecutive crossing of VREF(DC).
26. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.
27. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.
28. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
29. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.
30. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
31. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
32. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

## 4.3 IDD Specification

(VDD = 1.5V±0.075V; VDDQ =1.5V±0.075V)

**Table 36 - IDD Specification**

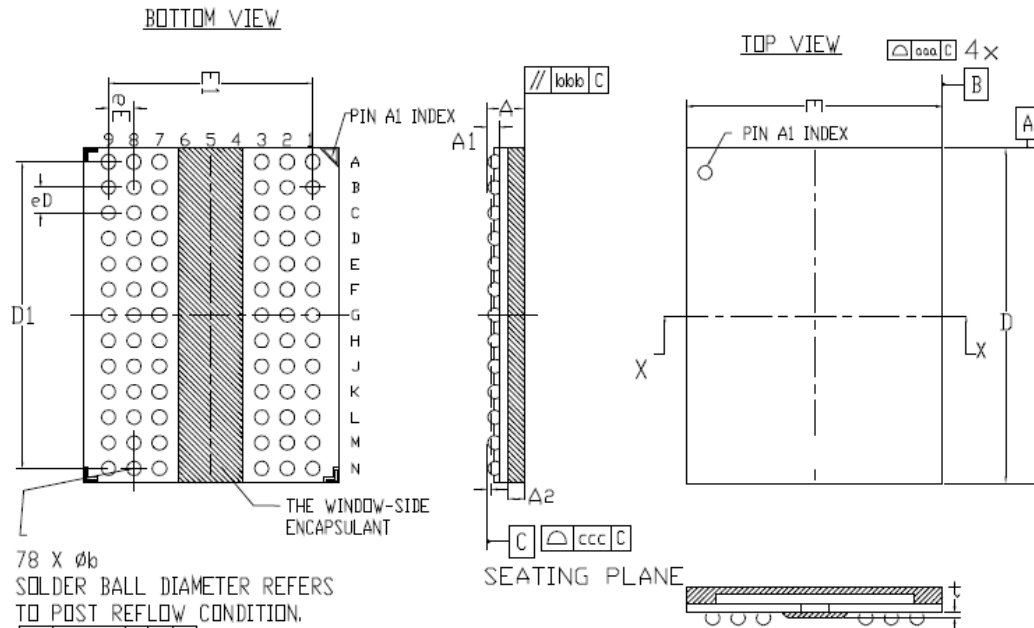
Conditions	Symbol	Data rate (Mbps)	IDD max. (x8)	IDD max. (X16)	Unit
			95°C <sub>2</sub> )	95°C <sub>2</sub> )	
<b>Operating One Bank Active-Precharge Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, CL: see timing used table; BL: 8; AL: 0; CS#: High between ACT and PRE; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD0	1600	80	100	mA
1333		75	95		
1066		70	90		
<b>Operating One Bank Active-Read-Precharge Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see timing used table; BL: 8; AL: 0; CS#: High between ACT, RD and PRE; Command, Address, Data IO: partially toggling; DM:stable at 0; Bank Activity: Cycling with one bank active at a time; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD1	1600	95	130	mA
1333		90	125		
1066		85	115		
<b>Precharge Power-Down Current Slow Exit;</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit	IDD2P0	1600	12	12	mA
1333					
1066					
<b>Precharge Power-Down Current Fast Exit;</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit	IDD2P1	1600	45	50	mA
1333		40	45		
1066		35	40		
<b>Precharge Standby Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2N	1600	60	65	mA
1333		55	60		
1066		50	55		
<b>Precharge Standby ODT Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: toggling	IDD2NT	1600	65	65	mA
1333		55	60		
1066		50	55		
<b>Precharge Quiet Standby Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD2Q	1600	60	65	mA
1333		55	60		
1066		50	55		
<b>Active Power-Down Current;</b> CKE: Low; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3P	1600	50	60	mA
1333		45	55		
1066		40	50		

Conditions	Symbol	Data rate (Mbps)	IDD max. (x8)	IDD max. (x16)	Unit
			95°C <sub>2</sub> )	95°C <sub>2</sub> )	
<b>Active Standby Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: stable at 1; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD3N	1600	65	80	mA
1333		60	70		
1066		55	65		
<b>Operating Burst Read Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: High between RD; Command, Address: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD4R	1600	180	280	mA
1333		140	210		
1066		120	180		
<b>Operating Burst Write Current;</b> CKE: High; External clock: On; tCK, CL: see timing used table; BL: 8; AL: 0; CS#: High between WR; Command, Address: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	IDD4W	1600	200	290	mA
1333		150	220		
1066		130	190		
<b>Burst Refresh Current;</b> CKE: High; External clock: On; tCK, CL, nRFC: see timing used table; BL: 8; AL: 0; CS#: High between REF; Command, Address: partially toggling; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD5B	1600	170	180	mA
1333		160	170		
1066		150	160		
<b>Self Refresh Current: Normal Temperature Range;</b> TCASE: 0- 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normal; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see timing used table; BL: 8; AL: 0; CS#, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: MID-LEVEL	IDD6	1600	4	14	mA
1333					
1066					
<b>Self Refresh Current: Extended Temperature Range;</b> TCASE: 0- 95°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Extended; CKE: Low; External clock: Off; CK and CK#: LOW; CL: see timing used table; BL: 8; AL: 0; CS#, Command, Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: MID-LEVEL	IDD6ET	1600	16	16	mA
1333					
1066					
<b>Operating Bank Interleave Read Current;</b> CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see timing used table; BL: 8; AL: CL-1; CS#: High between ACT and RDA; Command, Address: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	IDD7	1600	260	350	mA
1333		220	300		
1066		180	260		
<b>RESET Low Current;</b> RESET: Low; External clock: off; CK and CK#: LOW; CKE: FLOATING; CS#, Command, Address, Data IO: FLOATING; ODT Signal : FLOATING	IDD8	1600	20	20	mA
1333					
1066					

## 5 Package Outlines

Figure 6 reflects the current status of the outline dimensions of the DDR3 SDRAM packages for 1Gbit components x8 configuration. For functional description of each ball see Chapter 1.4.1.

Figure 6 - Package outline for x8 component



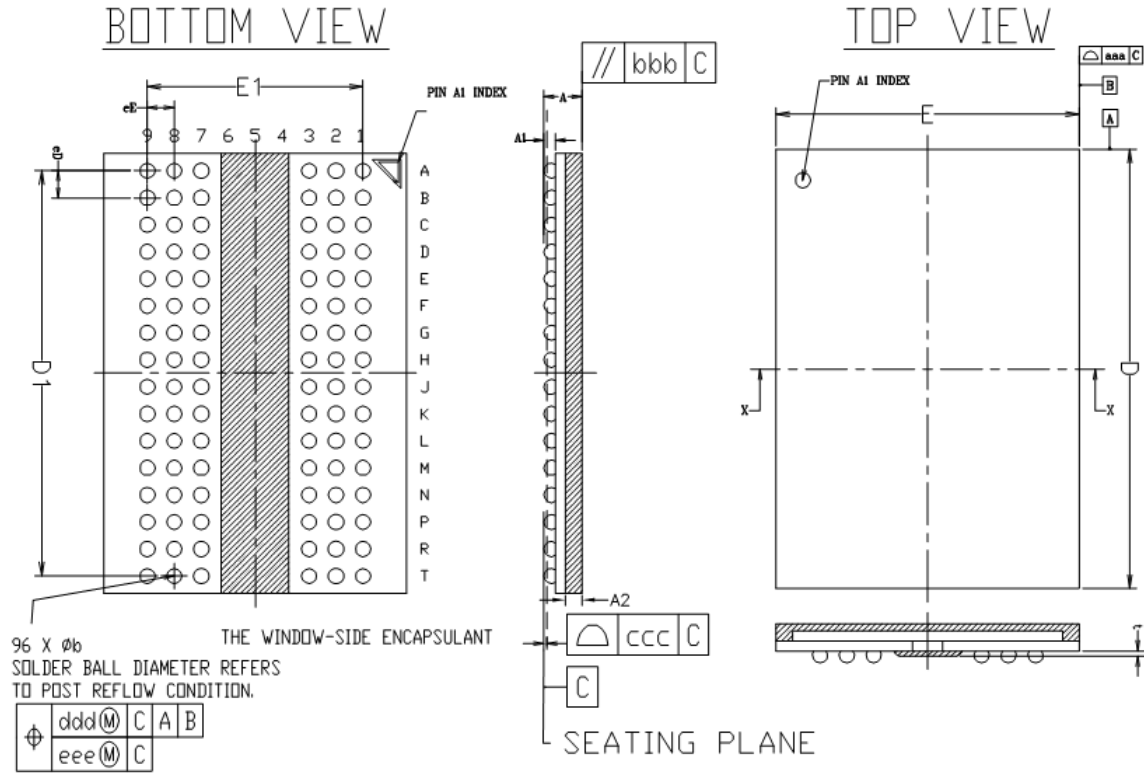
$\phi$	ddd	M	C	A	B
	eee	M	C		

### DIMENSION REFERENCES Units mm

REF.	MIN.	NOM.	MAX.
A	---	1.10	1.20
A1	0,25	0,35	0,40
A2	0,50	0,53	0,56
b	0,40	0,45	0,50
D	10,40	10,50	10,60
E	7,90	8,00	8,10
D1	9,60 BSC		
E1	6,40 BSC		
eE	0,80 BSC		
eD	0,80 BSC		
aaa	---	---	0,15
bbb	---	---	0,20
ccc	---	---	0,10
ddd	---	---	0,15
eee	---	---	0,08
t	---	0,17	0,20

Figure 7 reflects the current status of the outline dimensions of the DDR3 SDRAM packages for 1Gbit components x16 configuration. For functional description of each ball see Chapter 1.4.3.

Figure 7 - Package outline for x16 component



**DIMENSION REFERENCES Units mm**

REF.	MIN.	NOM.	MAX.
A	---	1.10	1.20
A1	0.25	0.35	0.40
A2	0.50	0.53	0.56
b	0.40	0.45	0.50
D	12.90	13.00	13.10
E	8.90	9.00	9.10
D1	12.00 BSC		
E1	6.40 BSC		
eE	0.80 BSC		
eD	0.80 BSC		
aaa	---	---	0.15
bbb	---	---	0.20
ccc	---	---	0.10
ddd	---	---	0.15
eee	---	---	0.08
t	---	0.17	0.20

## 6 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter.

**Table 37 - Examples for Nomenclature Fields**

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
DDR3 SDRAM	SCB	15	H	1G	16	0	A	F	–	13K	I

**Table 38 - DDR3 Memory Nomenclature**

Field	Description	Values	Coding
1	UniIC Component Prefix	SCB	Memory components
2	Interface Voltage [V]	15	SSTL_15, + 1.5 V ( $\pm 0.075$ V)
3	DRAM Technology	H	DDR3
4	Component Density [Mbit]	32	32 Mbit
		64	64 Mbit
		128	128 Mbit
		256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
		4G	4 Gbit
5	Number of I/Os	40	x 4
		80	x 8
		16	x 16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
8	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
9	Power	–	Standard power product
		L	Low power product

Field	Description	Values	Coding
10	Speed Grade	19F	CL-tRCD-tRP = 7-7-7
		19G	CL-tRCD-tRP = 8-8-8
		15G	CL-tRCD-tRP = 8-8-8
		15H	CL-tRCD-tRP = 9-9-9
		13K	CL-tRCD-tRP = 11-11-11
		11M	CL-tRCD-tRP = 13-13-13
11	Temperature range	Blank	Commercial temperature range: 0 °C to 95 °C
		I	Industrial temperature range: -40 °C to 95 °C
		A1	Automotive A1 Temperature range: -40 °C to 125 °C
		A2	Automotive A2 Temperature range: -40 °C to 105 °C
		A3	Automotive A3 Temperature range: -40 °C to 95 °C

# List of Figures

Figure 1 - Ballout for 128 Mb x8 Components (PG-TFBGA-78 Top View) .....	4
Figure 2 - Ballout for 64 Mb x16 Components (PG-TFBGA-96 Top View) .....	7
Figure 3 - Reference Load for AC Timings and Output Slew Rates .....	22
Figure 4 - AC Overshoot / Undershoot Definitions for Address and Control Signals .....	29
Figure 5 - AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals .....	30
Figure 6 - Package outline for x8 component .....	43
Figure 7 - Package outline for x16 component .....	44

# List of Tables

Table 1 - Ordering Information for 1Gbit DDR3 Components .....	2
Table 2 - 1Gbit DDR3 SDRAM Addressing .....	3
Table 3 - Input / Output Signal Functional Description for x8 component .....	5
Table 4 - Input / Output Signal Functional Description for x16 component .....	8
Table 5 - Command Truth Table .....	10
Table 6 - Clock Enable (CKE) Truth Table for Synchronous Transitions .....	12
Table 7 - Data Mask (DM) Truth Table .....	12
Table 8 - MR0 Mode register Definition (BA[2:0]=000B) .....	14
Table 9 - MR1 Mode Register Definition (BA[2:0]=001B) .....	16
Table 10 - MR2 Mode Register Definition (BA[2:0]=010B) .....	18
Table 11 - MR3 Mode Register Definition (BA[2:0]=011B) .....	19
Table 12 - Bit Order during Burst .....	20
Table 13 - Absolute Maximum Ratings .....	21
Table 14 - SDRAM Component Operating Temperature Range .....	21
Table 15 - DC Operating Conditions .....	22
Table 16 - Input and Output Leakage Currents .....	22
Table 17 - DC and AC Input Levels for Single-Ended Command, Address and Control Signals .....	23
Table 18 - DC and AC Input Levels for Single-Ended DQ and DM Signals .....	23
Table 19 - Differential swing requirement for clock (CK - CK#) and strobe (DQS - DQS#) .....	24
Table 20 - Allowed Time Before Ringback (tDVAC) for CK - CK# and DQS - DQS# .....	24
Table 21 - Each Single-Ended Levels for CK, DQS, DQS#, CK# .....	25
Table 22 - Cross Point Voltage for Differential Input Signals (CK, DQS) .....	25
Table 23 - DC and AC Output Levels for Single-Ended Signals .....	26
Table 24 - AC Output Levels for Differential Signals .....	26
Table 25 - Output Slew Rates .....	26
Table 26 - ODT DC Impedance and Mid-Level Characteristics .....	27
Table 27 - ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift .....	27
Table 28 - OTD DC Impedance Sensitivity Parameters .....	27
Table 29 - Interface Capacitance Values .....	28
Table 30 - AC Overshoot / Undershoot Specification for Address and Control Signals .....	29
Table 31 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals .....	30
Table 32 - DDR3-1066 Speed Bins .....	31
Table 33 - DDR3-1333 Speed Bins .....	32
Table 34 - DDR3-1600 Speed Bins .....	33
Table 35 - AC Timing parameters .....	35
Table 36 - IDD Specification .....	41
Table 37 - Examples for Nomenclature Fields .....	45
Table 38 - DDR3 Memory Nomenclature .....	45

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