

Super I/O with Temperature Sensing, Quiet Auto Fan and Glue Logic

PRODUCT FEATURES

Datasheet

- General Features
 - 3.3 Volt Operation (SIO Block is 5 Volt Tolerant)
 - LPC Interface
 - Programmable Wake-up Event Interface
 - PC99, PC2001 Compliant
 - ACPI 2.0 Compliant
 - Multiplexed Command, Address and Data Bus
 - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
 - PME Interface
 - ISA Plug-and-Play Compatible Register Set
 - 25 General Purpose Input/Output Pins
 - System Management Interrupt
- AC Power Failure Recovery
- Watchdog Timer
- 2.88MB Super I/O Floppy Disk Controller
 - Licensed CMOS 765B Floppy Disk Controller
 - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
 - Supports One Floppy Drive
 - Configurable Open Drain/Push-Pull Output Drivers
 - Supports Vertical Recording Format
 - 16-Byte Data FIFO
 - 100% IBM® Compatibility
 - Detects All Overrun and Underrun Conditions
 - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
 - DMA Enable Logic
 - Data Rate and Drive Control Registers
 - 480 Address, Up to Eight IRQ and Three DMA Options
 - Support 3 Mode FDD
- Enhanced Digital Data Separator
 - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
 - Programmable Precompensation Modes
- Serial Ports
 - Two Full Function Serial Ports
 - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
 - Supports 230k and 460k Baud
 - Programmable Baud Rate Generator
 - Modem Control Circuitry
 - 480 Address and 15 IRQ Options
- Infrared Port
 - Multiprotocol Infrared Interface
 - IrDA 1.0 Compliant
 - SHARP ASK IR
 - 480 Addresses, Up to 15 IRQ
- Multi-Mode™ Parallel Port with ChiProtect™
 - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional Parallel Port
 - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
 - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
 - ChiProtect Circuitry for Protection
 - 960 Address, Up to 15 IRQ and Three DMA Options
- Keyboard Controller
 - 8042 Software Compatible
 - 8 Bit Microcomputer
 - 2k Bytes of Program ROM
 - 256 Bytes of Data RAM
 - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
 - Asynchronous Access to Two Data Registers and One Status Register
 - Supports Interrupt and Polling Access
 - 8 Bit Counter Timer
 - Port 92 Support
 - Fast Gate A20 and KRESET Outputs
- Motherboard GLUE Logic
 - IDE Reset Output
 - (4) Buffered PCI Reset Outputs with software controlled reset capability - default transparent
 - 3VSB Gate and 3V Gate signal generation
 - Front Panel Reset Debouncing and Power Good Signal Generation
 - Power Supply Turn On Circuitry with Support for power button on PS/2 Keyboard
 - Resume Reset Signal Generation
 - SMBus Isolation Circuitry (2 sets external and 1 set internal for Hardware Monitoring Block)
 - SMBus 2.0 compliant interface for Hardware Monitoring
 - LED Control (2)

- Fan Control
 - 5 PWM (Pulse width Modulation) Outputs
 - Two and three piece linear fan function options.
 - Low frequency and high frequency PWM support
 - 6 Fan Tachometer Inputs
 - Programmable automatic fan control based on temperature
 - Interrupt Pin for out-of-limit Fantach Events
 - Fantach events generate PME's and/or Speaker warning
- Temperature Monitor
 - Monitoring of Two Remote Thermal Diodes
 - Internal Ambient Temperature Measurement
 - Limit Comparison of all Monitored Values
 - Interrupt Pin for out-of-limit Temperature Indication
 - Thermal events generate PME's and/or Speaker warning
 - Configurable offset for internal or external temperature channels.
- Voltage Monitor
 - Monitor Power supplies (5V, +5VTR, +12V, Vccp, Vbat, VTR, and VCC)
 - Limit Comparison of all Monitored Values
 - Interrupt Pin for out-of-limit Voltage Indication
 - Voltage events generate PME's and/or Speaker warning
- Security Features
 - Security Key Register (32 byte) for Device Authentication
- 6 VID (Voltage Identification) Inputs
- Phoenix Keyboard BIOS ROM
- 128 QFP Green, Lead-Free Package

ORDER NUMBER(S): SCH5017-NW FOR 128 PIN, QFP PACKAGE (GREEN, LEAD-FREE)



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Datasheet

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2. *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
3. *Advanced Configuration and Power Interface Specification, Revision 1.0b*, February 2, 1999
4. IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993.
5. Hardware Description of the 8042, Intel 8 bit Embedded Controller Handbook.
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7. I²C Bus Specification, version 2.0, Philips Semiconductors, Dec. 1998
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Chapter 1 General Description

The SCH5017 is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. SCH5017 also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

The SCH5017's hardware monitoring capability includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans. There are four analog inputs for monitoring external voltages of +5V, +5VTR, +12V and Vccp (core processor voltage), as well as internal monitoring of the SIO's VCC, VTR, and Vbat power supplies. The SCH5017 includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring ambient temperature. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and FANTACH conditions. The hardware monitoring block of the SCH5017 is accessible via the System Management Bus (SMBus). The same interrupt event reported on the nHWM_INT pin also creates PME wakeup events and speaker alarm annunciation.

The SCH5017 also allows for a two or three piece linear fan function. See [Section 26.1.7.4, "Zone Selection"](#) for more detail.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, SMBus buffers, and buffered PCI reset outputs.

The SCH5017 incorporates complete legacy Super I/O functionality including an 8042 based keyboard and mouse controller, an IEEE 1284, EPP, and ECP compatible parallel port, one serial port that is 16C550A UART compatible, one IrDA 1.0 infrared ports, and a floppy disk controller with SMSC's true CMOS 765B core and enhanced digital data separator. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and is software and register compatible with SMSC's proprietary 82077AA core. System related functionality, which offers flexibility to the system designer, General Purpose I/O control functions, control of two LED's, and fan control using fan tachometer inputs and pulse width modulator (PWM) outputs

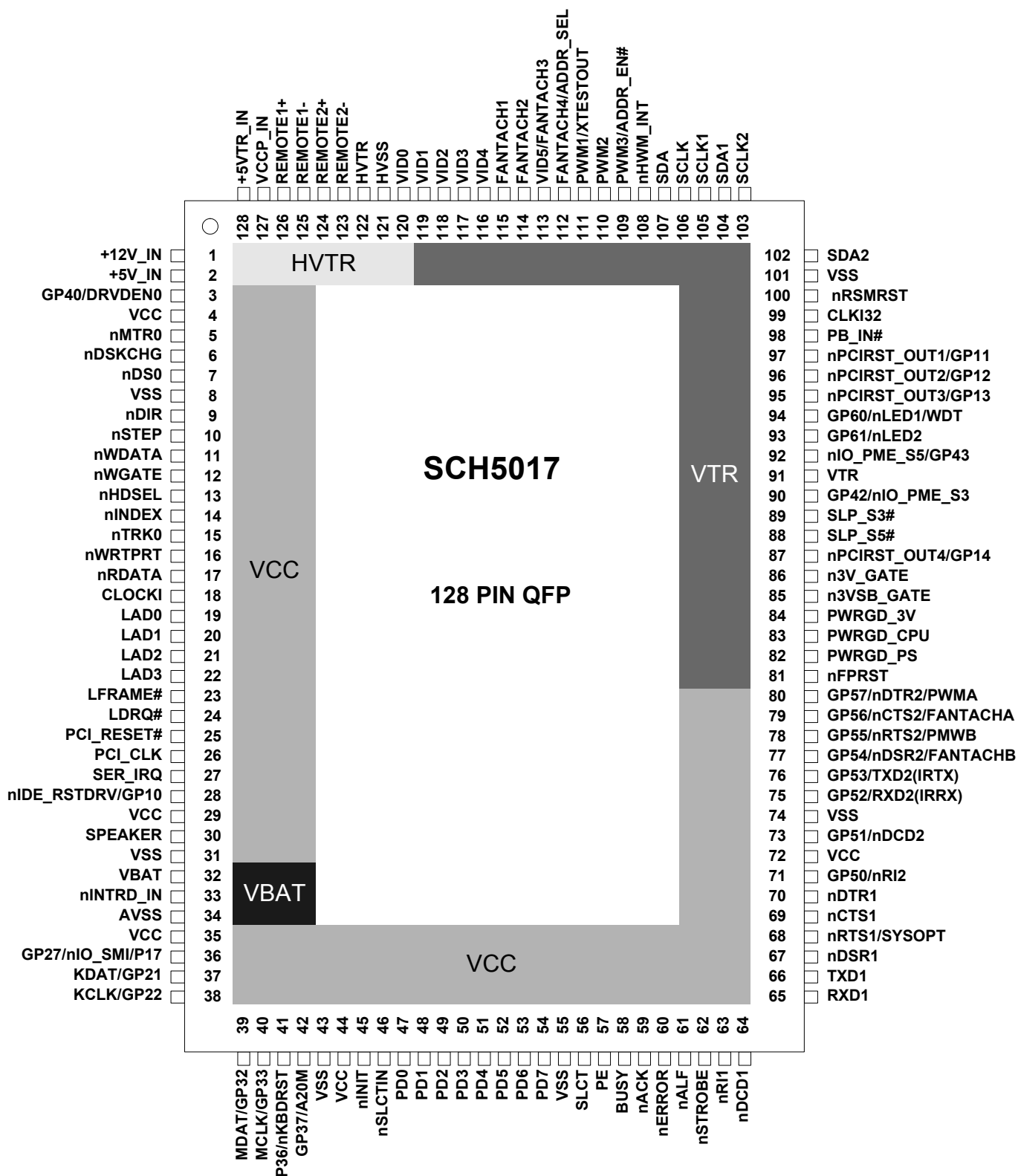
The SCH5017 is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard and mouse wake-up events.

The SCH5017 supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the SCH5017 may be reprogrammed through the internal configuration registers. There are up to 480 (960 - Parallel Port) I/O address location options, a Serialized IRQ interface, and Three DMA channels.



Chapter 2 Pin Layout

2.1 Pin Diagram



2.2 Pin Configuration

Table 2.1 SCH5017 QFP Pin Configuration - PRELIMINARY

PIN #	NAME	PIN #	NAME	PIN #	NAME	PIN #	NAME
1	+12V_IN	33	nINTRD_IN	65	RXD1	97	nPCIRST_OUT1/ GP11
2	+5V_IN	34	AVSS	66	TXD1/ SIO_XNOR_OUT	98	PB_IN#
3	GP40/DRV_DEN0	35	VCC	67	nDSR1	99	CLKI32
4	VCC	36	GP27/nIO_SMI/P17	68	nRTS1/SYSOPT	100	nRSMRST
5	nMTR0	37	KDAT/GP21	69	nCTS1	101	VSS
6	nDSKCHG	38	KCLK/GP22	70	nDTR1	102	SDA2
7	nDS0	39	MDAT/GP32	71	GP50/nRI2	103	SCLK2
8	VSS	40	MCLK/GP33	72	VCC	104	SDA1
9	nDIR	41	GP36/nKBDRST	73	GP51/nDCD2	105	SCLK1
10	nSTEP	42	GP37/A20M	74	VSS	106	SCLK
11	nWDATA	43	VSS	75	GP52/RXD2(IRR_X)	107	SDA
12	nWGATE	44	VCC	76	GP53/TXD2(IRT_X)	108	nHWM_INT
13	nHDSEL	45	nINIT	77	GP54/nDSR2/ FANTACHB	109	PWM3/ADDR_EN #
14	nINDEX	46	nSLCTIN	78	GP55/nRTS2/ PWMB	110	PWM2
15	nTRK0	47	PD0	79	GP56/nCTS2/ FANTACHA	111	PWM1/XTESTOU T
16	nWRTPRT	48	PD1	80	GP57/nDTR2/ PWMA	112	FANTACH4/ ADDR_SEL
17	nRDATA	49	PD2	81	nFPRST	113	VID5/FANTACH3
18	CLOCKI	50	PD3	82	PWRGD_PS	114	FANTACH2
19	LAD0	51	PD4	83	PWRGD_CPU	115	FANTACH1
20	LAD1	52	PD5	84	PWRGD_3V	116	VID4
21	LAD2	53	PD6	85	n3VSB_GATE	117	VID3
22	LAD3	54	PD7	86	n3V_GATE	118	VID2
23	LFRAME#	55	VSS	87	nPCIRST_OUT4/ GP14	119	VID1
24	LDRQ#	56	SLCT	88	SLP_S5#	120	VID0
25	PCI_RESET#	57	PE	89	SLP_S3#	121	HVSS
26	PCI_CLK	58	BUSY	90	GP42/nIO_PME_S 3	122	HVTR
27	SER_IRQ	59	nACK	91	VTR	123	REMOTE2-
28	nIDE_RSTDRV/ GP10	60	nERROR	92	nIO_PME_S5 /GP43	124	REMOTE2+
29	VCC	61	nALF	93	GP61/nLED2	125	REMOTE1-
30	SPEAKER	62	nSTROBE	94	GP60/nLED1/WDT	126	REMOTE1+
31	VSS	63	nRI1	95	nPCIRST_OUT3/ GP13	127	VCCP_IN
32	VBAT	64	nDCD1	96	nPCIRST_OUT2/ GP12	128	+5VTR_IN

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2.3 Pin Functions

Table 2.2 Pin Functions Description

NOTE	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (Note 2.1)
POWER PINS (16)				
2.3, 2.4	VCC	+3.3 Volt Supply Voltage		
2.3, 2.4	VTR	+3.3 Volt Standby Supply Voltage		
2.8	VBAT	+3.0 Volt Battery Supply)		
	VSS	Ground		
	AVSS	Analog Ground		
2.3	HVTR	Analog Power. +3.3V VTR pin dedicated to the Hardware Monitoring block. HVTR is powered by +3.3V Standby power VTR.		
2.3	HVSS	Analog Ground. Internally connected to all of the Hardware Monitoring Block circuitry.		
CLOCK PINS (2)				
	CLKI32	32.768kHz Trickle Clock Input	VTR	IS
	CLOCKI	14.318MHz Clock Input	VCC	IS
LPC INTERFACE (9)				
	LAD[3:0]	Multiplexed Command Address and Data	VCC	PCI_IO
	LFRAME#	Frame signal. Indicates start of new cycle and termination of broken cycle	VCC	PCI_I
	LDRQ#	Encoded DMA Request	VCC	PCI_O
	PCI_RESET#	PCI Reset	VCC	PCI_I
	PCI_CLK	PCI Clock	VCC	PCI_I
	SER_IRQ	Serial IRQ	VCC	PCI_IO
FDD INTERFACE (13)				
	GP40/ DRVDE0	General Purpose I/O /Drive Density Select 0	VCC	(I/O12/OD12)/ (O12/OD12)
	nMTR0	Motor On 0	VCC	(O12/OD12)
	nDSKCHG	Disk Change	VCC	IS
	nDS0	Drive Select 0	VCC	(O12/OD12)
	nDIR	Step Direction	VCC	(O12/OD12)
	nSTEP	Step Pulse	VCC	(O12/OD12)
	nWDATA	Write Disk Data	VCC	(O12/OD12)
	nWGATE	Write Gate	VCC	(O12/OD12)

Table 2.2 Pin Functions Description (continued)

NOTE	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (Note 2.1)
	nHDSEL	Head Select	VCC	(O12/OD12)
	nINDEX	Index Pulse Input	VCC	IS
	nTRK0	Track 0	VCC	IS
	nWRTPRT	Write Protected	VCC	IS
	nRDATA	Read Disk Data	VCC	IS
SERIAL PORT 1 INTERFACE (8)				
	RXD1	Receive Data 1	VCC	IS
	TXD1 /SIO XNOR_OUT	Transmit Data 1 / XNOR-Chain test mode Output for SIO block	VCC	O12/O12
	nDSR1	Data Set Ready 1	VCC	I
2.7	nRTS1/ SYSOPT	Request to Send 1/ SYSOPT (Configuration Port Base Address Control)	VCC	OP14/I
	nCTS1	Clear to Send 1	VCC	I
	nDTR1	Data Terminal Ready 1	VCC	O6
2.9	nRI1	Ring Indicator 1	VCC	IS
	nDCD1	Data Carrier Detect 1	VCC	I
SERIAL PORT 2 INTERFACE (8)				
2.9	GP50/nRI2	General Purpose I/O /Ring Indicator 2	VCC	(I/O8/OD8)/I
2.9	GP51 /nDCD2	General Purpose I/O /Data Carrier Detect 2	VCC	(I/O8/OD8)/I
2.9	GP52 /RXD2 (IRRX)	General Purpose I/O /Receive Data 2 (IRRX)	VCC	(IS/O8/OD8)/IS
2.11, 2.9	GP53 /TXD2 (IRTX)	General Purpose I/O /Transmit Data 2 (IRTX)	VCC	(I/O12/OD12) /O12
2.9	GP54 /nDSR2 /FANTACHB	General Purpose I/O /Data Set Ready 2 /Tachometer Input 6 for monitoring a fan.	VCC	(I/O8/OD8)/I/I
2.9	GP55 /nRTS2 /PWMB	General Purpose I/O /Request to Send 2 / PWM Output 5 controlling speed of fan.	VCC	(I/O8/OD8)/I /OD8
2.9	GP56 /nCTS2 /FANTACHA	General Purpose I/O /Clear to Send 2 /Tachometer Input 5 for monitoring a fan.	VCC	(I/O8/OD8)/I/I
2.9	GP57 /nDTR2 /PWMA	General Purpose I/O /Data Terminal Ready 2 /PWM Output 4 controlling speed of fan.	VCC	(I/O8/OD8)/I /OD8
PARALLEL PORT INTERFACE (17)				

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Table 2.2 Pin Functions Description (continued)

NOTE	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (Note 2.1)
	nINIT	Initiate Output	VCC	(OD14/OP14)
	nSLCTIN	Printer Select Input	VCC	(OD14/OP14)
	PD0	Port Data 0	VCC	IOP14
	PD1	Port Data 1	VCC	IOP14
	PD2	Port Data 2	VCC	IOP14
	PD3	Port Data 3	VCC	IOP14
	PD4	Port Data 4	VCC	IOP14
	PD5	Port Data 5	VCC	IOP14
	PD6	Port Data 6	VCC	IOP14
	PD7	Port Data 7	VCC	IOP14
	SLCT	Printer Selected Status	VCC	I
	PE	Paper End	VCC	I
	BUSY	Busy	VCC	I
	nACK	Acknowledge	VCC	I
	nERROR	Error	VCC	I
	nALF	Autofeed Output	VCC	(OD14/OP14)
	nSTROBE	Strobe Output	VCC	(OD14/OP14)
KEYBOARD/MOUSE INTERFACE (6)				
2.9	KDAT/GP21	Keyboard Data I/O General Purpose I/O	VCC	(I/OD16)/ (I/O16/OD16)
	KCLK/GP22	Keyboard Clock I/O General Purpose I/O	VCC	I/OD16/ (I/O16/OD16)
2.9	MDAT/GP32	Mouse Data I/O /General Purpose I/O	VCC	(I/OD16) /(I/O16/OD16)
2.9	MCLK/GP33	Mouse Clock I/O /General Purpose I/O	VCC	(I/O16/OD16) /(I/OD16)
2.6	GP36/ nKBDRST	General Purpose I/O. GPIO can be configured as an Open-Drain Output. Keyboard Reset Open-Drain Output (Note 2.6)	VCC	(I/O8/OD8) /OD8
2.6	GP37/ A20M	General Purpose I/O. GPIO can be configured as an Open-Drain Output. Gate A20 Open-Drain Output (Note 2.6)	VCC	(I/O8/OD8) /OD8
MISCELLANEOUS PINS (5)				
	GP42/ nIO_PME_ S3	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in S3 and below.	VTR	(I/O12/OD12) /(O12/OD12)

Table 2.2 Pin Functions Description (continued)

NOTE	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (Note 2.1)
	nIO_PME_S5/ GP43	Power Management Event Output. This active low Power Management Event signal allows this device to request wake-up in S4 or S5. General Purpose I/O.	VTR	(O12/OD12)/ (I/O12/OD12)
2.8, 2.9	GP60 /nLED1 /WDT	General Purpose I/O /nLED1 Watchdog Timer Output	VTR	(I/O12/OD12) /(O12/OD12) /(O12/OD12)
2.8, 2.9	GP61 /nLED2	General Purpose I/O /nLED2	VTR	(I/O12/OD12) /(O12/OD12)
2.9	GP27 /nIO_SMI /P17	General Purpose I/O /System Mgt. Interrupt /8042 P17 I/O	VCC	(I/O12/OD12) /(O12/OD12) /(I/O12/OD12)
INTRUDER DETECTION (1)				
2.9	nINTRD_IN	Intruder Input. Latches the state of a chassis cover removal switch. A high-to-low or low-to-high will set the INTRUSION bit to indicate an intrusion event. Note: the INTRUSION bit is also set to '1' on VBAT POR.	Vbat	IL
GLUE LOGIC (16)				
	PB_IN#	Power Button In is used to detect a power button event	VTR	I
	SLP_S3#	S3 Sleep State Input Pin.	VTR	I
	SLP_S5#	S5 Sleep State Input Pin.	VTR	I
	nFPRST	Front Panel Reset	VTR	ISPU_400
	PWRGD_PS	Power Good Input from Power Supply	VTR	ISPU_400
	PWRGD_CPU	Power Good Output – Open Drain	VTR	OD8
	PWRGD_3V	Power Good Output – Push Pull	VTR	O8
	n3VSB_GATE	PS Control	VTR	O8
	n3V_GATE	PS Control	VTR	O8
	nPCIRST_OUT1 /GP11	Buffered PCI Reset Output 1 /General Purpose Output.	VTR	OP14
	nPCIRST_OUT2 /GP12	Buffered PCI Reset Output 2 /General Purpose Output.	VTR	OP14
	nPCIRST_OUT3 /GP13	Buffered PCI Reset Output 3 /General Purpose Output.	VTR	OP14
	nPCIRST_OUT4 /GP14	Buffered PCI Reset Output 4 /General Purpose Output.	VTR	OD14
	nIDE_RSTDRV/ GP10	General Purpose Output IDE Reset Output	VCC	OD8
	SPEAKER	Speaker Output. Provides audio warning of HW Monitor or Intruder events and may be enabled by software.	VCC	OD4

Table 2.2 Pin Functions Description (continued)

NOTE	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (Note 2.1)
	nRSMRST	Resume Reset Output	VTR	O8
HARDWARE MONITORING BLOCK (23)				
	SDA	System Management Bus bi-directional Data. Open Drain output.	VTR	IOD8
	SCLK	System Management Bus Clock.	VTR	I
	nHWM_INT	Interrupt output for Hardware monitor	VTR	OD8
	VID0	Voltage ID 0 Input	HVTR	I_VID
	VID1	Voltage ID 1 Input	VTR	I_VID
	VID2	Voltage ID 2 Input	VTR	I_VID
	VID3	Voltage ID 3 Input	VTR	I_VID
	VID4	Voltage ID 4 Input	VTR	I_VID
	VID5/ FANTACH3	Voltage ID 5 Input. Tachometer Input 3 for monitoring a fan.	VTR	I_VID
2.10	+5V_IN	Analog input for +5V	HVTR	I _{AN}
2.10	+5VTR_IN	Analog input for +5V VTR	HVTR	I _{AN}
2.10	VCCP_IN	Analog input for +Vccp (processor voltage: 0 to 3.0V).	HVTR	I _{AN}
2.10	+12V_IN	Analog input for +12V	HVTR	I _{AN}
	REMOTE1-	This is the negative Analog input (current sink) from the remote thermal diode 1.	HVTR	I _{AND-}
	REMOTE1+	This is the positive input (current source) from the remote thermal diode 1.	HVTR	I _{AND+}
	REMOTE2-	This is the negative Analog input (current sink) from the remote thermal diode 2.	HVTR	I _{AND-}
	REMOTE2+	This is the positive input (current source) from the remote thermal diode 2.	HVTR	I _{AND+}
	PWM1/ XTESTOUT	Fan Speed Control 1 Output. HW Monitor XOR test tree output	VTR	OD8/O8
	PWM2	Fan Speed Control 2 Output	VTR	OD8
	PWM3/ ADDR_EN#	PWM Output 3 controlling speed of fan. If pulled to ground at power on, enables Address Select Mode (Address Select pin controls SMBus address of the device).	VTR	IOD8/I
	FANTACH1	Tachometer Input 1 for monitoring a fan.	VTR	I _M
	FANTACH2	Tachometer Input 2 for monitoring a fan.	VTR	I _M
	FANTACH4/ ADDR_SEL	Tachometer Input 4 for monitoring a fan. SMBus Address Select Control.	VTR	I _M

Table 2.2 Pin Functions Description (continued)

NOTE	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES (Note 2.1)
SMBUS POWER STATE ISOLATION (4)				
	SDA1	POWER STATE ISOLATION SMBus 1: System Management Bus bi-directional Data. Open Drain output.	VTR	nSW
	SCLK1	POWER STATE ISOLATION SMBus 1: System Management Bus Clock.	VTR	nSW
	SDA2	POWER STATE ISOLATION SMBus 2: System Management Bus bi-directional Data. Open Drain output.	VTR	nSW
	SCLK2	POWER STATE ISOLATION SMBus 2: System Management Bus Clock.	VTR	nSW

Note: The “n” as the first letter of a signal name or the “#” as the suffix of a signal name indicates an “Active Low” signal.

Note 2.1 Buffer types per function on multiplexed pins are separated by a slash “/”. Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 2.2 Pins that have input buffers must always be held to either a logical low or a logical high state when powered. Bi-directional buses that may be trisected should have either weak external pull-ups or pull-downs to hold the pins in a logic state (i.e., logic states are VCC or ground).

Note 2.3 VCC and VSS pins are for Super I/O Blocks. HVTR and HVSS are dedicated for the Hardware Monitoring Block.

Note 2.4 VTR can be connected to VCC if no wake-up functionality is required.

Note 2.5 The Over Current Sense Pin requires an external pull-up (30ua pull-up is suggested).

Note 2.6 External pull-ups must be placed on the nKBDRST and A20M pins. These pins are GPIOs that are inputs after an initial power-up (VTR POR). If the nKBDRST and A20M functions are to be used, the system must ensure that these pins are high.

Note 2.7 The nRTS1/SYSOPT pin requires an external pull-down resistor to put the base I/O address for configuration at 0x02E. An external pull-up resistor is required to move the base I/O address for configuration to 0x04E.

Note 2.8 The LED pins are powered by VTR so that the LEDs can be controlled when the part is under VTR power.

Note 2.9 This pin is an input into the wake-up logic that is powered by VTR.

Note 2.10 This analog input is backdrive protected. Although HVTR is powered by VTR, it is possible that monitored power supplies may be powered when HVTR is off.

Note 2.11 The GP53/TXD2(IRTX) pin defaults to the GPIO input function on a VTR POR and presents a tristate impedance. When VCC=0 the pin is tristate. If GP53 function is selected and VCC is power is applied, the pin reflects the current state of GP53. The GP53/TXD2(IRTX) pin is tristate when it is configured for the TXD2 (IRTX) function under various conditions detailed in [Section 8.1.1, "IR Transmit Pin," on page 100](#).

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2.4 Buffer Description

Table 2.3 lists the buffers that are used in this device. A complete description of these buffers can be found in [Section 31.2, "DC Electrical Characteristics," on page 321](#).

Table 2.3 Buffer Description

BUFFER	DESCRIPTION
I	Input TTL Compatible - Super I/O Block.
IL	Input, Low Leakage Current.
I _M	Input - Hardware Monitoring Block.
I _{AN}	Analog Input, Hardware Monitoring Block.
I _{ANP}	Back Bias Protected Analog Input, Hardware Monitoring Block.
I _{AND-}	Remote Thermal Diode (current sink) Negative Input
I _{AND+}	Remote Thermal Diode (current source) Positive Input
IS	Input with Schmitt Trigger.
I _{_VID}	Input. See Section 31.2, "DC Electrical Characteristics" .
I _M OD3	Input/Output (Open Drain), 3mA sink.
I _M O3	Input/Output, 3mA sink, 3mA source.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
IOD8	Input/Open Drain Output, 8mA sink, 4mA source.
IS/O8	Input with Schmitt Trigger/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
OD4	Open Drain Output, 4mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
IOD12	Input/Open Drain Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
IO16	Input/Output 16mA sink.
IOD16	Input/Output (Open Drain), 16mA sink.

Table 2.3 Buffer Description

BUFFER	DESCRIPTION
PCI_IO	Input/Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 2.12)
PCI_O	Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 2.12)
PCI_I	Input. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 2.12)
PCI_ICLK	Clock Input. These pins must meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2.13)
nSW	n Channel Switch ($R_{on} \sim 25$ Ohms)
ISPU_400	Input with 400mV Schmitt Trigger and 30uA Integrated Pull-Up.
ISPU	Input with Schmitt Trigger and Integrated Pull-Up.

Note 2.12 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2.

Note 2.13 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2 and 4.2.3.

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Chapter 3 Block Diagram

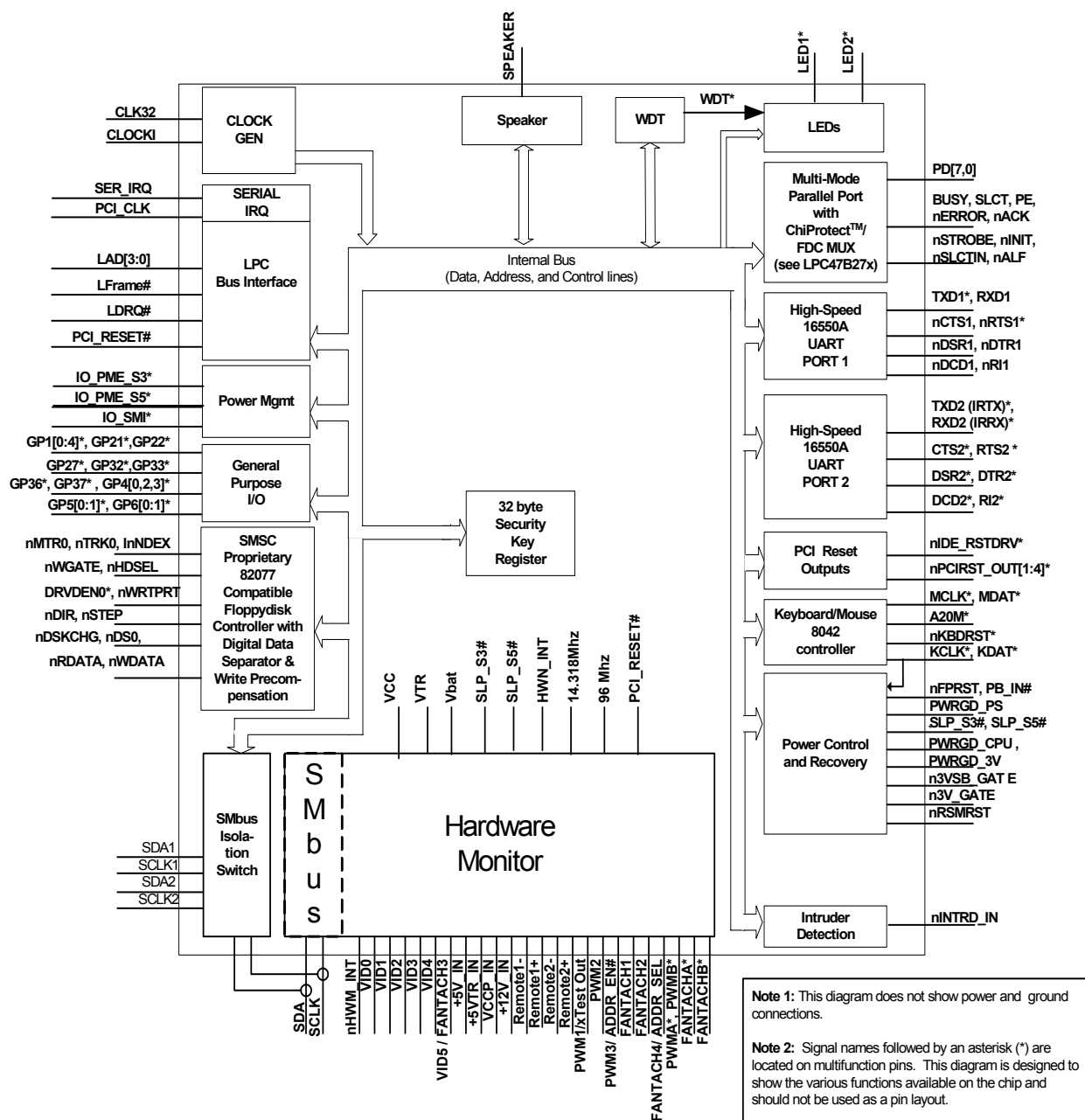


Figure 3.1 SCH5017 Block Diagram



Chapter 4 Power Functionality

The SCH5017 has five power planes: VCC, HVTR, VREF, VTR, and Vbat.

4.1 VCC Power

The SCH5017 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). VCC is the main power supply for the Super I/O Block. See [Section 31.2, "DC Electrical Characteristics," on page 321](#).

4.2 HVTR Power

The SCH5017 is a 3.3 Volt part. The HVTR supply is 3.3 Volts (nominal). HVTR is a dedicated power supply for the Hardware Monitoring Block. HVTR is connected to the VTR suspend well. See [Section 31.2, "DC Electrical Characteristics," on page 321](#).

Note: The hardware monitoring logic is powered by HVTR, but only operational when VCC is on. The hardware monitoring block is connected to the suspend well to retain the programmed configuration through a sleep cycle.

4.3 3 Volt Operation / 5 Volt Tolerance

The SCH5017 is a 3.3-Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the operating input voltage is 5.5V Max, and the I/O buffer output pads are backdrive protected (they do not impose a load on any external VCC powered circuitry).

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- LFRAME#
- LDRQ#

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins in the Super I/O Block:

- PCI_RESET#
- PCI_CLK
- SER_IRQ
- nIO_PME_S3
- nIO_PME_S5

4.4 VTR Support

The SCH5017 requires a trickle supply (VTR) to provide sleep current for the programmable wake-up events in the PME interface when VCC is removed. The VTR supply is 3.3 Volts (nominal). See [Chapter 31, "Operational Description," on page 321](#). The maximum VTR current that is required depends on the functions that are used in the part. See [Chapter 31, "Operational Description," on page 321](#).

If the SCH5017 is not intended to provide wake-up capabilities on standby current, VTR can be connected to VCC. VTR powers the IR interface, the PME configuration registers, and the PME interface. The VTR pin generates a VTR Power-on-Reset signal to initialize these components. If VTR is to be used for programmable wake-up events when VCC is removed, VTR must be at its full

minimum potential at least 10 ms before Vcc begins a power-on cycle. Note that under all circumstances, the hardware monitoring HVTR must be driven as the same source as VTR.

4.4.1 Trickle Power Functionality

When the SCH5017 is running under VTR only (VCC removed), PME wakeup events are active and (if enabled) able to assert the nIO_PME_S3 and nIO_PME_S5 pins active low. (See [Table 15.2, "PME Events," on page 147.](#))

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means, at a minimum, they will source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup as input are GP21-GP22, GP27, GP32, GP33, GP50-GP57, GP60, GP61 (See [Table 13.1, "GPIO Functionality," on page 137.](#)) These GPIOs function as follows (with the exception of GP60 and GP61 - see below):

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are PME wakeup as a GPIO (or alternate function).

GP32 and GP33 revert to their non-inverting GPIO input function when VCC is removed from the part.

The other GPIOs function as follows:

GP36, GP37 and GP40:

- Buffers are powered by VCC. In the absence of VCC they are backdrive protected. These pins do not have input buffers into the wakeup logic that are powered by VTR, and are not used for wakeup.

GP42, GP43, GP60 and GP61:

- Buffers powered by VTR. GP42 and GP43 are the nIO_PME_S3 and nIO_PME_S5 pins which is active under VTR. GP60 and GP61 have LED as the alternate function and the logic is able to control the pin under VTR.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- PME runtime register block (includes all PME, SMI, GPIO, Fan and other miscellaneous registers)
- Digital logic in the Hardware Monitoring block
- "Wake on Specific Key" logic
- LED control logic
- Watchdog Timer
- Power Recovery Logic
- Intruder Detection Logic
- Pins for PME Wakeup:
 - GP42/nIO_PME_S3 (output, buffer powered by VTR)
 - GP43/nIO_PME_S5 (output, buffer powered by VTR)
 - CLOCKI32 (input, buffer powered by VTR)
 - nRI1 (input)
 - GP50/nRI2 (input)

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GP52/RXD2(IRR)X (input)
 KDAT/GP21 (input)
 MDAT/GP32 (input)
 nINTRD_IN (input)
 GPIOs (GP21-GP22, GP27, GP32, GP33, GP50-GP57, GP60, GP61) – all input-only except GP60, GP61. See below.

- Other Pins
 - GP60/LED1 (output, buffer powered by VTR)
 - GP61/LED2 (output, buffer powered by VTR)
 - nRSMRST
 - PWRGD_PS
 - nFPRST
 - SLP_S3#
 - SLP_S3#
 - SLP_S5#
 - PWRGD_CPU
 - PWRGD_3V
 - n3V_GATE
 - n3VSB_GATE

4.5 Vbat Support

Vbat is a battery generated power supply that is needed to support the power recovery logic. The power recovery logic is used to restore power to the system in the event of a power failure. Power may be returned to the system by a keyboard power button, the main power button, or by the power recovery logic following an unexpected power failure.

The Vbat supply is 3.0 Volts (nominal). See [Chapter 31, "Operational Description," on page 321](#).

The following pin is powered by Vbat:

- nINTRD_IN

The following Runtime Registers are powered by Vbat:

- Bank 2 of the Runtime Register block used for the 32kbyte Security Key register
- PME_S5_EN at offset 03h
- PMES5_EN1, PMES5_EN3, PMES5_EN5, PMES5_EN6 at offset 10h-13h
- PWR_REC Register at offset 49h
- SLP_S3_Shift Register at offset 4Ah
- INTRD Register at offset 52h
- SLP_S3_Pre_State at offset 53h
- Keyboard Scan Code – Make Byte 1 at offset 5Fh
- Keyboard Scan Code – Make Byte 2 at offset 60h
- Keyboard Scan Code – Break Byte 1 at offset 61h
- Keyboard Scan Code – Break Byte 2 at offset 62h
- Keyboard Scan Code – Break Byte 3 at offset 63h
- Keyboard PWRBTN/SPEKEY at offset 64h
- SMB_ISO Register at offset 6Ah

Note: All Vbat powered pins and registers are powered by VTR when VTR power is on and are battery backed-up when VTR is removed.

4.6 32.768 KHz Trickle Clock Input

The SCH5017 utilizes a 32.768 KHz trickle input to supply a clock signal for the WDT, LED blink, Power Recovery Logic, and wake on specific key function.

Indication of 32KHZ Clock

There is a bit to indicate whether or not the 32KHz clock input is connected to the SCH5017. This bit is located at bit 0 of the CLKI32 register at 0xF0 in Logical Device A. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32KHz clock is connected to the CLKI32 pin (default)

1=32KHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32KHz (nominal) clock for the LED blink logic and the “wake on specific key” logic. When the external 32KHz clock is connected, that will be the source for the fan, LED and “wake on specific key” logic. When the external 32KHz clock is not connected, an internal 32KHz clock source will be derived from the 14MHz clock for the LED and “wake on specific key” logic.

The following functions will not work under VTR power (VCC removed) if the external 32KHz clock is not connected. These functions will work under VCC power even if the external 32 KHz clock is not connected.

- Wake on specific key
- LED blink
- Power Recovery Logic
- WDT
- Front Panel Reset with Input Debounce, Power Supply Gate, and CPU Powergood Signal Generation

4.7 Super I/O Functions

The maximum VTR current, I_{TR} , is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The super I/O pins that are powered by VTR are as follows: GP42/nIO_PME_S3, GP43/nIO_PME_S5, GP60/LED1, GP61/LED2, PWRGD_CPU, PWRGD_3V, n3V_GATE, n3VSB_GATE, and CLKI32. These pins, if configured as push-pull outputs, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC} , is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

The maximum Vbat current, I_{bat} , is given with all outputs open (not loaded) and all inputs in a fixed state (i.e., 0V or 3.3V).

4.8 Power Management Events (PME/SCI)

The SCH5017 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME_S3 and nIO_PME_S5 output signal. See [Chapter 15, "PME Support," on page 147](#) section.

Chapter 5 SIO Overview

The SCH5017 is a Super I/O Device with hardware monitoring. The Super I/O features are implemented as logical devices accessible through the LPC interface. The Super I/O blocks are powered by VCC, VTR, or Vbat. The Hardware Monitoring block is powered by VTR and is accessible via the SMBus interface. The following chapters define each of the functional blocks implemented in the SCH5017, their corresponding registers, and physical characteristics.

This chapter offers an introduction into the Super I/O functional blocks, registers and host interface. Details regarding the hardware monitoring block and SMBus interface are defined in later chapters. The block diagram in [Chapter 3](#) further details the layout of the device. Note that the Super I/O registers are implemented as typical Plug-and-Play components.

Note: There are two main interfaces used to access the components of this chip. The LPC interface is used to access the Super I/O registers and the SMBus is used to access the Hardware Monitoring registers.

5.1 Super I/O Registers

The address map, shown below in [Table 5.1](#) shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of all the Super I/O Logical Blocks, including the configuration register block, can be moved or relocated via the configuration registers.

Note: Some addresses are used to access more than one register.

5.2 Host Processor Interface (LPC)

The host processor communicates with the Super I/O features in the SCH5017 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in [Table 5.1](#), "Super I/O Block Addresses". Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Table 5.1 Super I/O Block Addresses

ADDRESS	BLOCK NAME	LOGICAL DEVICE	NOTES
Base+(0-5) and +(7)	Floppy Disk	0	
na	Reserved	1	(Note 5.3)
na	Reserved	2	(Note 5.3)
Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	3	
Base+(0-7)	Serial Port Com 1	4	
Base+(0-7)	Serial Port Com 2	5	
na	Reserved	6	
60, 64	KYBD	7	
na	Reserved	8,9	

Table 5.1 Super I/O Block Addresses (continued)

ADDRESS	BLOCK NAME	LOGICAL DEVICE	NOTES
Base1 + (0-7F) Base2 + (0-1F)	Runtime Registers Security Key Registers	A	(Note 5.2)
na	Reserved	B	(Note 5.3)
Base + (0-1)	Configuration		(Note 5.1)

Note 5.1 Refer to the configuration register descriptions for setting the base address.

Note 5.2 Logical Device A is referred to as the Runtime Register block at Base1 or PME Block and may be used interchangeably throughout this document.

Note 5.3 na = not applicable

Chapter 6 LPC Interface

6.1 LPC Interface Signal Definition

The signals implemented for the LPC bus interface are described in the tables below. LPC bus signals use PCI 33MHz electrical signal characteristics.

6.1.1 LPC Required Signals

SIGNAL NAME	TYPE	DESCRIPTION
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset. Same functionality as RST_DRV but active low 3.3V.
PCI_CLK	Input	PCI Clock.

6.1.2 LPC Optional Signals

SIGNAL NAME	TYPE	DESCRIPTION	COMMENT
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.	Implemented
SER_IRQ	I/O	Serial IRQ.	Implemented
CLKRUN#	OD	Clock Run	Not Implemented
nIO_PME_S3	OD	Same as the PME# or Power Mgt Event signal. Allows the SCH5017 to request wakeup in S3 and below.	Implemented
nIO_PME_S5	OD	Same as the PME# or Power Mgt Event signal. Allows the SCH5017 to request wakeup in S4 or S5.	Implemented
LPCPD#	I	Power down - Indicates that the device should prepare for LPC I/F shutdown	Not Implemented
LSMI#	OD	Only need for SMI# generation on I/O instruction for retry.	Not Implemented

6.2 Supported LPC Cycles

Table 6.1 summarizes the cycle types are supported by the SCH5017. All other cycle types are ignored.

Table 6.1 Supported LPC Cycles

CYCLE TYPE	TRANSFER SIZE	COMMENT
I/O Write	1 Byte	Supported
I/O Read	1 Byte	Supported
Memory Write	1 Byte	Not Supported

Table 6.1 Supported LPC Cycles (continued)

CYCLE TYPE	TRANSFER SIZE	COMMENT
Memory Read	1 Byte	Not Supported
DMA Write	1 Byte	Supported
DMA Write	2 Byte	Supported
DMA Write	4 Byte	Not Supported
DMA Read	1 Byte	Supported
DMA Read	2 Byte	Supported
DMA Read	4 Byte	Not Supported
Bus Master Memory Write	1 Byte	Not Supported
Bus Master Memory Write	2 Byte	Not Supported
Bus Master Memory Write	4 Byte	Not Supported
Bus Master Memory Read	1 Byte	Not Supported
Bus Master Memory Read	2 Byte	Not Supported
Bus Master Memory Read	4 Byte	Not Supported
Bus Master I/O Write	1 Byte	Not Supported
Bus Master I/O Write	2 Byte	Not Supported
Bus Master I/O Write	4 Byte	Not Supported
Bus Master I/O Read	1 Byte	Not Supported
Bus Master I/O Read	2 Byte	Not Supported
Bus Master I/O Read	4 Byte	Not Supported

6.3 Device Specific Information

The LPC interface conforms to the “*Low Pin Count (LPC) Interface Specification*”. The following section will review any implementation specific information for this device.

6.3.1 SYNC Protocol

The SYNC pattern is used to add wait states. For read cycles, the SCH5017 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SCH5017 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SCH5017 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value. The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The SCH5017 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the SCH5017 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

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6.3.2 Reset Policy

The following rules govern the reset policy:

- When PCI_RESET# goes inactive (high), the PCI clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
- When PCI_RESET# goes active (low):
 1. The host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
 2. The SCH5017 ignores LFRAME#, tristates the LAD[3:0] pins and drives the LDRQ# signal inactive (high).



Chapter 7 Floppy Disk Controller

The Floppy Disk controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection. SCH5017 supports a single floppy disk drive.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

7.1 FDC Internal Registers

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 7.1 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

(Shown with base addresses of 3F0 and 370)

Table 7.1 Status, Data and Control Registers

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TDR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

7.1.1 Status Register A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 – D7 are held in a high impedance state for a read of address 3F0.

PS/2 MODE

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

Bit 0 DIRECTION

Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

Bit 1 nWRITE PROTECT

Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

Bit 2 nINDEX

Active low status of the INDEX disk interface input.

Bit 3 HEAD SELECT

Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

Bit 4 nTRACK 0

Active low status of the TRK0 disk interface input.

Bit 5 STEP

Active high status of the STEP output disk interface output pin.

Bit 6 nDRV2

This function is not supported. This bit is always read as "1".

Bit 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt output.

7.1.2 PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

Bit 0 DIRECTION

Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

Bit 1 WRITE PROTECT

Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

Bit 2 INDEX

Active high status of the INDEX disk interface input.

Bit 3 HEAD SELECT

Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

Datasheet**Bit 4 TRACK 0**

Active high status of the TRK0 disk interface input.

Bit 5 STEP

Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

Bit 6 DMA REQUEST

Active high status of the DMA request pending.

Bit 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt.

STATUS REGISTER B (SRB)**Address 3F1 READ ONLY**

This register is read-only and monitors the state of several disk interface pins in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 – D7 are held in a high impedance state for a read of address 3F1.

PS/2 MODE

	7	6	5	4	3	2	1	0
	Reserved	Reserved	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	Reserved	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

Bit 0 MOTOR ENABLE 0

Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

Bit 1 Reserved

Reserved will return a zero (0) when read. This bit is low after a hardware reset and unaffected by a software reset.

Bit 2 WRITE GATE

Active high status of the WGATE disk interface output.

Bit 3 READ DATA TOGGLE

Every inactive edge of the RDATA input causes this bit to change state.

Bit 4 WRITE DATA TOGGLE

Every inactive edge of the WDATA input causes this bit to change state.

Bit 5 DRIVE SELECT 0

Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

Bit 6 RESERVED

Always read as a logic "1".

Bit 7 RESERVED

Always read as a logic "1".

PS/2 MODEL 30 MODE

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

Bit 0 nDRIVE SELECT 2

The DS2 disk interface is not supported.

Bit 1 nDRIVE SELECT 3

The DS3 disk interface is not supported.

Bit 2 WRITE GATE

Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

Bit 3 READ DATA

Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

Bit 4 WRITE DATA

Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

Bit 5 nDRIVE SELECT 0

Active low status of the DS0 disk interface output.

Bit 6 nDRIVE SELECT 1

The DS 1 disk interface is not supported.

Bit 7 nDRV2

Active low status of the DRV2 disk interface input. Note: This function is not supported.

DIGITAL OUTPUT REGISTER (DOR)
Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

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	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

Bit 0 and 1 DRIVE SELECT

These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time. For proper device operation, they must be programmed to 0b00.

Bit 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

Bit 3 DMAEN

PC/AT and Model 30 Mode:

Writing this bit to logic "1" will enable the DMA and interrupt functions. This bit being a logic "0" will disable the DMA and interrupt functions. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic "0".

Bit 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

Bit 5 MOTOR ENABLE 1

The MTR1 disk interface output is not support in the LPC5M262. For proper device operation this bit must be programmed with a zero (0).

DRIVE	DOR VALUE
0	1CH

Table 7.2 Internal 2 Drive Decode – Normal

DIGITAL OUTPUT REGISTER			DRIVE SELECT OUTPUTS (ACTIVE LOW)	MOTOR ON OUTPUTS (ACTIVE LOW)
Bit 4	Bit1	Bit 0	nDS0	nMTR0
1	0	0	0	nBIT 4
X	1	0	1	nBIT 4
X	X	1	1	nBIT 4

Bit 6 MOTOR ENABLE 2

The MTR2 disk interface output is not supported in the SCH5017.

Bit 7 MOTOR ENABLE 3

The MTR3 disk interface output is not supported in the SCH5017.

TAPE DRIVE REGISTER (TDR)
Address 3F3 READ/WRITE

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 7.3 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

Table 7.3 Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1 (not supported)
1	0	2 (not supported)
1	1	3 (not supported)

APPLICATION NOTE: Note that in this device since only drive 0 is supported, the tape sel0/1 bits must be set to 0b00 for proper operation.

NORMAL FLOPPY MODE

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 – 7 are '0'

Note only drive 0 is supported.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	0	0	0	0	0	0	tape sel1	tape sel0

ENHANCED FLOPPY MODE 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

Note only drive 0 is supported

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

Table 7.4 Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 – DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 – B1	L0-CRF2 – B0
0	1	L0-CRF2 – B3	L0-CRF2 – B2
1	0	L0-CRF2 – B5	L0-CRF2 – B4
1	1	L0-CRF2 – B7	L0-CRF2 – B6

Note: L0-CRF2-Bx = Logical Device 0, Configuration Register F2, Bit x.

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE- COMP2	PRE- COMP1	PRE- COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30.

Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

Bit 0 and 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See [Table 7.6](#) for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Bit 2 through 4 PRECOMPENSATION SELECT

These three bits select the value of write precompensation that will be applied to the WDATA output signal. [Table 7.5](#) shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. This starting track number can be changed by the configure command.

Table 7.5 Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY (NSEC)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default
Default: See Table 7.8 on page 49 .		

Bit 5 UNDEFINED

Should be written as a logic "0".

Bit 6 LOW POWER

A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

Bit 7 SOFTWARE RESET

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Note: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, located at the offset 0x1F in the runtime register block Separator circuits will be turned off. The controller will come out of manual low power.

Table 7.6 Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0

Datasheet**Table 7.6 Data Rates (continued)**

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format

01 = 3-Mode Drive

10 = 2 Meg Tape

Note: The DRATE and DENSEL values are mapped onto the DRV DEN pins.

Table 7.7 DRV DEN Mapping

DT1	DT0	DRV DEN1 (1)	DRV DEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 7.8 Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

MAIN STATUS REGISTER**Address 3F4 READ ONLY**

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	Reserved	DRV0 BUSY

Bit 0 DRV0 BUSY

This bit is set to 1 when a drive is in the seek portion of a command, including implied and overlapped seeks and re calibrates.

BIT 1 RESERVED

Reserved - read returns 0

Bit 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Re calibrate commands), this bit is returned to a 0 after the last command byte.

Bit 5 NON-DMA

Reserved, read '0'. This part does not support non-DMA mode.

Bit 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

Bit 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)**Address 3F5 READ/WRITE**

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. [Table 7.9](#) gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{DELAY} = \text{Fifo Threshold \#} \times \text{DATA RATE} \times 8 - 1.5 \mu\text{s}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 7.9 FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 MBPS DATA RATE
1 byte 2 bytes 8 bytes 15 bytes	$1 \times 4 \mu\text{s} - 1.5 \mu\text{s} = 2.5 \mu\text{s}$ $2 \times 4 \mu\text{s} - 1.5 \mu\text{s} = 6.5 \mu\text{s}$ $8 \times 4 \mu\text{s} - 1.5 \mu\text{s} = 30.5 \mu\text{s}$ $15 \times 4 \mu\text{s} - 1.5 \mu\text{s} = 58.5 \mu\text{s}$
FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 MBPS DATA RATE
1 byte 2 bytes 8 bytes 15 bytes	$1 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 6.5 \mu\text{s}$ $2 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 14.5 \mu\text{s}$ $8 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 62.5 \mu\text{s}$ $15 \times 8 \mu\text{s} - 1.5 \mu\text{s} = 118.5 \mu\text{s}$
FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 KBPS DATA RATE
1 byte 2 bytes 8 bytes 15 bytes	$1 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 14.5 \mu\text{s}$ $2 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 30.5 \mu\text{s}$ $8 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 126.5 \mu\text{s}$ $15 \times 16 \mu\text{s} - 1.5 \mu\text{s} = 238.5 \mu\text{s}$

DIGITAL INPUT REGISTER (DIR)**Address 3F7 READ ONLY**

This register is read-only in all modes.

PC-AT MODE

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit 0 – 6 UNDEFINED

The data bus outputs D0 – 6 are read as '0'.

Bit 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see the Runtime Register at offset 0x1E).

PS/2 MODE

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH DENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

Bit 0 nHIGH DENS

This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

Bits 1 – 2 DATA RATE SELECT

These bits control the data rate of the floppy controller. See [Table 7.6 on page 48](#) for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Bits 3 – 6 UNDEFINED

Always read as a logic “1”

Bit 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

MODEL 30 MODE

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

Bits 0 – 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See [Table 7.6](#) for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Bit 2 NOPREC

This bit reflects the value of NOPREC bit set in the CCR register.

Bit 3 DMAEN

This bit reflects the value of DMAEN bit set in the DOR register bit 3.

Bits 4 – 6 UNDEFINED

Always read as a logic “0”

Bit 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

Datasheet**7.1.2.1 Configuration Control Register (CCR)****Address 3F7 WRITE ONLY****PC/AT AND PS/2 MODES**

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

Bit 0 and 1 DATA RATE SELECT 0 and 1

These bits determine the data rate of the floppy controller. See [Table 7.6 on page 48](#) for the appropriate values.

Bit 2 – 7 RESERVED

Should be set to a logical “0”

PS/2 MODEL 30 MODE

	7	6	5	4	3	2	1	0
	0	0	0	0	0	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

Bit 0 and 1 DATA RATE SELECT 0 and 1

These bits determine the data rate of the floppy controller. See [Table 7.6 on page 48](#) for the appropriate values.

Bit 2 NO PRECOMPENSATION

This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

Bit 3 – 7 RESERVED

Should be set to a logical “0”

[Table 7.7 on page 49](#) shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

7.1.3 Status Register Encoding

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 7.10 Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 7.11 Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overflow/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.

Datasheet**Table 7.11 Status Register 1 (continued)**

BIT NO.	SYMBOL	NAME	DESCRIPTION
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the nINDEX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 7.12 Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 7.13 Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WRTprt pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the PCI_RESET# pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a PCI_RESET#, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

PCI_RESET# Pin (Hardware Reset)

The PCI_RESET# pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits in LD0-CRF0[3,2].

PC/AT Mode

The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is an active high signal.

PS/2 Mode

This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care". The DMA and interrupt functions are always enabled, and DENSEL is active low.

Model 30 mode

This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is active low.

DMA TRANSFERS

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating a DMA request cycle. DMA read, write and verify cycles are supported. The FDC supports two DMA transfer modes: Single Transfer and Burst Transfer. Burst mode is enabled via Logical Device 0-CRF0-Bit[1] (LD0-CRF0[1]).

CONTROLLER PHASES

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to [Table 7.14 on page 58](#) for the command set descriptions). These bytes of data must be transferred in the order prescribed.

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Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to “1” and “0” respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains “0” and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the “Invalid Command” condition.

EXECUTION PHASE

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by a read/write or DMA cycle depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a “fast” system.

A high value of threshold (i.e. 12) is used with a “sluggish” system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode – Transfers from the FIFO to the Host

This part does not support non-DMA mode.

Non-DMA Mode – Transfers from the Host to the FIFO

This part does not support non-DMA mode.

DMA Mode – Transfers from the FIFO to the Host

The FDC generates a DMA request cycle when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DMA request when the FIFO becomes empty by generating the proper sync for the data transfer.

DMA Mode – Transfers from the Host to the FIFO.

The FDC generates a DMA request cycle when entering the execution phase of the data transfer commands. The DMA controller must respond by placing data in the FIFO. The DMA request remains active until the FIFO becomes full. The DMA request cycle is reasserted when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will terminate the DMA cycle after a TC, indicating that no more data is required.

DATA TRANSFER TERMINATION

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overflow and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a TC cycle was received. The only difference between these implicit functions and TC cycle is that they return “abnormal termination” result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

RESULT PHASE

The generation of the interrupt determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to [Table 7.14](#) for explanations of the various symbols used. [Table 7.15](#) lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 7.14 Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1	Drive Select 0-1	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select	00 Drive 0 selected 01 not allowed 1x not allowed
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).

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Table 7.14 Description of Command Symbols (continued)

SYMBOL	NAME	DESCRIPTION
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either the DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07" would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. N SECTOR SIZE 00 128 Bytes 01 256 Bytes 02 512 Bytes 03 1024 Bytes ... 07 16K Bytes ...
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	Write '0'. This part does not support non-DMA mode.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW is defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.

Table 7.14 Description of Command Symbols (continued)

SYMBOL	NAME	DESCRIPTION
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

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7.1.4 Instruction Set**Table 7.15 Instruction Set**

READ DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS 1	DS 0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

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WRITE DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

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READ A TRACK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERSION										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

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FORMAT A TRACK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution for Each Sector Repeat:	W	C								Input Sector Parameters
	W	H								
	W	R								
	W	N								
										FDC formats an entire cylinder
Result	R	ST0								Status information after Command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

RECALIBRATE										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each seek operation.
	R	PCN								

SPECIFY										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

SENSE DRIVE STATUS										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

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SEEK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	FIFOTHR				
Execution	W	PRETRK								

RELATIVE SEEK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	FIFOTHR				
	R	PRETRK								

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READ ID										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST0								Status information after Command execution. Disk status after the Command has completed.
	R	ST1								
	R	ST2								
	R	C								
	R	H								
	R	R								
	R	N								

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST0								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

7.1.5 Data Transfer Commands

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

READ DATA

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see [Table 7.16](#)). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 7.16 Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to [Table 7.17](#).

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. [Table 7.18](#) describes the effect of the SK bit on the Read Data command execution and results. Except where noted in [Table 7.18](#), the C or R value of the sector address is automatically incremented (see [Table 7.20 on page 75](#)).

Table 7.17 Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 7.18 Skip Bit vs. Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination. Address not incremented. Next sector not searched for. Normal termination. Normal termination. Sector not read ("skipped").
0	Deleted Data	Yes	Yes	
1	Normal Data	Yes	No	
1	Deleted Data	No	Yes	

READ DELETED DATA

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

[Table 7.19](#) describes the effect of the SK bit on the Read Deleted Data command execution and results. Except where noted in [Table 7.19](#), the C or R value of the sector address is automatically incremented (see [Table 7.20](#)).

Table 7.19 Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for. Normal termination. Normal termination. Sector not read ("skipped"). Normal termination.
0	Deleted Data	Yes	No	
1	Normal Data	No	Yes	
1	Deleted Data	Yes	No	

READ A TRACK

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the nINDEX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 7.20 Result Phase

MT	HEAD	FINAL SECTOR TRANSFERRED TO	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
		HOST	C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.

LSB: Least Significant Bit, the LSB of H is complemented.

WRITE DATA

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

Transfer Capacity

EN (End of Cylinder) bit

ND (No Data) bit

Head Load, Unload Time Interval

ID information when the host terminates the command

Definition of DTL when N = 0 and when N does not = 0

WRITE DELETED DATA

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, the TC cycle cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to [Table 7.20 on page 75](#) and [Table 7.21 on page 76](#) for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 7.21 Verify Command Result Phase

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT <= # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

FORMAT A TRACK

The Format command allows an entire track to be formatted. After a pulse from the nINDEX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

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After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the nINDEX pin again and it terminates the command.

Table 7.22 on page 78 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS																		
SYSTEM 34 (DOUBLE DENSITY) FORMAT																		
GAP 4a 80x 4E	SYN C 12x 00	IAM		GA P1 50x 4E	SYN C 12x 00	IDA M	C Y L	H D	S E C	N O	C R C	GA P2 22x 4E	SYN C 12x 00	DAT A AM	DA TA	C R C	GA P3	GAP 4b
		3 x C 2	F C			3 x A 1	F E							3 x A 1	F B F 8			
SYSTEM 3740 (SINGLE DENSITY) FORMAT																		
GAP 4a 40x FF	SYN C 6x 00	IAM		GA P1 26x FF	SYN C 6x 00	IDA M	C Y L	H D	S E C	N O	C R C	GA P2 11x FF	SYN C 6x 00	DAT A AM	DA TA	C R C	GA P3	GAP 4b
		FC				FE								FB or F8				
PERPENDICULAR FORMAT																		
GAP 4a 80x 4E	SYN C 12x 00	IAM		GA P1 50x 4E	SYN C 12x 00	IDA M	C Y L	H D	S E C	N O	C R C	GA P2 41x 4E	SYN C 12x 00	DAT A AM	DA TA	C R C	GA P3	GAP 4b
		3 x C 2	F C			3 x A 1	F E							3 x A 1	F B F 8			

Table 7.22 Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
3.5" Drives	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74
GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections. GPL2 = suggested GPL value in Format A Track command. *PC/AT values (typical) **PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives. Note: All values except sector size are in hex.						

CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Re calibrate, and Seek. The other control commands do not generate an interrupt.

Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTRK0 pin from the FDD. As long as the nTRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTRK0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTRK0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

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The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once. Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

- PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
- PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated. During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1. Seek command - Step to the proper track
2. Sense Interrupt Status command - Terminate the Seek command
3. Read ID - Verify head is on proper track
4. Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command is issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

SENSE INTERRUPT STATUS

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
 - a. Read Data command
 - b. Read A Track command
 - c. Read ID command
 - d. Read Deleted Data command
 - e. Write Data command
 - f. Format A Track command
 - g. Write Deleted Data command
 - h. Verify command
2. End of Seek, Relative Seek, or Recalibrate command

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 7.23 Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

SENSE DRIVE STATUS

Sense Drive Status obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in [Table 7.24](#). The values are the same for MFM and FM.

DMA operation is selected by the ND bit. When ND is "0", the DMA mode is selected. This part does not support non-DMA mode. In DMA mode, data transfers are signaled by the DMA request cycles.

Configure

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Table 7.24 Drive Control Delays (ms)

	HUT					SRT				
	2M	1M	500K	300K	250K	2M	1M	500K	300K	250K
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2
	HLT									
	2M		1M		500K	300K		250K		
00	64		128		256	426		512		
01	0.5		1		2	3.3		4		
02	1		2		4	6.7		8		
7F	63		126		252	420		504		
7F	63.5		127		254	423		508		

Configure Default Values:

EIS - No Implied Seeks

EFIFO - FIFO Disabled

POLL - Polling Enabled

FIFOTH - FIFO Threshold Set to 1 Byte

PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTH - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

DIR	ACTION
0	Step Head Out
1	Step Head In

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 usable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

PERPENDICULAR MODE

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. [Table 7.25 on page 84](#) describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head

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is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The Format Fields table illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, an approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP = 0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

- The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
- The write pre-compensation given to a perpendicular mode drive will be 0ns.
- For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1". If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e. all conventional mode.

Table 7.25 Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

Lock

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS" by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the PCI_RESET# pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

Enhanced Dumpreg

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

COMPATIBILITY

The SCH5017 was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

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Chapter 8 Serial Port (UART)

The SCH5017 incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA, HP-SIR and ASK-IR modes of operation.

Note: The UARTs 1 and 2 may be configured to share an interrupt. Refer to [Table 29.9, "Serial Port, Logical Device 4 \[Logical Device Number = 0X04," on page 315](#) located in the [Chapter 29, Configuration](#) for more information.

Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see [Chapter 29, "Configuration," on page 301](#)). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SCH5017 contains two serial ports, each of which contain a register set as described below.

Table 8.1 Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write)

Note: *DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)**Address Offset = 0H, DLAB = 0, READ ONLY**

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)**Address Offset = 0H, DLAB = 0, WRITE ONLY**

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)**Address Offset = 1H, DLAB = 0, READ/WRITE**

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SCH5017. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic "0".

FIFO CONTROL REGISTER (FCR)**Address Offset = 2H, DLAB = X, WRITE**

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCRs are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x21).

Bit 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from

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FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the Trigger Level For The Rcvr Fifo Interrupt.

INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to [Table 8.2 on page 88](#)). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table ([Table 8.2](#)).

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic "0".

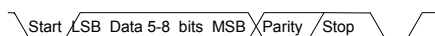
Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

BIT 7	BIT 6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

Table 8.2 Interrupt Control

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

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This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5

This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

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This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when

a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

Bit 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Datasheet**Bit 7**

This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

[Table 8.3 on page 95](#) shows the baud rates possible.

EFFECT OF THE RESET ON THE REGISTER FILE

The Reset Function (details the effect of the Reset input on each of the registers of the Serial Port.

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

- The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
- The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
- The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

- A FIFO timeout interrupt occurs if all the following conditions exist:

At least one character is in the FIFO.

The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).

The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12-bit character.

- Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

- When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
- When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

- The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
- The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

Bit 5 indicates when the XMIT FIFO is empty.

Bit 6 indicates that both the XMIT FIFO and shift register are empty.

Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 8.3 Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL (8.1)	HIGH SPEED BIT (8.2)
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note 8.1 The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Note 8.2 The High Speed bit is located in the Device Configuration Space.

Table 8.4 Reset Function

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/Read IIR/Write THR	Low
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 8.5 Pin Reset

PIN SIGNAL	RESET CONTROL	RESET STATE
TXDn	RESET	High-Z (Note 8.3)
nRTSx	RESET	High-Z (Note 8.3)
nDTRx	RESET	High-Z (Note 8.3)

Note 8.3 Serial ports 1 and 2 may be placed in the powerdown mode by clearing the associated activate bit located at CR30 or by clearing the associated power bit located in the Power Control register at CR22. When in the powerdown mode, the serial port outputs are tristated. In cases where the serial port is multiplexed as an alternate function, the corresponding output will only be tristated if the serial port is the selected alternate function.

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Table 8.6 Register Summary for an Individual UART Channel

REGISTER ADDRESS (Note 8.4)	REGISTER NAME	REGISTER SYMBOL	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (Note 8.5)
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	0	0	0	0	Enable MODEM Status Interrupt (EMSI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Transmitter Register Empty Interrupt (ETREI)	Enable Received Data Available Interrupt (ERDAI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	FIFOs Enabled (Note 8.9)	FIFOs Enabled (Note 6)	0	0	Interrupt ID Bit (Note 8.9)	Interrupt ID Bit	Interrupt ID Bit	"0" if Interrupt Pending
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 8.11)	RCVR Trigger MSB	RCVR Trigger LSB	Reserved	Reserved	DMA Mode Select (Note 8.10)	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
ADDR = 3	Line Control Register	LCR	Divisor Latch Access Bit (DLAB)	Set Break	Stick Parity	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
ADDR = 4	MODEM Control Register	MCR	0	0	0	Loop	OUT2 (Note 8.7)	OUT1 (Note 8.7)	Request to Send (RTS)	Data Terminal Ready (DTR)
ADDR = 5	Line Status Register	LSR	Error in RCVR FIFO (Note 8.9)	Transmitter Empty (TEMT) (Note 8.6)	Transmitter Holding Register (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
ADDR = 6	MODEM Status Register	MSR	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)

Table 8.6 Register Summary for an Individual UART Channel (continued)

REGISTER ADDRESS (Note 8.4)	REGISTER NAME	REGISTER SYMBOL	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADDR = 7	Scratch Register (Note 8.8)	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Note 8.4 DLAB is Bit 7 of the Line Control Register (ADDR = 3). Note 8.5 Bit 0 is the least significant bit. It is the first bit serially transmitted or received. Note 8.6 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty. Note 8.7 This bit no longer has a pin associated with it. Note 8.8 When operating in the XT mode, this register is not available. Note 8.9 These bits are always zero in the non-FIFO mode. Note 8.10 Writing a one to this bit has no effect. DMA modes are not supported in this chip. Note 8.11 The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (runtime register at offset 0x20) and UART2 FIFO Control Shadow Register (runtime register at offset 0x21).										

NOTES ON SERIAL PORT OPERATION

FIFO Mode Operation:

General

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

8.0.1 TXD2 Pin

The TXD2 signal is located on the GP53/TXD2(IRTx) pin. The operation of this pin following a power cycle is defined in [Section 8.1.1, "IR Transmit Pin," on page 100](#).

8.1 Infrared Interface

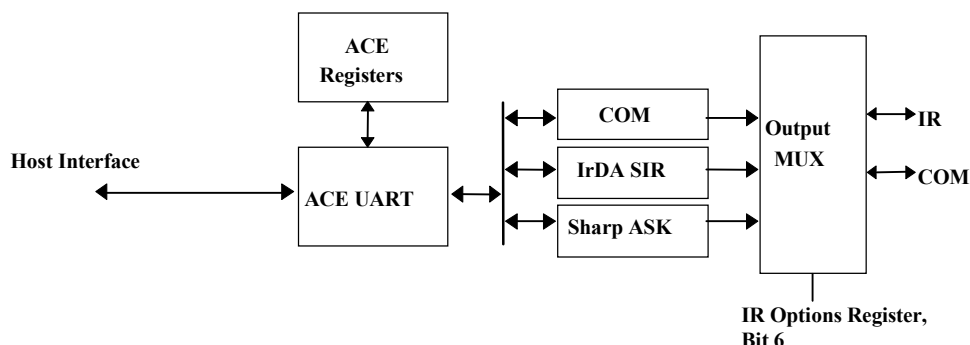
The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two IR implementations have been provided for the second UART in this chip (logical device 5), IrDA and Amplitude Shift Keyed IR. The IR transmission can use the standard UART2 TXD2 and RXD2 pins. These can be selected through the configuration registers.

IrDA 1.0 allows serial communication at baud rates up to 115.2 kbps. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single IR pulse at the beginning of the serial bit time. A one is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform.

The Amplitude Shift Keyed IR allows asynchronous serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

If the Half Duplex option is chosen, there is a time-out when the direction of the transmission is changed. This time-out starts at the last bit transferred during a transmission and blocks the receiver input until the timeout expires. If the transmit buffer is loaded with more data before the time-out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time-out expires after the last receive bit has been received. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The IR half duplex time-out is programmable via CRF2 in Logical Device 5. This register allows the time-out to be programmed to any value between 0 and 10msec in 100usec increments.

The following figure shows the block diagram of the IR components in the SCH5017:



8.1.1 IR Transmit Pin

The following description describes the state of the GP53/TXD2(IRTX) pin following a power cycle.

GP53/TXD2(IRTX) Pin. This pin defaults to the GPIO input function on a VTR POR.

The GP53/TXD2(IRTX) pin will be tristate following a VCC POR, VTR POR, Soft Reset, or PCI Reset when it is configured for the TXD2 (IRTX) function. It will remain tristate until the UART is powered. Once the UART is powered, the state of the pin will be determined by the UART block. If VCC>2.4V and GP53 function is selected the pin will reflect the current state of GP53.

Note: External hardware should be implemented to protect the transceiver when the IRTX2 pin is tristated.

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Chapter 9 Parallel Port

The SCH5017 incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power- down, changing the base address of the parallel port, and selecting the mode of operation.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below:

DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H
EPP ADDR PORT	BASE ADDRESS + 03H
EPP DATA PORT 0	BASE ADDRESS + 04H
EPP DATA PORT 1	BASE ADDRESS + 05H
EPP DATA PORT 2	BASE ADDRESS + 06H
EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	NOTE
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	1
CONTROL PORT	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2

Notes:

1. These registers are available in all modes.
2. These registers are only available in EPP mode.

Table 9.1 Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	83	nSTROBE	nWrite	nStrobe
2-9	68-75	PD<0:7>	PData<0:7>	PData<0:7>
10	80	nACK	Intr	nAck
11	79	BUSY	nWait	Busy, PeriphAck(3)
12	78	PE	(User Defined)	PError, nAckReverse (3)
13	77	SLCT	(User Defined)	Select
14	82	nALF	nDatastb	nAutoFd, HostAck(3)
15	81	nERROR	(User Defined)	nFault (1) nPeriphRequest (3)
16	66	nINIT	nRESET	nInit(1) nReverseRqst(3)
17	67	nSLCTIN	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the *IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14*, July 14, 1993. This document is available from Microsoft.

9.0.1 IBM XT/AT Compatible, Bi-Directional and EPP Modes

DATA PORT

ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the internal data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of a read cycle. The bits of the Status Port are defined as follows:

Bit 0 TMOUT - TIME OUT

This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic 0 means that no time out error has occurred; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. If the TIMEOUT_SELECT bit (bit 4 of the Parallel Port Mode Register 2, 0xF1 in Logical Device 3 Configuration Registers) is '0', writing a one to this bit clears the TMOUT status bit. Writing a zero to this bit has no effect. If the TIMEOUT_SELECT bit (bit 4 of the

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Parallel Port Mode Register 2, 0xF1 in Logical Device 3 Configuration Registers) is '1', the TMOUT bit is cleared on the trailing edge of a read of the EPP Status Register.

Bits 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

Bit 3 nERR – nERROR

The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

Bit 4 SLT - Printer Selected Status

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

Bit 5 PE - Paper End

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

Bit 6 nACK - Acknowledge

The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

Bit 7 nBUSY - nBUSY

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

CONTROL PORT**ADDRESS OFFSET = 02H**

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

Bit 0 STROBE - Strobe

This bit is inverted and output onto the nSTROBE output.

Bit 1 AUTOFD - Autofeed

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

Bit 2 nINIT - Initiate Output

This bit is output onto the nINIT output without inversion.

Bit 3 SLCTIN - Printer Select Input

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

Bit 4 IRQE - Interrupt Request Enable

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

Bit 5 PCD - PARALLEL CONTROL DIRECTION

Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

EPP ADDRESS PORT**ADDRESS OFFSET = 03H**

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP ADDRESS WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

EPP DATA PORT 0**ADDRESS OFFSET = 04H**

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP DATA WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

EPP DATA PORT 1**ADDRESS OFFSET = 05H**

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2**ADDRESS OFFSET = 06H**

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3**ADDRESS OFFSET = 07H**

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 OPERATION

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from

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the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

- If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
- If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host initiates an I/O write cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
6.
 - a. The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
 - b. The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.
7. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
8. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

EPP 1.9 READ

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. The chip inserts wait states into the LPC I/O read cycle until it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

- If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.
- If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nWRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host initiates an I/O read cycle to the selected EPP register.

2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip tri-states the PData bus and deasserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
5. Peripheral drives PData bus valid.
6. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
- 7.
- a. The chip latches the data from the PData bus for the internal data bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.
- b. The chip drives the sync that indicates that no more wait states are required and drives valid data onto the LAD[3:0] signals, followed by the TAR to complete the read cycle.
8. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

EPP 1.7 OPERATION

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to the end of the cycle. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for an EPP read.

EPP 1.7 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. The chip inserts wait states into the I/O write cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

- The host sets PDIR bit in the control register to a logic "0". This asserts nWRITE.
- The host initiates an I/O write cycle to the selected EPP register.
- The chip places address or data on PData bus.
- Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
- If nWAIT is asserted, the chip inserts wait states into I/O write cycle until the peripheral deasserts nWAIT or a time-out occurs.
- The chip drives the final sync, deasserts nDATASTB or nADDRSTRB and latches the data from the internal data bus for the PData bus.
- Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Datasheet**EPP 1.7 READ**

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. The chip inserts wait states into the I/O read cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

- The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.
- The host initiates an I/O read cycle to the selected EPP register.
- Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
- If nWAIT is asserted, the chip inserts wait states into the I/O read cycle until the peripheral deasserts nWAIT or a time-out occurs.
- The Peripheral drives PData bus valid.
- The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
- The chip drives the final sync and deasserts nDATASTB or nADDRSTRB.
- Peripheral tri-states the PData bus.
- Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 9.2 EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
nWAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
nDATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
nRESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
nADDRSTB	Address Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.
Notes: 1. SPP and EPP can use 1 common register. 2. nWrite is the only EPP output that can be over-riden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.			

9.0.2 Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel Interlocked handshake, for fast reliable transfer
Optional single byte RLE compression for improved throughput (64:1)
Channel addressing for low-cost peripherals
Maintains link and data layer separation
Permits the use of active output drivers
permits the use of adaptive signal timing
Peer-to-peer capability.

VOCABULARY

The following terms are used in this document:

- assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
- forward: Host to Peripheral communication.
- reverse: Peripheral to Host communication
- Pword: A port word; equal in size to the width of the LPC interface. For this implementation, PWord is always 8 bits.
- 1 A high level.
- 0 A low level.

These terms may be considered synonymous:

PeriphClk, nAck

HostAck, nAutoFd

PeriphAck, Busy

nPeriphRequest, nFault

nReverseRequest, nInit

nAckReverse, PError

Xflag, Select

ECPMode, nSelectIn

HostClk, nStrobe

Reference Document: *IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard*, Rev 1.14, July 14, 1993. This document is available from Microsoft.

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The bit map of the Extended Parallel Port registers is:

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dscr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16 byte FIFO.
3. The ECP Parallel Port Config Reg B reflects the IRQ and DMA channel selected by the Configuration Registers.

ECP IMPLEMENTATION STANDARD

This specification describes the standard interface to the Extended Capabilities Port (ECP). All LPC devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the *IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14*, July 14, 1993. This document is available from Microsoft.

Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 9.3 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

REGISTER DEFINITIONS

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. [Table 9.4](#) lists these dependencies. Operation of the devices in modes other than those specified is undefined.

Table 9.4 ECP Register Definitions

NAME	ADDRESS (NOTE 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dscr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register
Notes: 1. These addresses are added to the parallel port base address as selected by configuration register or jumpers. 2. All addresses are qualified with AEN. Refer to the AEN pin definition.			

Table 9.5 Mode Descriptions

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	Reserved
110	Test mode
111	Configuration mode
*Refer to ECR Register Description	

DATA AND ECPAFIFO PORT**ADDRESS OFFSET = 00H**

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to [Figure 32.18 ECP Parallel Port Forward Timing](#) on page 340, located in [Chapter 32](#) of this data sheet.

DEVICE STATUS REGISTER (DSR)**ADDRESS OFFSET = 01H**

The Status Port is located at an offset of '01H' from the base address. Bits0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

Bit 3 nFault

The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

Bit 4 Select

The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

Bit 5 PError

The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

Bit 6 nAck

The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

Bit 7 nBusy

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

DEVICE CONTROL REGISTER (DCR)**ADDRESS OFFSET = 02H**

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

Bit 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

Bit 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAutoFd output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

Bit 2 nINIT - INITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

Bit 3 SELECTIN

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

Bit 4 ackIntEn - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

Datasheet**Bit 5 DIRECTION**

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)

ADDRESS OFFSET = 400H

Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)

ADDRESS OFFSET = 400H

Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)

ADDRESS OFFSET = 400H

Mode = 111

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)

ADDRESS OFFSET = 401H

Mode = 111

Bit 7 compress

This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression.

Bit 6 intrValue

Returns the value of the interrupt to determine possible conflicts.

Bit [5:3] Parallel Port IRQ (read-only)

to [Table 9.7 on page 116](#).

Bits [2:0] Parallel Port DMA (read-only)

to [Table 9.8 on page 116](#).

ecr (Extended Control Register)

ADDRESS OFFSET = 402H

Mode = all

This register controls the extended ECP parallel port functions.

Bits 7,6,5

These bits are Read/Write and select the Mode.

Bit 4 nErrIntrEn

Read/Write (Valid only in ECP Mode)

1: Disables the interrupt generated on the asserting edge of nFault.

0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

Bit 3 dmaEn

Read/Write

1: Enables DMA (DMA starts when serviceIntr is 0).

0: Disables DMA unconditionally.

Bit 2 serviceIntr

Read/Write

1: Disables DMA and all of the service interrupts.

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0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.

case dmaEn=1:

During DMA (this bit is set to a 1 when terminal count is reached).

case dmaEn=0 direction=0:

This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.

case dmaEn=0 direction=1:

This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

Bit 1 full

Read only

1: The FIFO cannot accept another byte or the FIFO is completely full.

0: The FIFO has at least 1 free byte.

Bit 0 empty

Read only

1: The FIFO is completely empty.

0: The FIFO contains at least 1 byte of data.

Table 9.6 Extended Control Register (a)

R/W	MODE
000:	Standard Parallel Port Mode. In this mode the FIFO is reset and common drain drivers are used on the control lines (nStrobe, nAutoFd, nIntr and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register L3-CRF0. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the configA, configB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

Table 9.7 Extended Control Register (b)

IRQ SELECTED	CONFIG REG B BITS 5:3
15	110
14	101
11	100
10	011
9	010
7	001
5	111
All others	000

Table 9.8 Extended Control Register (c)

IRQ SELECTED	CONFIG REG B BITS 5:3
3	011
2	010
1	001
All others	000

OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

Datasheet**ECP OPERATION**

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

Set `Direction` = 0, enabling the drivers.

Set `strobe` = 0, causing the `nStrobe` signal to default to the deasserted state.

Set `autoFd` = 0, causing the `nAutoFd` signal to default to the deasserted state.

Set `mode` = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the `ecpAFifo` or `ecpDFifo` respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the `ecpDFifo` as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

TERMINATION FROM ECP MODE

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

COMMAND/DATA

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8 bit commands.

When in the forward direction, normal data is transferred when `HostAck` is high and an 8 bit command is transferred when `HostAck` is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when `PeriphAck` is high and an 8 bit command is transferred when `PeriphAck` is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 9.9 Channel/Data Commands Supported in ECP Mode

Forward Channel Commands (HostAck Low) Reverse Channel Commands (PeriphAck Low)	
D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

DATA COMPRESSION

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

PIN DEFINITION

The drivers for nStrobe, nAutoFd, nIntr and nSelectIn are open-drain in mode 000 and are push-pull in all other modes.

LPC CONNECTIONS

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

INTERRUPTS

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupts generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

An interrupt is generated when:

1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC cycle is received.
2. For Programmed I/O:
 - a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
 - b. When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.
3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO OPERATION

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or DMA cycle depending on the selection of DMA or Programmed I/O mode.



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The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system. A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA TRANSFERS

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by encoding the LDRQ# pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests a DMA cycle shall not be requested for more than 32 DMA cycles in a row. The FIFO is enabled directly by the host initiating a DMA cycle for the requested channel, and addresses need not be valid. An interrupt is generated when a TC cycle is received. (Note: The only way to properly terminate DMA transfers is with a TC cycle.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA MODE - TRANSFERS FROM THE FIFO TO THE HOST

Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP requests a DMA cycle whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP stops requesting DMA cycles when the FIFO becomes empty or when a TC cycle is received, indicating that no more data is required. If the ECP stops requesting DMA cycles due to the FIFO going empty, then a DMA cycle is requested again as soon as there is one byte in the FIFO. If the ECP stops requesting DMA cycles due to the TC cycle, then a DMA cycle is requested again when there is one byte in the FIFO, and serviceIntr has been re-enabled.

PROGRAMMED I/O MODE OR NON-DMA MODE

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the interrupt. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

PROGRAMMED I/O - TRANSFERS FROM THE FIFO TO THE HOST

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

$\text{readIntrThreshold} = (16 - \langle \text{threshold} \rangle)$ data bytes in FIFO

An interrupt is generated when `serviceIntr` is 0 and the number of bytes in the FIFO is greater than or equal to $(16 - \langle \text{threshold} \rangle)$. (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO). The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of $(16 - \langle \text{threshold} \rangle)$ bytes may be read from the FIFO in a single burst.

PROGRAMMED I/O - TRANSFERS FROM THE HOST TO THE FIFO

In the forward direction an interrupt occurs when `serviceIntr` is 0 and there are `writeIntrThreshold` or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with `writeIntrThreshold` bytes.

$\text{writeIntrThreshold} = (16 - \langle \text{threshold} \rangle)$ free bytes in FIFO

An interrupt is generated when `serviceIntr` is 0 and the number of bytes in the FIFO is less than or equal to $\langle \text{threshold} \rangle$. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of $(16 - \langle \text{threshold} \rangle)$ bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

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Chapter 10 Power Management

Power management capabilities are provided for the following logical devices: floppy disk, UART 1, UART 2 and the parallel port.

Note: Each Logical Device may be place in powerdown mode by clearing the associated activate bit located at CR30 or by clearing the associated power bit located in the Power Control register at CR22.

FDC Power Management

Direct power management is controlled by CR22. Refer to CR22 for more information.

FDD Interface Pins

All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED.

[Table 10.1, "State of Floppy Disk Drive Interface Pins in Powerdown"](#) depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 10.1 State of Floppy Disk Drive Interface Pins in Powerdown

FDD PINS	STATE IN POWERDOWN
INPUT PINS	
nRDATA	Input
nWRTprt	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
OUTPUT PINS	
nMTR0	Tristated
nDS0	Tristated
nDIR	Tristated
nSTEP	Tristated
nWDATA	Tristated
nWGATE	Tristated
nHDSEL	Tristated
DRVden[0:1]	Tristated

UART Power Management

Direct power management is controlled by CR22. Refer to CR22 for more information.

Parallel Port

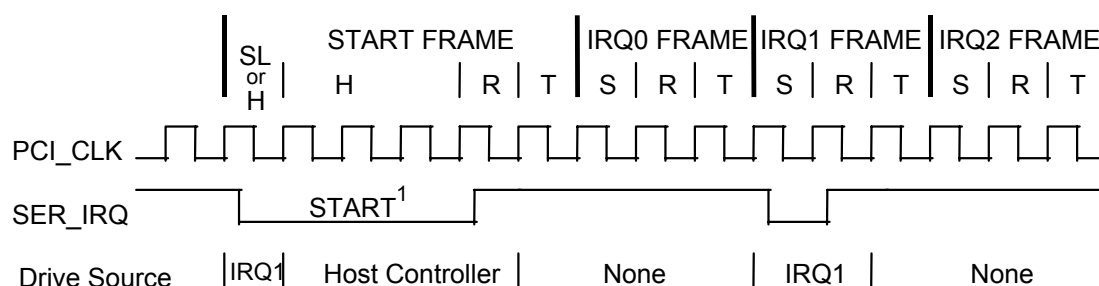
Direct power management is controlled by CR22. Refer to CR22 for more information.

Chapter 11 Serial IRQ

The SCH5017 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0.

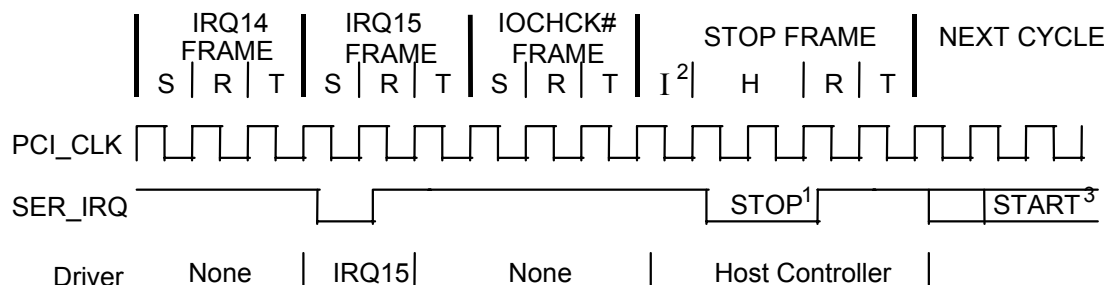
TIMING DIAGRAMS FOR SER_IRQ CYCLE

- a. Start Frame timing with source sampled a low pulse on IRQ1



Notes:

1. H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample
 2. Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.
- b. Stop Frame Timing with Host using 17 SER_IRQ sampling period



Notes:

1. H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle
2. The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.
3. There may be none, one or more Idle states during the Stop Frame.
4. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.

SER_IRQ CYCLE CONTROL

There are two modes of operation for the SER_IRQ Start Frame

1. **Quiet (Active) Mode:** Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active

between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The SCH5017) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle

2. **Continuous (Idle) Mode:** Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

SER_IRQ DATA FRAME

Once a Start Frame has been initiated, the SCH5017 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the SCH5017 must drive the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ must be left tri-stated. During the Recovery phase the SCH5017 must drive the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the SCH5017 must tri-state the SER_IRQ. The SCH5017 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, $(6 \times 3) - 1 = 17^{\text{th}}$ clock after the rising edge of the Start Pulse).

SER_IRQ SAMPLING PERIODS		
SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	nIO_SMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29

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SER_IRQ SAMPLING PERIODS		
SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices 0 (FDC), 3 (Par Port), 4 (Ser Port 1), 5 (Ser Port 2), and 7 (KBD) shall have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the nIO_SMI pin via bit 7 of the SMI Enable Register 2.

STOP CYCLE CONTROL

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuous mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

LATENCY

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84 μ S with a 25MHz PCI Bus or 2.88 μ S with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR READ LATENCY

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

AC/DC SPECIFICATION ISSUE

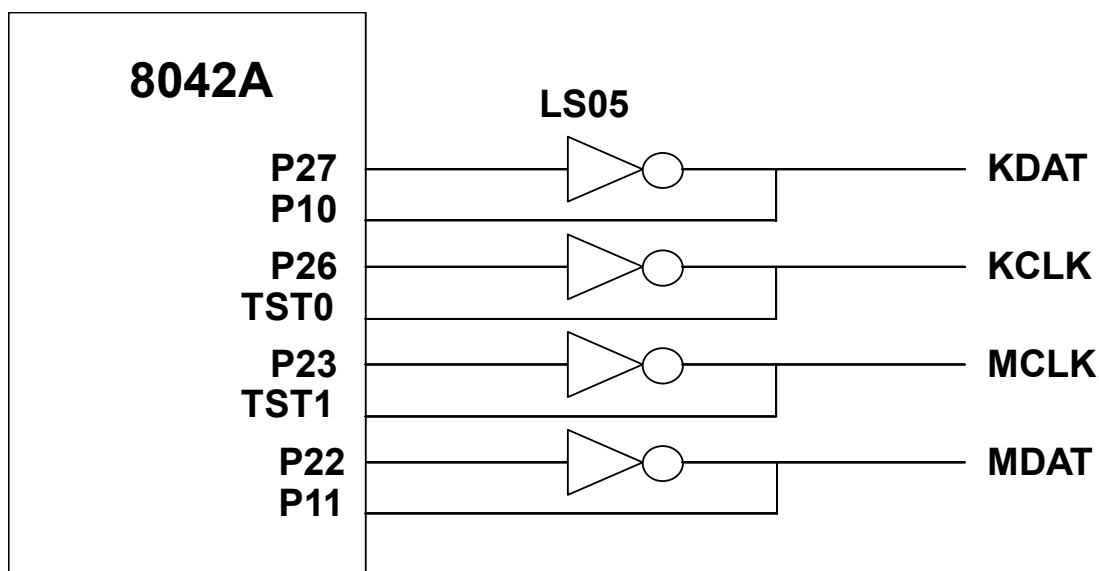
All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

RESET AND INITIALIZATION

The SER_IRQ bus uses PCI_RESET# as its reset signal. The SER_IRQ pin is tri-stated by all agents while PCI_RESET# is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee SER_IRQ bus is in IDLE state before the system configuration changes.

Chapter 12 8042 Keyboard Controller Description

The SCH5017 is a Super I/O and Universal Keyboard Controller that is designed for intelligent keyboard management in desktop computer applications. The Universal Keyboard Controller uses an 8042 microcontroller CPU core. This section concentrates on the SCH5017 enhancements to the 8042. For general information about the 8042, refer to the "Hardware Description of the 8042" in the *8-Bit Embedded Controller Handbook*.



Keyboard and Mouse Interface

Figure 12.1 SCH5017 Keyboard and Mouse Interface

KIRQ is the Keyboard IRQ

MIRQ is the Mouse IRQ

Port 21 is used to create a GATEA20 signal from the SCH5017.

12.0.1 Keyboard Interface

The SCH5017 LPC interface is functionally compatible with the 8042 style host interface. It consists of the D0-7 data signals; the read and write signals and the Status register, Input Data register, and Output Data register. [Table 12.1](#) shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQs.

Table 12.1 I/O Address Map

ADDRESS	COMMAND	BLOCK	FUNCTION (SEE Note 12.1)
0x60	Write	KDATA	Keyboard Data Write (C/D=0)
	Read	KDATA	Keyboard Data Read
0x64	Write	KDCTL	Keyboard Command Write (C/D=1)
	Read	KDCTL	Keyboard Status Read
Note 12.1 These registers consist of three separate 8-bit registers. Status, Data/Command Write and Data Read.			

Keyboard Data Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

Keyboard Data Read

This is an 8 bit read only register. If enabled by “ENABLE FLAGS”, when read, the KIRQ output is cleared and the OBF flag in the status register is cleared. If not enabled, the KIRQ and/or AUXOBF1 must be cleared in software.

Keyboard Command Write

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

Keyboard Status Read

This is an 8 bit read only register. Refer to the description of the Status Register for more information.

CPU-to-Host Communication

The SCH5017 CPU can write to the Output Data register via register DBB. A write to this register automatically sets Bit 0 (OBF) in the Status register. See [Table 12.2](#).

Table 12.2 Host Interface Flags

8042 INSTRUCTION	FLAG
OUT DBB	Set OBF, and, if enabled, the KIRQ output signal goes high

Host-to-CPU Communication

The host system can send both commands and data to the Input Data register. The CPU differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is “1”, the CPU interprets the register contents as a command. When bit 3 is “0”, the CPU interprets the register contents as data. During a host write operation, bit 3 is set to “1” if SA2 = 1 or reset to “0” if SA2 = 0.

KIRQ

If “EN FLAGS” has been executed and P24 is set to a one: the OBF flag is gated onto KIRQ. The KIRQ signal can be connected to system interrupt to signify that the SCH5017 CPU has written to the output data register via “OUT DBB,A”. If P24 is set to a zero, KIRQ is forced low. On power-up, after a valid RST pulse has been delivered to the device, KIRQ is reset to 0. KIRQ will normally reflects the status of writes “DBB”. (KIRQ is normally selected as IRQ1 for keyboard support.)

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If "EN FLAGS" has not been executed: KIRQ can be controlled by writing to P24. Writing a zero to P24 forces KIRQ low; a high forces KIRQ high.

MIRQ

If "EN FLAGS" has been executed and P25 is set to a one; IBF is inverted and gated onto MIRQ. The MIRQ signal can be connected to system interrupt to signify that the SCH5017 CPU has read the DBB register. If "EN FLAGS" has not been executed, MIRQ is controlled by P25. Writing a zero to P25 forces MIRQ low, a high forces MIRQ high. (MIRQ is normally selected as IRQ12 for mouse support).

Gate A20

A general purpose P21 is used as a software controlled Gate A20 or user defined output.

8042 PINS

The 8042 functions P17, P16 and P12 are implemented as in a true 8042 part. Reference the 8042 spec for all timing. A port signal of 0 drives the output to 0. A port signal of 1 causes the port enable signal to drive the output to 1 within 20-30nsec. After 500nsec (six 8042 clocks) the port enable goes away and the external pull-up maintains the output signal as 1.

In 8042 mode, the pins can be programmed as open drain. When programmed in open drain mode, the port enables do not come into play. If the port signal is 0 the output will be 0. If the port signal is 1, the output tristates: an external pull-up can pull the pin high, and the pin can be shared. In 8042 mode, the pins cannot be programmed as input nor inverted through the GP configuration registers.

12.0.2 External Keyboard and Mouse Interface

Industry-standard PC-AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the SCH5017 provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The SCH5017 has four high-drive, open-drain output, bidirectional port pins that can be used for external serial interfaces, such as external keyboard and PS/2-type mouse interfaces. They are KCLK, KDAT, MCLK, and MDAT. P26 is inverted and output as KCLK. The KCLK pin is connected to TEST0. P27 is inverted and output as KDAT. The KDAT pin is connected to P10. P23 is inverted and output as MCLK. The MCLK pin is connected to TEST1. P22 is inverted and output as MDAT. The MDAT pin is connected to P11.

Note: External pull-ups may be required.

12.0.2.1 Keyboard/Mouse Swap Bit

There is a Kbd/mouse Swap bit in the Keyboard Select configuration register located at 0xF1 in Logical Device 7. This bit can be used to swap the keyboard and mouse clock and data pins into/out of the 8042. The default value of this bit is '0' on VCC POR, VTR POR and PCI Reset.

1=internally swap the KCLK pin and the MCLK pin, and the KDAT pin and the MDAT pin into/out of the 8042.

0=do not swap the keyboard and mouse clock and data pins

12.0.3 Keyboard Power Management

The keyboard provides support for two power-saving modes: soft power-down mode and hard power-down mode. In soft power-down mode, the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the 8042 is stopped.

Soft Power-Down Mode

This mode is entered by executing a HALT instruction. The execution of program code is halted until either RESET is driven active or a data byte is written to the DBBIN register by a master CPU. If this

mode is exited using the interrupt, and the IBF interrupt is enabled, then program execution resumes with a CALL to the interrupt routine, otherwise the next instruction is executed. If it is exited using RESET then a normal reset sequence is initiated and program execution starts from program memory location 0.

Hard Power-Down Mode

This mode is entered by executing a STOP instruction. The oscillator is stopped by disabling the oscillator driver cell. When either RESET is driven active or a data byte is written to the DBBIN register by a master CPU, this mode will be exited (as above). However, as the oscillator cell will require an initialization time, either RESET must be held active for sufficient time to allow the oscillator to stabilize. Program execution will resume as above.

12.0.4 Interrupts

The SCH5017 provides the two 8042 interrupts: IBF and the Timer/Counter Overflow.

12.0.5 Memory Configurations

The SCH5017 provides 2K of on-chip ROM and 256 bytes of on-chip RAM.

12.0.6 Register Definitions

Host I/F Data Register

The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register will load the Keyboard Data Read Buffer, set the OBF flag and set the KIRQ output if enabled. A read of this register will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the KIRQ and Status register descriptions for more information.

Host I/F Status Register

The Status register is 8 bits wide.

Table 12.3 shows the contents of the Status register.

Table 12.3 Status Register

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	UD	UD	C/D	UD	IBF	OBF

Status Register

This register is cleared on a reset. This register is read-only for the Host and read/write by the SCH5017 CPU.

UD Writable by SCH5017 CPU. These bits are user-definable.

C/D (Command Data)-This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host data/command write operation, this bit is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

IBF (Input Buffer Full)- This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the SCH5017 CPU's nIBF (MIRQ) interrupt if enabled. When the SCH5017 CPU reads the input data register (DBB), this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF (Output Buffer Full) - This flag is set to whenever the SCH5017 CPU write to the output data register (DBB). When the host system reads the output data register, this bit is automatically reset.

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12.0.7 External Clock Signal

The SCH5017 Keyboard Controller clock source is a 12 MHz clock generated from a 14.318 MHz clock. The reset pulse must last for at least 24 16 MHz clock periods. The pulse-width requirement applies to both internally (VCC POR) and externally generated reset signals. In power-down mode, the external clock signal is not loaded by the chip.

12.0.8 Default Reset Conditions

The SCH5017 has one source of hardware reset: an external reset via the PCI_RESET# pin. Refer to [Table 12.4](#) for the effect of each type of reset on the internal registers.

Table 12.4 Resets

DESCRIPTION	HARDWARE RESET (PCI_RESET#)
KCLK	Low
KDAT	Low
MCLK	Low
MDAT	Low
Host I/F Data Reg	N/A
Host I/F Status Reg	00H
Note: N/A = Not Applicable	

GATEA20 AND KEYBOARD RESET

The SCH5017 provides two options for GateA20 and Keyboard Reset: 8042 Software Generated GateA20 and KRESET and Port 92 Fast GateA20 and KRESET.

PORT 92 FAST GATEA20 AND KEYBOARD RESET

Port 92 Register

This port can only be read or written if Port 92 has been enabled via bit 2 of the KRST_GA20 Register (Logical Device 7, 0xF0) set to 1.

This register is used to support the alternate reset (nALT_RST) and alternate A20 (ALT_A20) functions.

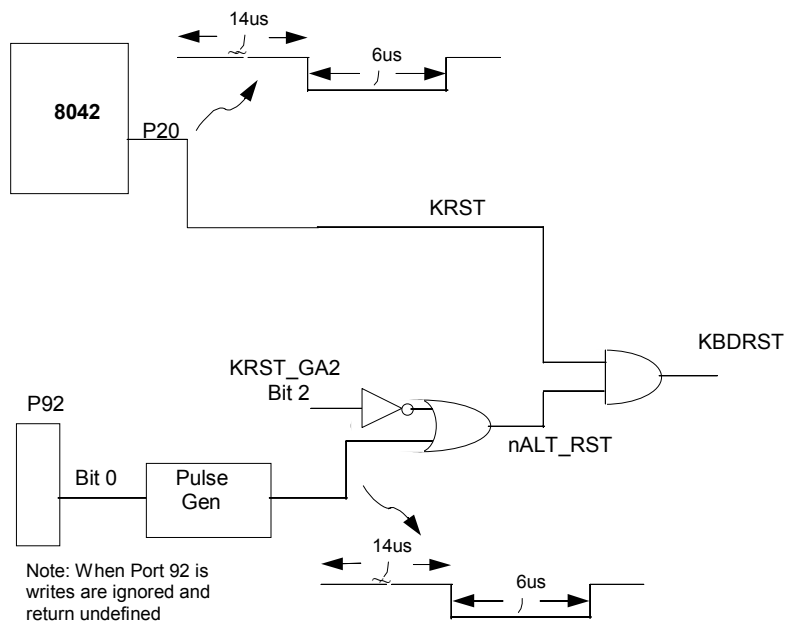
NAME	PORT 92
Location	92h
Default Value	24h
Attribute	Read/Write
Size	8 bits

PORT 92 REGISTER	
BIT	FUNCTION
7:6	Reserved. Returns 00 when read
5	Reserved. Returns a 1 when read
4	Reserved. Returns a 0 when read
3	Reserved. Returns a 0 when read
2	Reserved. Returns a 1 when read
1	ALT_A20 Signal control. Writing a 0 to this bit causes the ALT_A20 signal to be driven low. Writing a 1 to this bit causes the ALT_A20 signal to be driven high.
0	Alternate System Reset. This read/write bit provides an alternate system reset function. This function provides an alternate means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the Keyboard controller. This bit is set to a 0 by a system reset. Writing a 1 to this bit will cause the nALT_RST signal to pulse active (low) for a minimum of 1 μ s after a delay of 500 ns. Before another nALT_RST pulse can be generated, this bit must be written back to a 0.

NGATEA20		
8042 P21	ALT_A20	SYSTEM NA20M
0	0	0
0	1	1
1	0	1
1	1	1

Bit 0 of Port 92, which generates the nALT_RST signal, is used to reset the CPU under program control. This signal is AND'ed together externally with the reset signal (nKBDRST) from the keyboard controller to provide a software means of resetting the CPU. This provides a faster means of reset than is provided by the keyboard controller. Writing a 1 to bit 0 in the Port 92 Register causes this signal to pulse low for a minimum of 6 μ s, after a delay of a minimum of 14 μ s. Before another nALT_RST pulse can be generated, bit 0 must be set to 0 either by a system reset of a write to Port 92. Upon reset, this signal is driven inactive high (bit 0 in the Port 92 Register is set to 0).

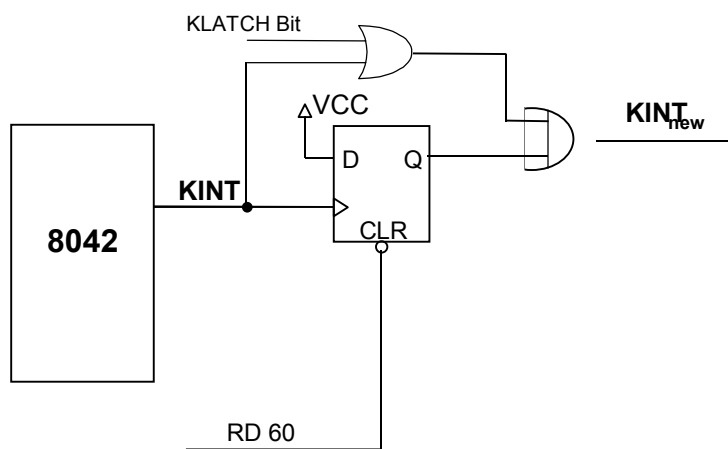
If Port 92 is enabled, i.e., bit 2 of KRST_GA20 is set to 1, then a pulse is generated by writing a 1 to bit 0 of the Port 92 Register and this pulse is AND'ed with the pulse generated from the 8042. This pulse is output on pin KRESET and its polarity is controlled by the GPIO polarity configuration.

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Bit 1 of Port 92, the ALT_A20 signal, is used to force nA20M to the CPU low for support of real mode compatible software. This signal is externally OR'ed with the A20GATE signal from the keyboard controller and CPURST to control the nA20M input of the CPU. Writing a 0 to bit 1 of the Port 92 Register forces ALT_A20 low. ALT_A20 low drives nA20M to the CPU low, if A20GATE from the keyboard controller is also low. Writing a 1 to bit 1 of the Port 92 Register forces ALT_A20 high. ALT_A20 high drives nA20M to the CPU high, regardless of the state of A20GATE from the keyboard controller. Upon reset, this signal is driven low.

Latches On Keyboard and Mouse IRQs

The implementation of the latches on the keyboard and mouse interrupts is shown below.

**Figure 12.2 Keyboard Latch**

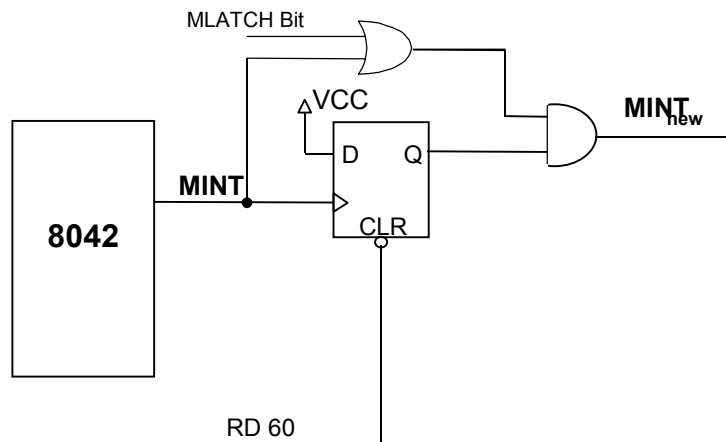


Figure 12.3 Mouse Latch

The KLATCH and MLATCH bits are located in the KRST_GA20 register, in Logical Device 7 at 0xF0.

These bits are defined as follows:

Bit[4]: MLATCH – Mouse Interrupt latch control bit. 0=MINT is the 8042 MINT ANDed with Latched MINT (default), 1=MINT is the latched 8042 MINT.

Bit[3]: KLATCH – Keyboard Interrupt latch control bit. 0=KINT is the 8042 KINT ANDed with Latched KINT (default), 1=KINT is the latched 8042 KINT.

See [Table 29.11, “KYBD. Logical Device 7 \[Logical Device Number = 0X07\],” on page 317](#) for a description of this register.

12.0.9 Keyboard and Mouse PME Generation

The SCH5017 sets the associated PME Status bits when the following conditions occur:

Keyboard Interrupt

- Mouse Interrupt
- Active Edge on Keyboard Data Signal (KDAT)
- Active Edge on Mouse Data Signal (MDAT)

These events can cause a PME to be generated if the associated PME Wake Enable register bit and the global PME_EN bit are set. Refer to [Chapter 15, “PME Support,” on page 147](#) for more details on the PME interface logic and refer to [Chapter 28, “Runtime Registers,” on page 271](#) for details on the PME Status and Enable registers.

The keyboard interrupt and mouse interrupt PMEs can be generated when the part is powered by VCC. The keyboard data and mouse data PMEs can be generated both when the part is powered by VCC, and when the part is powered by VTR (VCC=0).

When using the keyboard and mouse data signals for wakeup, it may be necessary to isolate the keyboard signals (KCLK, KDAT, MCLK, MDAT) from the 8042 prior to entering certain system sleep states. This is due to the fact that the normal operation of the 8042 can prevent the system from entering a sleep state or trigger false PME events. The SCH5017 has “isolation” bits for the keyboard and mouse signals, which allow the keyboard and mouse data signals to go into the wakeup logic but block the clock and data signals from the 8042. These bits may be used anytime it is necessary to isolate the 8042 keyboard and mouse signals from the 8042 before entering a system sleep state.

See the SMSC Application Note (AN 8-8) “Keyboard and Mouse Wakeup Functionality”, dated 03/23/02 for more information.

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The bits used to isolate the keyboard and mouse signals from the 8042 are located in Logical Device 7, Register 0xF0 (KRST_GA20) and are defined below. These bits reset on VTR POR only.

Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect the MDAT signal to The mouse wakeup (PME) logic.

1 = block mouse clock and data signals into 8042

0 = do not block mouse clock and data signals into 8042

Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect the KDAT signal to the keyboard wakeup (PME) logic.

1 = block keyboard clock and data signals into 8042

0 = do not block keyboard clock and data signals into 8042

When the keyboard and/or mouse isolation bits are used, it may be necessary to reset the 8042 upon exiting the sleep state. If either of the isolation bits is set prior to entering a sleep state where VCC goes inactive (S3-S5), then the 8042 must be reset upon exiting the sleep mode. Write 0x40 to global configuration register 0x2C to reset the 8042. The 8042 must then be taken out of reset by writing 0x00 to register 0x2C since the bit that resets the 8042 is not self-clearing.

Caution: Bit 6 of configuration register 0x2C is used to put the 8042 into reset - do not set any of the other bits in register 0x2C, as this may produce undesired results.

It is not necessary to reset the 8042 if the isolation bits are used for a sleep state where VCC does not go inactive (S1, S2).

USER'S NOTE: Regarding External Keyboard and Mouse:

This is an application matter resulting from the behavior of the external 8042 in the keyboard.

When the external keyboard and external mouse are powered up, the KDAT and MDAT lines are driven low. This sets the KBD bit (D3) and the MOUSE bit (D4) of the PME Wake Status Register since the KDAT and MDAT signals cannot be isolated internal to the part. This causes an nIO_PME_S3 and/or nIO_PME_S5 assertion to be generated if the keyboard and/or mouse PME events are enabled. Note that the keyboard and mouse isolation bits only prevent the internal 8042 in the part from setting these status bits.

Case 1: Keyboard and/or Mouse Powered by VTR

The KBD and/or MOUSE status bits will be set upon a VTR POR if the keyboard and/or mouse are powered by VTR.

In this case, a nIO_PME_S3 will not be generated, since the keyboard and mouse PME S3 enable bits are reset to zero on a VTR POR. The BIOS software needs to clear these PME status bits after power-up.

In this case, an nIO_PME_S5 will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are Bvat powered. Therefore, if the keyboard and mouse are powered by VTR, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VTR is removed (i.e., S4 or S5) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME and/or wake events from the power states S3 or below.

Case 2: Keyboard and/or Mouse Powered by VCC

The KBD and/or MOUSE status bits will be set upon a VCC POR if the keyboard and/or mouse are powered by VCC. In this case, a nIO_PME_S3 and a nIO_PME_S5 will be generated if the enable bits were set for wakeup, since the keyboard and mouse PME enable bits are VTR or Vbat powered. Therefore, if the keyboard and mouse are powered by VCC, the enable bits for keyboard and mouse events should be cleared prior to entering a sleep state where VCC is removed (i.e., S3) to prevent a false PME from being generated. In this case, the keyboard and mouse should only be used as PME

and/or wake events from the S0 and/or S1 states. The BIOS software needs to clear these PME status bits after power-up.

Chapter 13 General Purpose I/O (GPIO)

The SCH5017 provides a set of flexible Input/Output control functions to the system designer through the 25 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

13.1 GPIO Pins

The following pins include GPIO functionality. These pins are defined in the table below. All GPIOs default to the GPIO function except on indicated by [Note 13.2](#).

Table 13.1 GPIO Functionality

GPIO PIN		GPIO REGISTER								
	PIN NAME (DEFAULT FUNC/ ALTERNATE FUNCS)	P W R E L L	V T R P O R	REG OFFSET (HEX)	REG	P C I R E S E T	V C C P O R	VTR POR	SMI/PME	NOTE
1.	GP40/DRV DEN0	VCC	In	3B	GP40	-	-	0x01	-	
2.	KDAT/GP21	VCC	In	2C	GP21	-	-	0x0D	SMI/PME	13.1 , 13.2
3.	KCLK/GP22	VCC	In	2D	GP22	-	-	0x0D	SMI/PME	13.1 , 13.2 ,
4.	nIDE_RSTDRV/GP10	VCC	Out	23	GP10	-	-	0x02	PME	13.1 , 13.2
5.	nPCIRST_OUT1/GP11	VTR	Out	24	GP11	-	-	0x02	PME	13.2 13.3
6.	nPCIRST_OUT2/GP12	VTR	Out	25	GP12	-	-	0x02	PME	13.2 13.3
7.	nPCIRST_OUT3/GP13	VTR	Out	26	GP13	-	-	0x02	PME	13.2 13.3
8.	nPCIRST_OUT4/GP14	VTR	Out	27	GP14	-	-	0x82	PME	13.2 13.3
9.	GP42/nIO_PME_S3	VTR	Out	3D	GP42	-	-	0x01	SMI	
10.	nIO_PME_S5/GP43	VTR	Out	3E	GP43			0x84		13.2 13.3 , 13.4
11.	GP60/nLED1/WDT	VTR	In	47	GP60	-	-	0x01	SMI/PME	13.1
12.	GP61/nLED2#	VTR	In	48	GP61	-	-	0x01	SMI/PME	13.1
13.	GP27/nIO_SMI /P17	VCC	In	32	GP27	-	-	0x01	nIO_SMI/ PME	13.1
14.	MDAT/GP32	VCC	In	35	GP32	-	-	0x05	SMI/PME	13.1 13.2

Table 13.1 GPIO Functionality (continued)

GPIO PIN		GPIO REGISTER								
	PIN NAME (DEFAULT FUNC/ ALTERNATE FUNCS)	P W R E L L	V T R P O R	REG OFFSET (HEX)	REG	P C I R E S E T	V C C P O R	VTR POR	SMI/PME	NOTE
15.	MCLK/GP33	VCC	In	36	GP33	-	-	0x05	SMI/PME	13.1 13.2
16.	GP36/nKBDRST	VCC	In	39	GP36	-	-	0x01	-	
17.	GP37/A20M	VCC	In	3A	GP37	-	-	0x01	-	
18.	GP50/nRI2	VCC	In	3F	GP50	-	-	0x01	PME	13.1
19.	GP51/nDCD2	VCC	In	40	GP51	-	-	0x01	PME	13.1
20.	GP52/RXD2 (IRRX)	VCC	In	41	GP52	-	-	0x01	PME	13.1
21.	GP53/TXD2 (IRTX)	VCC	In	42	GP53	-	-	0x01	PME	13.1
22.	GP54/nDSR2	VCC	In	43	GP54	-	-	0x01	SMI/PME	13.1
23.	GP55/nRTS2	VCC	In	44	GP55	-	-	0x01	SMI/PME	13.1
24.	GP56/nCTS2	VCC	In	45	GP56	-	-	0x01	SMI/PME	13.1
25.	GP57/nDTR2	VCC	In	46	GP57	-	-	0x01	SMI/PME	13.1

Note 13.1 These pins are inputs to VCC and VTR powered logic.

Note 13.2 This pin's primary function (power up default function) is not GPIO function; however, the pin can be configured a GPIO Alternate function.

Note 13.3 This is only an output and can not be configured as an input

Note 13.4 This pin, defaults to nIO_PME_S5 pin function active low, open-drain output at Vbat POR and retains its setting through all other POR's. The output buffer is not driven until VTR is present.

Note 13.5 The GPIO Data and Configuration Registers are located in PME block at the offset shown from the PME_BLK address. See [Chapter 28, "Runtime Registers," on page 271](#) for detailed register description.

13.2 Description

Each GPIO port has a 1-bit data register and an 8-bit configuration control register. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP6. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. All of the GPIO registers are located in the PME block see [Chapter 28, Runtime Registers](#). The GPIO ports with their alternate functions and configuration state register addresses are listed in [Table 13.2](#).

Table 13.2 General Purpose I/O Port Assignments

DEFAULT FUNCTION	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	DATA REGISTER (SEE Note 13.5)	DATA REGISTER BIT NO.
nIDE_RSTDRV	GPIO			GP1 OFFSET 4B	0
nPCIRST_OUT1	GPIO				1
nPCIRST_OUT2	GPIO				2
nPCIRST_OUT3	GPIO				3
nPCIRST_OUT4	GPIO				4
Reserved					5
Reserved					6
Reserved					7
Reserved				GP2 OFFSET 4C	0
KDAT (See Note 13.6)	GPIO				1
KCLK (See Note 13.6)	GPIO				2
Reserved					4:3
Reserved					5
Reserved					6
GPIO	SMI Output	P17 (See Note 13.6)			7
Reserved				GP3 OFFSET 4D	0
Reserved					1
MDAT (See Note 13.6)	GPIO				2
MCLK (See Note 13.6)	GPIO				3
Reserved					4
Reserved					5
GPIO	Keyboard Reset				6
GPIO	Gate A20				7

Table 13.2 General Purpose I/O Port Assignments (continued)

DEFAULT FUNCTION	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	DATA REGISTER (SEE Note 13.5)	DATA REGISTER BIT NO.
GPIO	Drive Density Select 0			GP4 OFFSET 4E	0
Reserved					1
GPIO	nIO_PME_S3				2
nIO_PME_S5	GPIO				3
Reserved					4:7
GPIO	Ring Indicator 2			GP5 OFFSET 4F	0
GPIO	Data Carrier Detect 2				1
GPIO	Receive Serial Data 2				2
GPIO	Transmit Serial Data 2				3
GPIO	Data Set Ready 2				4
GPIO	Request to Send 2				5
GPIO	Clear to Send 2				6
GPIO	Date Terminal Ready				7
GPIO Note 13.7	nLED1	WDT	WDT	GP6 OFFSET 50	0
GPIO Note 13.7	nLED2				1
Reserved					7:2

Note 13.6 When this pin function is selected, the associated GPIO pins have bi-directional functionality.

Note 13.7 These pins have Either Edge Triggered Interrupt (EETI) functionality. See [Section 13.5](#), "GPIO PME and SMI Functionality," on page 142 for more details.

13.3 GPIO Control

Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in [Chapter 28, Runtime Registers](#) section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. Bit[0] of each GPIO Configuration Register determines the port direction, bit[1] determines the signal polarity, and bit[7] determines the output driver type select. The GPIO configuration register Output Type select bit[7] applies to GPIO functions and the nSMI Alternate functions

The basic GPIO configuration options are summarized in .

Table 13.3 GPIO Configuration Option

SELECTED FUNCTION	DIRECTION BIT	POLARITY BIT	DESCRIPTION
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

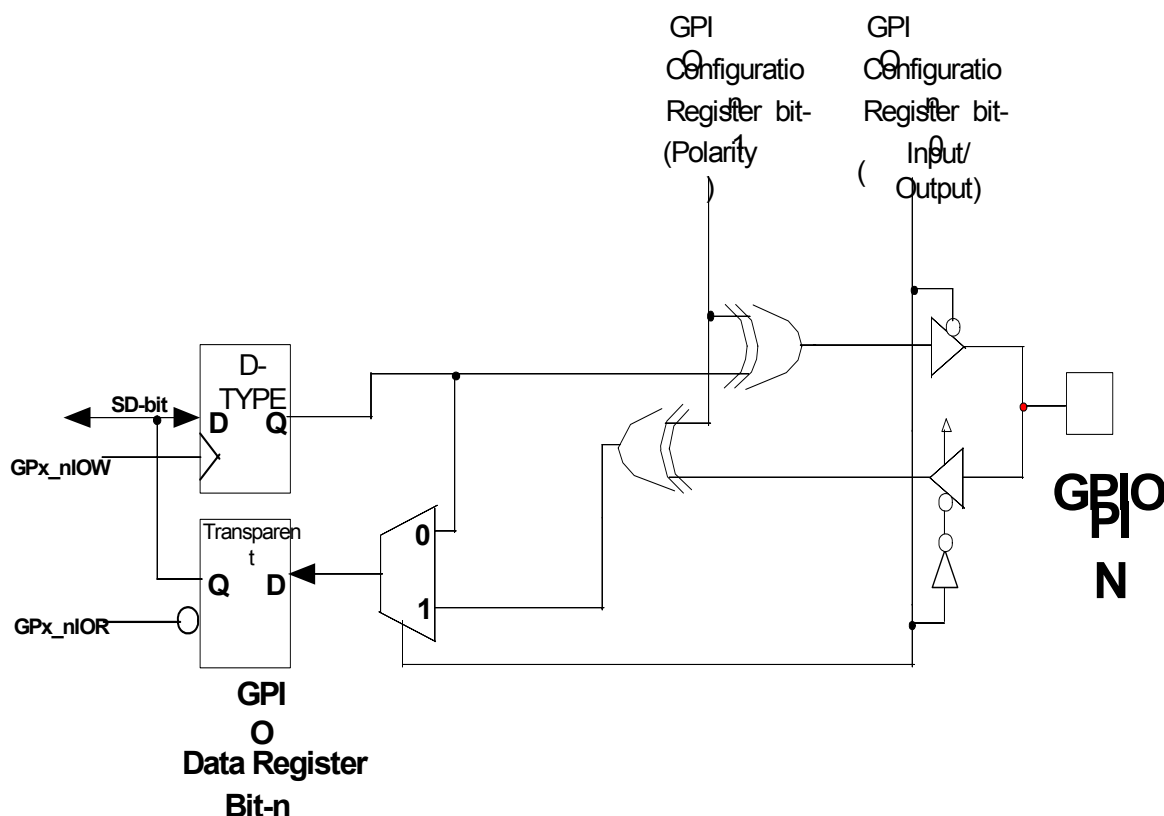
The following GPIO have limited functionality as indicated in the notes in [Table 13.1, "GPIO Functionality," on page 137](#): GP10, GP11, GP12, GP13, GP14, GP42, GP43. The corresponding GPIO Control Register have read only bits in position 0, 1, and/or 7.

13.4 GPIO Operation

The operation of the GPIO ports is illustrated in [Figure 13.1](#).

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect ([Table 13.4](#))

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register ([Table 13.4](#)). When the GPIO is programmed as an output, the pin is excluded from the PME and SMI logic.


Figure 13.1 GPIO Function Illustration

Note: Figure 13.1 is for illustration purposes only and is not intended to suggest specific implementation details.

Table 13.4 GPIO Read/Write Behavior

HOST OPERATION	GPIO INPUT PORT	GPIO OUTPUT PORT
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

13.5 GPIO PME and SMI Functionality

The SCH5017 provides GPIOs that can directly generate a PME. The polarity bit in the GPIO control registers select the edge on these GPIO pins that will set the associated status bit in a PME Status. For additional description of PME behavior see [Chapter 15, "PME Support," on page 147](#). The default is the low-to-high transition. In addition, the SCH5017 provides GPIOs that can directly generate an SMI.

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP21-GP22, GP27, GP32-GP33 are controlled by [PMES3_STS3](#), [PMES5_STS3](#), [PMES3_EN3](#), and [PMES5_EN3](#) registers.

GP50-GP57 are controlled by [PMES3_STS5](#), [PMES5_STS5](#), [PMES3_EN5](#), and [PMES5_EN5](#) registers.

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GP60, GP61 are controlled by [PMES3_STS6](#), [PMES5_STS6](#), [PMES3_EN6](#), and [PMES5_EN6](#) registers.

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP21, GP22, GP54, GP55, GP56, GP57, GP60 are controlled by [SMI_STS3](#), and [SMI_EN3](#) registers.

GP32, GP33, GP42, GP61 are controlled by [SMI_STS4](#), and [SMI_EN4](#) registers.

The following GPIOs have "either edge triggered interrupt" (EETI) input capability: GP22, GP60, GP61. These GPIOs can generate a PME and an SMI on both a high-to-low and a low-to-high edge on the GPIO pin. These GPIOs have a status bit in the [MSC_STS](#) status register that is set on both edges. The corresponding bits in the PME and SMI status registers are also set on both edges.

13.6 Either Edge Triggered Interrupts

Three GPIO pins are implemented such that they allow an interrupt (PME or SMI) to be generated on both a high-to-low and a low-to-high edge transition, instead of one or the other as selected by the polarity bit.

The either edge triggered interrupts (EETI) function as follows: If the EETI function is selected for the GPIO pin, then the bits that control input/output, polarity and open drain/push-pull have no effect on the function of the pin. However, the polarity bit does affect the value of the GP bit (i.e., register [GP2](#), bit 2 for GP22).

A PME or SMI interrupt occurs if the PME or SMI enable bit is set for the corresponding GPIO and the EETI function is selected on the GPIO. The PME or SMI status bits are set when the EETI pin transitions (on either edge) and are cleared on a write of '1'. There are also status bits for the EETIs located in the [MSC_STS](#) register, which are also cleared on a write of '1'. The [MSC_STS](#) register provides the status of all of the EETI interrupts within one register. The PME, SMI or MSC status is valid whether or not the interrupt is enabled and whether or not the EETI function is selected for the pin.

Miscellaneous Status Register ([MSC_STS](#)) is for the either edge triggered interrupt status bits. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding MSC status bits. Status bits are cleared on a write of '1'. See [Chapter 28, "Runtime Registers," on page 271](#) for more information.

The configuration register for the either edge triggered interrupt status bits is defined in [Chapter 28, Runtime Registers](#).

13.7 LED Functionality

The SCH5017 provides LED functionality on two GPIOs, GP60 and GP61. These pins can be configured to turn the LED on and off and blink independent of each other through the LED1 and LED2 runtime registers at offset 0x5D and 0x5E from the base address located in the primary base I/O address in Logical Device A.

The LED pins (GP60 and GP61) are able to control the LED while the part is under VTR power with VCC removed. In order to control a LED while the part is under VTR power, the GPIO pin must be configured for the LED function and either open drain or push-pull buffer type. In the case of open-drain buffer type, the pin is capable of sinking current to control the LED. In the case of push-pull buffer type, the part will source current. The part is also able to blink the LED under VTR power. The LED will not blink under VTR power (VCC removed) if the external 32KHz clock is not connected.

The LED pins can drive a LED when the buffer type is configured to be push-pull and the part is powered by either VCC or VTR, since the buffers for these pins are powered by VTR. This means they will source their specified current from VTR even when VCC is present.

The LED control registers are defined in [Chapter 28, Runtime Registers](#).



Chapter 14 System Management Interrupt (SMI)

The SCH5017 implements a “group” nIO_SMI output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from each of the functional blocks in the chip and many of the GPIOs and the Fan tachometer pins. The GP27/nIO_SMI/P17 pin, when selected for the nIO_SMI function, can be programmed to be active high or active low via the polarity bit in the GP27 register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the GP27 register. The nIO_SMI pin function defaults to active low, open-drain output.

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1 to 4. The nSMI output is then enabled onto the group nIO_SMI output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2. The internal SMI can also be enabled onto the nIO_PME_S3 pin. Bit[5] of the SMI Enable Register 2 ([SMI_EN2](#)) is used to enable the SMI output onto the nIO_PME_S3 pin (GP42). This bit will enable the internal SMI output into the PME logic through the DEVINT_STS bit in [PMES3_STS3](#). See [Chapter 15, "PME Support," on page 147](#) for more details.

An example logic equation for the nSMI output for SMI registers 1 and 2 is as follows:

$$\text{nSMI} = (\text{EN_PINT and IRQ_PINT}) \text{ or } (\text{EN_U2INT and IRQ_U2INT}) \text{ or } (\text{EN_U1INT and IRQ_U1INT}) \text{ or } (\text{EN_FINT and IRQ_FINT}) \text{ or } (\text{EN_MINT and IRQ_MINT}) \text{ or } (\text{EN_KINT and IRQ_KINT}) \text{ or } (\text{EN_IRINT and IRQ_IRINT}) \text{ or } (\text{ENP12 and IRQ_P12}) \text{ or } (\text{SPEMSE_EN and SPEMSE_STS})$$

Note: The prefixes EN and IRQ are used above to indicate SMI enable bit and SMI status bit respectively.

SMI Registers

The SMI event bits for the GPIOs and the Fan tachometer events are located in the SMI status and Enable registers 3-5. The polarity of the edge used to set the status bit and generate an SMI is controlled by the polarity bit of the control registers. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding SMI status bit. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for these events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI registers are accessed at an offset from PME_BLK (see [Chapter 28, "Runtime Registers," on page 271](#) for more information).

The SMI event bits for the super I/O devices are located in the SMI status and enable register 1 and 2. All of these status bits are cleared at the source except for IRINT, which is cleared by a read of the SMI_STS2 register; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See [Chapter 28, "Runtime Registers," on page 271](#) for the definition of these registers.



Chapter 15 PME Support

The SCH5017 offers support for power management events (PMEs), also referred to as a System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the nIO_PME_S3 signal when in S3 power state or below and nIO_PME_S5 signal in S4 or S5 power states.

APPLICATION NOTE: Software must properly configure the enable and status bits for the individual PME events in the registers described below. There is no hardware power states interpretation and nIO_PME_S3 and nIO_PME_S5 pin configuration.

Table 15.1 describes the PME interface.

Table 15.1 PME Interface

NAME	BUFFER	POWER WELL	DESCRIPTION
nIO_PME_S3	(O12/OD12)	VTR	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wakeup in S3 and below.
nIO_PME_S5	(O12/OD12)	VTR	General Purpose I/O. Power Management Event Output. This active low Power Management Event signal allows this device to request wakeup in S4 or S5.

15.1 PME Events

All PME the events asserted on nIO_PME_S3 and nIO_PME_S5 are listed in Table 15.2.

Table 15.2 PME Events

EVENTS	PME_S3	PME_S5	COMMENT
Mouse			
by IRQ	Y (from group SMI)	N	
DATA pin edge sensitive	Y	Y	
Specific Mouse Click	Y	Y	See Section 15.5, "Wake on Specific Mouse Click," on page 150 for details
Keyboard			
Any Key	Y	Y	
Specific Key	Y	Y (default enabled)	
by IRQ	Y (from group SMI)	N	
Power button input		Y (default enabled)	
Last state before Power Loss	Y	Y (default enabled)	
FDC	Y (from group SMI)	N	

Table 15.2 PME Events (continued)

EVENTS	PME_S3	PME_S5	COMMENT
PIO	Y (from group SMI)	N	
UART-A			
by IRQ	Y (from group SMI)	N	
by nRI1 pin	Y	Y	
UART-B			
by IRQ	Y (from group SMI)	N	
by nRI2 pin	Y	Y	
Hardware Monitor	nHWM_INT		
Watch Dog Timer	Y		
GPIO, total 25 pins	Y		
Low-Battery	Y	N	Detect on VCC POR only not a S3 wakeup either
Intrusion	Y	Y	

The PME function is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in configuration registers 0x60 and 0x61 in Logical

There are four types of registers which control PME_S3 events:

1. PME Wake Status register ([PMES3_STS1](#), [PMES3_STS3](#), [PMES3_STS5](#), [PMES3_STS6](#).) provides the status of individual wake events.
2. PME Wake Enable ([PMES3_EN1](#), [PMES3_EN3](#), [PMES3_EN5](#), [PMES3_EN6](#)) provides the enable for individual wake events.
3. PME Pin Enable Register ([PME_S3_EN](#).) provides an enable for the PME output pins.
4. PME Pin Status Register ([PME_S3_STS](#)) provides the status for the PME output pins.

Similarly, there are four types of registers which control PME_S5 events:

1. PME Wake Status register ([PMES5_STS1](#), [PMES5_STS3](#), [PMES5_STS5](#), [PMES5_STS6](#)) provides the status of individual wake events.
2. PME Wake Enable([PMES5_EN1](#), [PMES5_EN3](#), [PMES5_EN5](#), [PMES5_STS6](#)) provides the enable for individual wake events.
3. PME Pin Enable Register ([PME_S5_EN](#).) provides an enable for the PME output pins.
4. PME Pin Status Register ([PME_S5_STS](#)) provides the status for the PME output pins.

See [Chapter 28, "Runtime Registers," on page 271](#) for detailed register description

The following describes the behavior to the PME status bits for each event:

Each wake source has a bit in a PME Wake Status register which indicates that a wake source has occurred. The PME Wake Status bits are "sticky"(unless otherwise stated in bit description in [Section 28.2, "Runtime Register Description," on page 276](#)): once a status bit is set by the wake-up event, the bit will remains set until cleared by writing a '1' to the bit.

Each PME Wake Status register has a corresponding PME Wake Enable Register.

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If the corresponding bit in both in a PME Wake Status register and the PME Wake Enable Register are set then the PME Pin Status Register bit is set. If both corresponding PME Pin Status and the PME Pin Enable Register bit are set then the IO_PME_S3 or IO_PME_S5 pin will asserted.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the polarity bit of the GPIO control register. For non-inverted polarity (default) the status bit is set on the low-to-high edge. If the EETI function is selected for a GPIO then both a high-to-low and a low-to-high edge will set the corresponding PME status bits. Status bits are cleared on a write of '1'.

The PME Wake registers also include status and enable bits for the HW Monitor Block.

See [Section 12.0.9, "Keyboard and Mouse PME Generation," on page 134](#) for information about using the keyboard and mouse signals to generate a PME.

15.2 Enabling SMI Events onto the PME Pin

There is a bit in the PME Status Register 3 to show the status of the internal "group" SMI signal in the PME logic (if bit 5 of the SMI_EN2 register is set). This bit, DEVINT_STS, is at bit 3 of the PME_STS3 register. When this bit is clear, the group SMI output is inactive. When bit is set, the group SMI output is active. The corresponding Wake-up enable bit is DEVINT_EN, is at bit 3 of the PME_EN3 register.

Bit 5 of the SMI_EN2 register must also be set. This bit is cleared on a write of '1'.

15.3 PME Function Pin Control

The GP42/nIO_PME_S3 pin, when selected for the nIO_PME_S3 function, can be programmed to be active high or active low via the polarity bit in the [GP42](#) register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the [GP42](#) register. The nIO_PME_S3 pin function defaults to active low, open-drain output; however the GP42/nIO_PME_S3 pin defaults to the GP42 function.

The nIO_PME_S5/GP43 pin, when selected for the nIO_PME_S5 function, can be programmed to be active high or active low via the polarity bit in the [GP43](#) register. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 of the [GP43](#) register. The [GP43](#) register defaults on Vbat POR and retains its setting through all other POR's. The nIO_PME_S5/GP43 pin defaults to the nIO_PME_S5 pin function active low, open-drain output.

In the SCH5017 the nIO_PME_S3 and nIO_PME_S5 pins can be programmed to be an open drain, active low, driver. The SCH5017 nIO_PME_S3 and nIO_PME_S5 pins are fully isolated from other external devices that might pull the signal low; i.e., the nIO_PME_S3 and nIO_PME_S5 pins are capable of being driven high externally by another active device or pull-up even when the SCH5017 VCC is grounded, providing VTR power is active. The SCH5017 nIO_PME_S3 and nIO_PME_S5 pin driver sinks 6mA at 0.55V max (see section 4.2.1.1 DC Specifications in the PCI Local Bus Specification, Revision 2.2, December 18, 1998).

15.4 Wake on Specific Key Code

The SCH5017 Wake on Specific Key Code feature is enabled for the assertion of the nIO_PME_S5 signal in S4 or S5 power states by the SPEKEY bit in the [PMES5_EN6](#) register. This bit defaults to enabled and is Vbat powered.

At Vbat POR the Wake on Specific Key Code feature is disabled. During the first VTR POR and VCC POR the Wake on Specific Key Code feature remains disabled. Software selects the precise Specific Key Code event (configuration) to wake the system and then enables the feature via the SPEKEY bit in the [PMES5_STS6](#) register. The system then may go the sleep and/or have a power failure. After returning to or remaining in S5 sleep, the system will fully awake by a Wake on Specific Key Code. The Specific Key Code configuration and the enable for the nIO_PME_S5 are retained via Vbat backed registers.

The SCH5017 Wake on Specific Key Code feature is enabled for assertion of the nIO_PME_S3 signal when in S3 power state or below by the SPEKEY bit in the [PMES3_EN6](#) register. This bit defaults to disabled and is VTR powered.

15.5 Wake on Specific Mouse Click

The SPESME SELECT field in the [Mouse_Specific_Wake](#) Register selects which mouse event is routed to the [PMES3_STS6](#) and [PMES5_STS6](#) if enabled by [PMES3_EN6](#) and/or [PMES5_EN6](#). The KB_MSE_SWAP bit in the [Mouse_Specific_Wake](#) Register can swap the Mouse port and Keyboard interfaces internally.

The Lock bit in the [Mouse_Specific_Wake](#) Register provides a means of changing access to read only to prevent tampering with the Wake on Mouse settings. The other bits in the [Mouse_Specific_Wake](#) Register are VBAT powered and reset on VBAT POR; therefore, the mouse event settings are maintained through a power failure. The lock bit also controls access to the [DBLCLICK](#) Register.

The [DBLCLICK](#) register contains a numeric value that determines the time interval used to check for a double mouse click. The value is the time interval between mouse clicks. For example, if [DBLCLICK](#) is set to 0.5 seconds, you have one half second to click twice for a double-click.

The larger the value in the [DBLCLICK](#) Register, the longer you can wait between the first and second click for the SCH5017 to interpret the two clicks as a double-click mouse wake event. If the [DBLCLICK](#) value is set to a very small value, even quick double clicks may be interpreted as two single clicks.

The [DBLCLICK](#) register has a six bit weighted sum value from 0 to 0x3Fh which provides a double click interval between 0.0859375 and 5.5 seconds. Each incremental digit has a weight of 0.0859375 seconds.

The [DBLCLICK](#) Register is VBAT powered and reset on VBAT POR; therefore, the double click setting is maintained through a power failure. The default setting provides a 1.03125 second time interval.

[DBLCLICK](#) Writing to the [DBLCLICK](#) register shall reset the Mouse Wake-up internal logic and initialize the Mouse Wake-up state machines. The SPEMSE_EN bit in of the [CLOCKI32](#) configuration register at 0xF0 in Logical Device A is used to control the "Wake on Specific Mouse Click" feature. This bit is used to turn the logic for this feature on and off. It will disable the 32KHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:

0= "Wake on Specific Mouse Click" logic is on (default)

1= "Wake on Specific Mouse Click" logic is off

The generation of a PME for this event is controlled by the PME enable bits (SPEMSE_EN bit in the [PMES3_EN6](#) register and SPEMSE_EN in the [PMES5_EN6](#) register, and in the [SMI_EN2](#) register) when the logic for feature is turned on. See [Section 18.6, "Wake on Specific Mouse Event," on page 172](#).

APPLICATION NOTE: The Wake on Specific Mouse Click feature requires use of the M_ISO bit in the KRST_GA20 register. SMSC Application Note 8.8 titled "Keyboard and Mouse Wake-up Functionality".

When using the wake on specific mouse event, it may be necessary to isolate the Mouse Port signals (MCLK, MDAT) from the 8042 prior to entering certain system sleep states. This is due to the fact that the normal operation of the 8042 can prevent the system from entering a sleep state or trigger false PME events. SCH5017 has an "isolation" bit for the mouse signals, which allows the mouse data signals to go into the wake-up logic but block the clock and data signals from the 8042.

When the mouse isolation bit are used, it may be necessary to reset the 8042 upon exiting the sleep state. If M_SIO bit is set prior to entering a sleep state where VCC goes inactive (S3-S5), then the 8042 must be reset upon exiting the sleep mode. Write 0x40 to global configuration register 0x2C to reset the 8042. The 8042 must then be taken out of reset by writing 0x00 to register 0x2C since the bit that resets the 8042 is not self-clearing. Caution: Bit 6 of configuration register 0x2C is used to put the 8042 into reset - do not set any of the other bits in register 0x2C, as this may produce undesired results.

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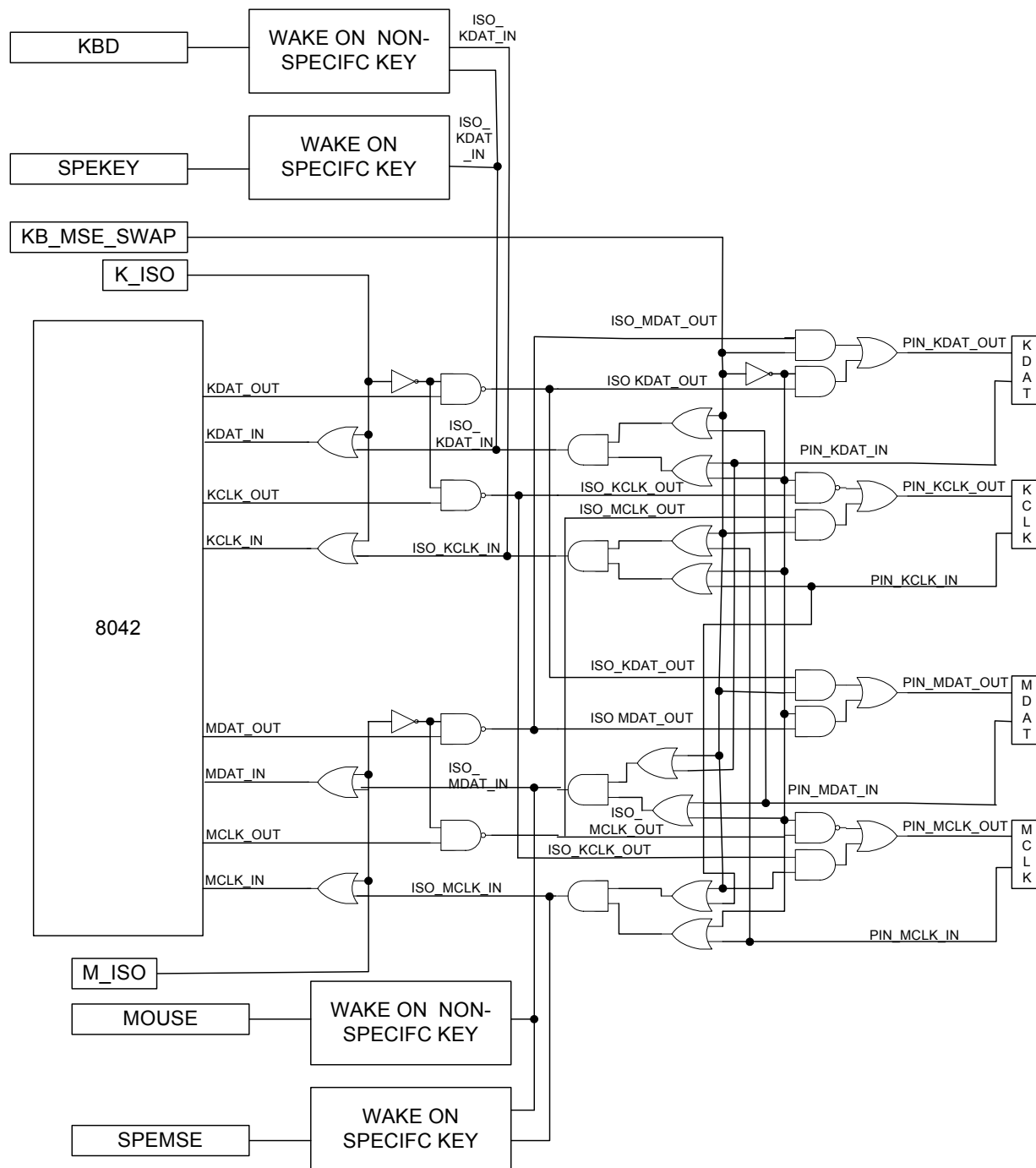


Figure 15.1 8042 Isolation and Keyboard and Mouse Port Swap Representation

Note: This figure is for illustration purposes only and not meant to imply specific implementation details



Chapter 16 Watchdog Timer

The SCH5017 contains a Watchdog Timer (WDT). The Watchdog Time-out status bit may be mapped to an interrupt through the WDT_CFG Runtime Register.

The SCH5017's WDT has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 seconds with 1 second resolution. The units of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register. The WDT time-out value is set through the WDT_VAL Runtime register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Runtime register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

Two system events can reset the WDT: a Keyboard Interrupt or a Mouse Interrupt. The effect on the WDT for each of these system events may be individually enabled or disabled through bits in the WDT_CFG Runtime register. When a system event is enabled through the WDT_CFG register, the occurrence of that event will cause the WDT to reload the value stored in WDT_VAL and reset the WDT time-out status bit if set. If both system events are disabled, the WDT_VAL register is not re-loaded.

The Watchdog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. The WDT interrupt is mapped to an interrupt channel through the WDT_CFG Runtime register. When mapped to an interrupt the interrupt request pin reflects the value of the WDT time-out status bit.

The host may force a Watchdog time-out to occur by writing a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Runtime register. Writing a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watchdog Status). Bit 2 of the WDT_CTRL is self-clearing.

- See [Chapter 28, "Runtime Registers," on page 271](#) for description of these registers.



Chapter 17 Buffered PCI Outputs

17.1 Buffered PCI Outputs Interface

SCH5017 provides four software controlled PCIRST# outputs and one buffered IDE Reset.

Table 17.1 describes the interface.

Table 17.1 Buffered PCI outputs Interface

NAME	BUFFER	POWER WELL	DESCRIPTION
PCI_RESET#	PCI_I	VCC	PCI Reset Input
nIDE_RSTDRV	OD8	VCC	IDE Reset Output
nPCIRST_OUT1	OP14	VTR	Buffered PCI Reset Output
nPCIRST_OUT2	OP14	VTR	Buffered PCI Reset Output
nPCIRST_OUT3	OP14	VTR	Buffered PCI Reset Output
nPCIRST_OUT4	OD14	VTR	Buffered PCI Reset Output

17.1.1 IDE Reset Output

nIDE_RST is an open drain buffered copy of PCI_RESET#. This signal requires an external 1K Ω pull-up to VCC or 5V. This pin is an output only pin which floats when VCC=0. The pin function's default state on VTR POR is the nIDE_RST function; however the pin function can be programmed to the a GPO pin function by bit 2 in the GP10 GPIO control register.

The nIDE_RST output has a programmable forced reset. The software control of the programmable forced reset function is located in the GP1 GPIO Data register. When the GP10 bit (bit 0) is set, the nIDE_RST output follows the PCI_RESET# input; this is the default state on VTR POR. When the GP10 bit is cleared, the nIDE_RST output stays low.

See GP10 and GP1 for Runtime Register Description (Table 28.2 on page 276).

Table 17.2 nIDE_RSTDRV Truth Table

PCI_RESET# (INPUT)	nIDE_RSTDRV (OUTPUT)
0	0
1	Hi-Z

Table 17.3 nIDE_RSTDRV Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
Tf	nIDE_RSTDRV high to low fall time. Measured from 90% to 10%			15	ns
Tpropf	nIDE_RSTDRV high to low propagation time. Measured from PCI_RESET# to nIDE_RSTDRV.			22	ns

Table 17.3 nIDE_RSTDRV Timing (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
CO	Output Capacitance			25	pF
CL	Load Capacitance			40	pF

17.1.2 nPCIRST_OUT Output Logic

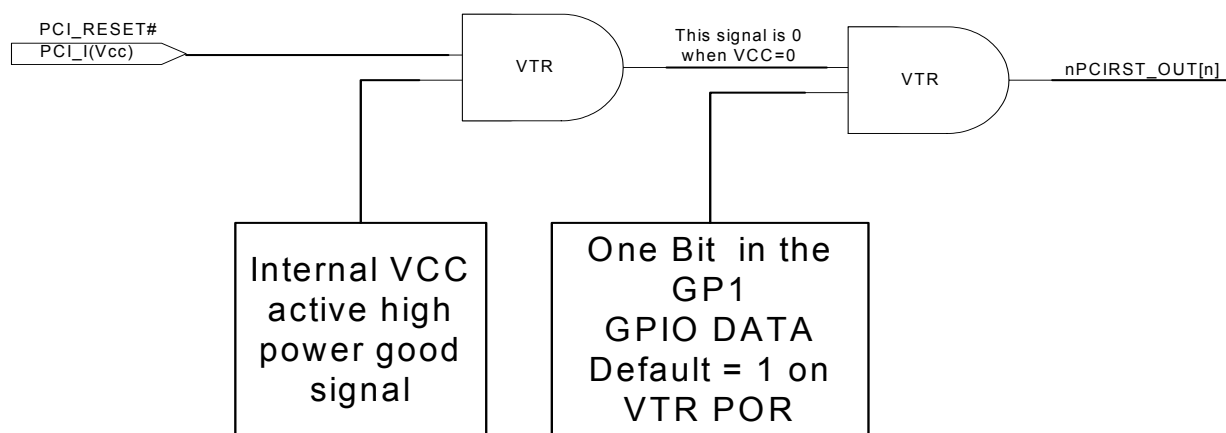
The nPCIRST_OUT1, nPCIRST_OUT2, and nPCIRST_OUT3 outputs are 3.3V balance buffer push-pull buffered copies of PCI_RESET# input. The nPCIRST_OUT4 output is 3.3V open drain buffered copy of PCI_RESET# input. Each pin function's default state on VTR POR is the nPCIRST_OUT function; however, the pin function can be programmed to the a GPO pin (output only) function by bit 2 in the corresponding GPIO control register (GP11. GP12, GP13 GP14).

Each nPCIRST_OUT[n] output has a programmable force reset. The software control of the programmable forced reset function is located in the GP1 GPIO Data register. When the corresponding (GP11. GP12, GP13 GP14) bit in the GP1 GPIO Data register is set, the nPCIRST_OUT[n] output follows the PCI_RESET# input; this is the default state on VTR POR. When the corresponding (GP11. GP12, GP13 GP14) bit in the GP1 GPIO Data register is cleared, the nPCIRST_OUT[n] output stays low.

See GP11. GP12, GP13 GP14 on page 285 and GP1 on page 291 for Runtime Register Description.

When the VTR power is applied, VCC is powered down, and the GPIO control register's contents are default, the nPCIRST_OUT[n] pin output is low.

The Figure 17.1 illustrates the nPCIRST_OUT[n] function. The figure is for illustration purposes only and in not intended to suggest specific implementation details.



Note: This figure is for illustration purposes only and not meant to imply specific implementation details

Figure 17.1 Figure 2 - nPCIRST_OUT[n] Logic

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Chapter 18 Power Control Features

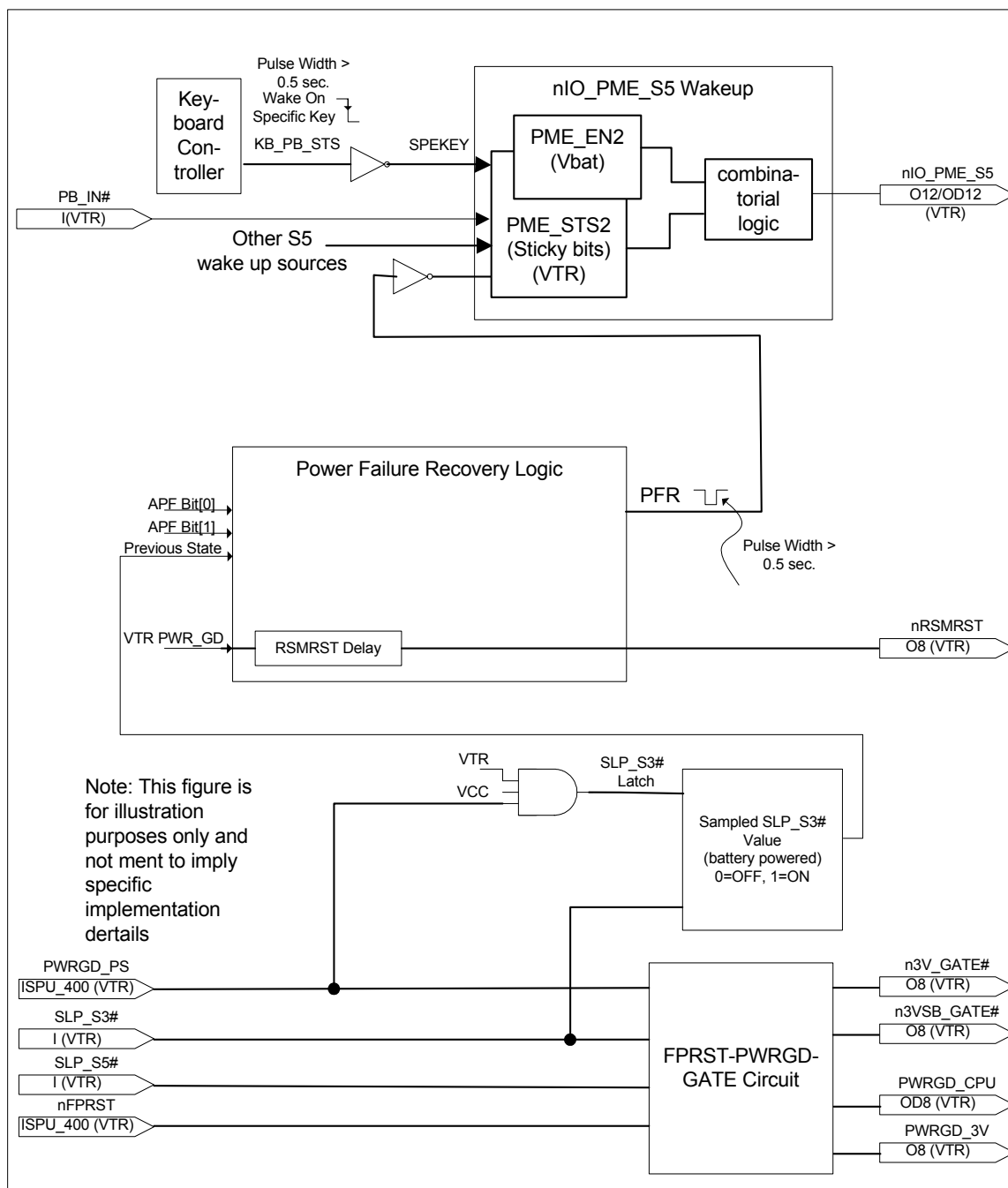
Table 18.1 and Figure 18.1 describe the interface and connectivity of the following Power Control Features:

1. Front Panel Reset with Input Debounce, Power Supply Gate, and CPU Powergood Signal Generation
2. AC Recovery Circuit with nRSMRST generation
3. Keyboard Wake on Mouse.
4. S5 PME wakeup

Table 18.1 Power Control Interface

NAME	DIRECTION	DESCRIPTION
nRSMRST	Output	Resume Reset Output (See Note 18.1.)
PWRGD_PS	Input	Power Good Input from Power Supply
nFPRST	Input	Reset Input from Front Panel
SLP_S3#	Input	From south bridge
SLP_S5#	Input	From south bridge
PWRGD_CPU	Output	Power Good Output – Open Drain
PWRGD_3V	Output	Power Good Output – Push Pull
n3V_GATE	Output	PS Control
n3VSB_GATE	Output	PS Control
nIO_PME_S5	Output	Power Management Event Output signal allows this device to request wakeup in S4 or S5.

Note 18.1 This pin maintains a logic low level of 0.5V or less at 5mA while the VTR is 0V and the VTR powered functional logic is disabled. This operation requires Vbat is present. When VTR is applied, the VTR powered functional logic determines the state of the pin.


Figure 18.1 Power Control Block Diagram

18.1 nIO_PME_S5 Pin use in Power Control

The nIO_PME_S5 signal is used to control the state of the power supply. The nIO_PME_S5 signal will be asserted when a PME event occurs and the PME logic is enabled. The following is a summary of the Power control S5 PME events (See [Figure 18.1](#)):

1. PB_IN# input signal assertion.
2. When the Wake On Specific Key Logic detects the programmed keyboard event it will generate a wake event (KB_PB_STS).

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3. Upon returning from a power failure and the power supply needs to be turned on.

Each PME wake event sets a status bit in the [PMES5_STS6](#) register. If the corresponding enable bit in the [PMES5_EN6](#) register is set then the nIO_PME_S5 pin will be asserted. The enable bits in the [PMES5_EN6](#) register default to set and are Vbat powered. [Chapter 15, PME Support](#) for description of the PME support for this PME event.

18.2 Front Panel Reset, Power Supply Gates & CPU Powergood Generation

[Figure 18.2](#) illustrates the Front Panel Reset Input Debounce and n3V_GATE, n3VSB_GATE & Powergood Signal Generation (FPRST-PWRGD-GATE) interface and circuit.

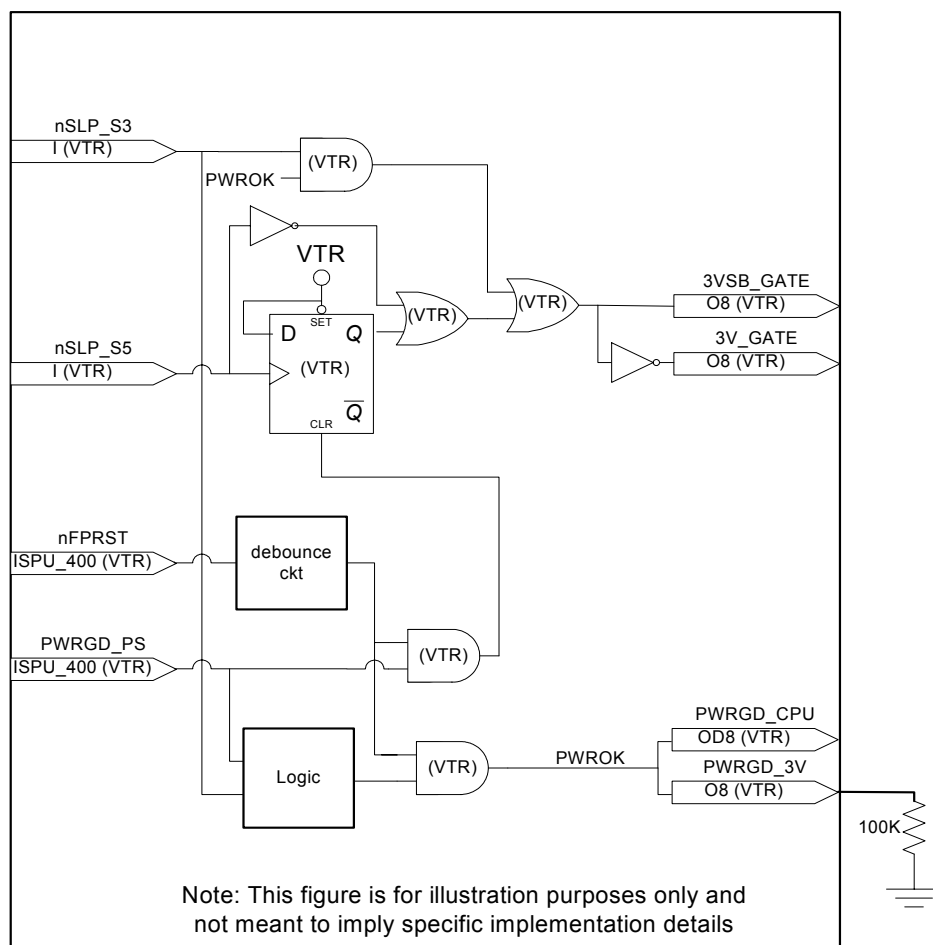


Figure 18.2 FPRST-PWRGD-GATE Circuit

18.2.1 FPRST Debounce

The nFPRST input has internal debounce circuitry that is valid on both edges for at least 16ms before the output is changed. The 32.768kHz is used to meet the timing requirement. See [Figure 18.3](#) for nFPRST debounce timing.

Note: The actual minimum debounce time is 15.8msec

The 32.768 kHz trickle input **must** be connected to supply the clock signal for the nFPRST debounce circuitry. SCH5017 has a legacy feature which is incompatible with use of the nFPRST input signal.

An internal 32kHz clock source derived from the 14MHz (VCC powered) can be selected when the external 32kHz clock is not connected.

APPLICATION NOTE: The 32.768 kHz trickle input must be connected to supply the clock signal for the nFPRST debounce circuitry.

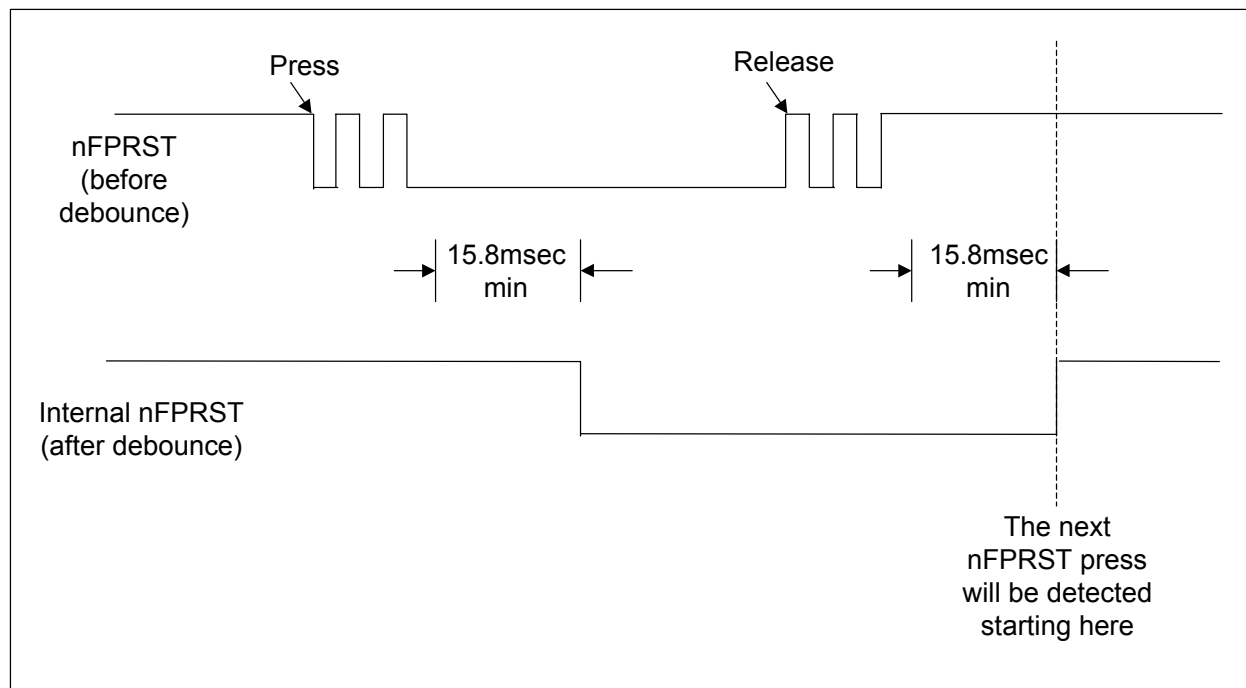


Figure 18.3 nFPRST Debounce Timing

18.2.2 Powergood Generation

The PWRGD_3V signal is a function of PWRGD_PS, nSLP_S3 and nFPRST.

The inputs, PWRGD_PS and nFPRST have hysteresis and are internally pulled to VTR through a 30uA resistor. The nFPRST is debounced internally.

The following description applies to the PWRGD_3V signal and the PWRGD_CPU signal. An optional delay is provided for power sequencing control.

The assertion and de-assertion edge is described below, and is summarized in [Table 18.2, "PWRGD_3V Truth Table"](#).

- **Negative edge (S0->S3/S5):** The 1-0 transition of nSLP_S3 input or the 1-0 transition (or 0 level) of PWRGD_PS input will cause an immediate 1-0 transition (or 0 level) of PWRGD_3V.
- **Positive edge (S3/S5->S0):** The 0-1 transition of PWRGD_PS input would cause a 0-1 transition of PWRGD_3V. The PWRGD_3V transition is either immediate (no delay) or after a 100ms (min.) to 120ms (max) delay from the 0-1 transition of PWRGD_PS.

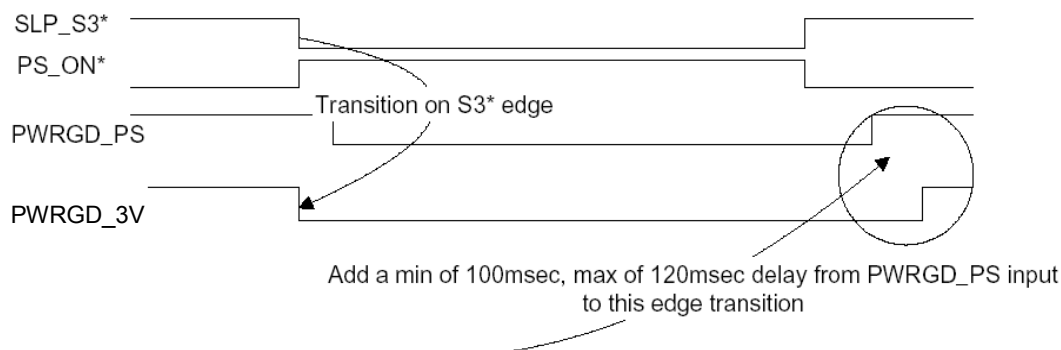
The delay is optional and is controlled by a lockable select bit in the SMB_ISO register (located at offset 6Ah in the Runtime Register Block). Default operation selects the delay. An internal delay counter is used to determine whether the 100-120 msec delay time has elapsed.

Table 18.2 PWRGD_3V Truth Table

NFPRST	NSLP_S3	PWRGD_PS	PWRGD_3V DELAY SELECT BIT	INTERNAL DELAY ELAPSED? 0 = NO 1= YES	PWRGD_3V, PWRGD_CPU (OD)
0	x	x	x	x	0
1	1-0 transition or 0 level	X	X	X	0
1	X	1-0 transition or 0 level	X	X	0
1	1	0-1 transition	0	X	1 (no delay)
1	1	0-1 transition	1	0	0 (delay time not elapsed)
1	1	0-1 transition	1	1	1 (after 100-120 msec delay)

Note: For PWRGD_CPU (OD), 1=Hi-Z.

Figure 18.4 shows a timing diagram for PWRGD_3V.

**Figure 18.4 PWRGD_3V Generation**

18.2.3 Power Supply Gate Circuit

The n3V_GATE and n3VSB_GATE outputs together control a S3 Dual voltage plane. The Dual plane has voltage applied in S3 through S0 and no voltage applied in S4 and S5.

Figure 18.2 illustrates the circuit and Figure 18.5 the n3VSB_GATE timing. The n3VSB_GATE and n3V_GATE are both active low signals. n3V_GATE is inverted from n3VSB_GATE.

When the n3V_GATE signal is low the dual voltage plane is connected to the main voltage plane. When the n3V_GATE signal is high the dual voltage plane is connected to the standby voltage plane.

The following three functions are OR'ed together to generate the n3VSB_GATE (active low) output:

1. The n3V_GATE output is asserted when the of SLP_S3# is deasserted and PWROK is asserted.
2. The assertion of SLP_S5# input unconditionally asserts the n3V_GATE output. (no power applied to the dual power plane.)
3. The n3V_GATE output will remain asserted after SLP_S5# deasserts (rising edge) until PWR_OK asserts or VTR is removed.

Additionally, on VTR POR the n3V_GATE output will be asserted

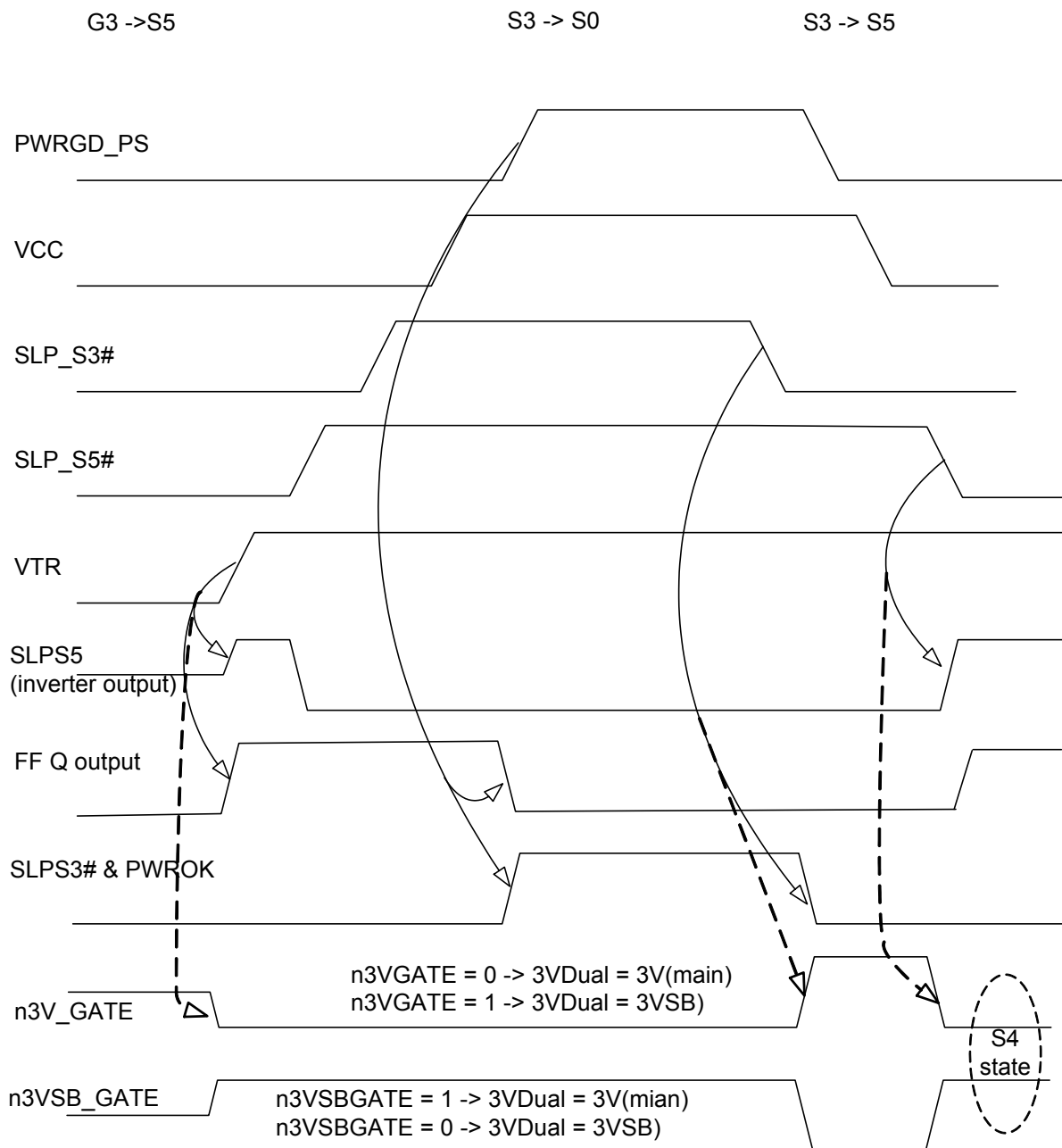


Figure 18.5 n3V_GATE Timing

Note 18.2 SLPS5 (inverter output), FF Q output, and SLPS3# & PWROK (AND gate output) are internal to SCH5017 and are shown in [Figure 18.5](#) to indicate effect of Power State transitions.

Note 18.3 In the S3 to S5 power transition and the S5 to S3 power transition the S3 Dual Plane power is switch to main when no power is applied to the main power plane. This is shown in [Figure 18.5](#) as the S4 State of the 3V_GATE and 3VSB_GATE outputs.

18.3 A/C Power Failure Recovery Control

The Power Failure Recovery Control logic, which is powered by VTR, is used to return a system to a pre-defined state after a power failure (VTR=0V). The [PWR_REC](#) Register, which is powered by Vbat, contains two bits defined as APF (After Power Failure). These bits are used to determine if the power supply should be powered on, powered off, or set to the previous power state before VTR was removed ([Table 18.3 on page 164](#)).

Note: The A/C Power Failure Recovery Logic is required to retain the state information through a power failure; therefore the Power Failure Recovery registers are powered by Vbat.

18.3.1 SLP_S3# determines the AC Recovery Previous State

The SLP_S3# signal is sampled by SCH5017 to determine the AC recovery previous state. If SLP_S3# is asserted when sampled, VCC should be off. If SLP_S3# is deasserted when sampled, VCC should be on.

If a power failure occurs and the Power Supply should be in the ON state, the Power Failure Recovery logic will generate a PME wake event when VTR power returns. This will cause a assertion of the nIO_PME_S5 pin which will wake up the system

18.3.2 Modes for determining the AC Recovery Previous State

Two modes may be used to determine the previous state of the SLP_S3# pin in the event of a power failure. This allows the system to recover from a power failure.

Mode 1: (Suggested)

Mode 1, which is enabled when Bit[3] S3_SLP# sampling is disabled, latches the current value of the S3_SLP# pin when VTR, VCC, or PWRGD_PS transition to the inactive state, whichever comes first. This value is latched into Bit[4] Previous State Bit of the [PWR_REC](#) Register located at offset 49h and is used to determine the state of the S3_SLP# pin when VTR becomes active.

Mode 2:

Mode 2 is enabled when Bit[3] S3_SLP# sampling is enabled. To determine the previous power state, the S3_SLP# pin is sampled every 0.5 seconds while VTR power. This sample is inserted into a battery powered 8-bit shift register. The hardware will select a bit from the shift register depending on the value of the S3_SLP# Previous State Select bits in the [SLP_S3_Pre_State](#) register located in the Runtime Register block at offset 53h to determine the state of the S3_SLP# pin when VTR becomes active. The value in the 8-bit shift register is latched into the [SLP_S3_Shift](#) Register at offset 4Ah in the Runtime Register block after VTR power is returned to the system, but before the internal shift register is cleared and activated. The [SLP_S3_Shift](#) Register is a battery powered register that is only reset on a Vbat POR.

Note: In Mode 2, when VTR falls below [VTRIP](#) the current value of the S3_SLP# pin will be latched into Bit [4] Previous State Bit located in the [PWR_REC](#) at offset 49h. This bit will not be used by hardware, but may be read by software to determine the state of the S3_SLP# pin when the power failure occurred. See definition of [VTRIP on page 347](#)

If a power failure occurs and the Power Supply should be in the ON state, the Power Failure Recovery logic will generate a PME wake event when VTR powers returns and set the PFR_STS bit in the [PMES5_STS6](#) register. If the PFR_EN bit in the [PMES5_EN6](#) register is set then the nIO_PME_S5 pin will be asserted. The PFR_EN bit in the [PMES5_EN6](#) register default set and is Vbat powered. [Chapter 15, PME Support](#) for description of the PME support for this PME event.

If the Power Supply should remain off, the Power Failure Recovery logic will have will not generate a PME wake event and have no effect on the nIO_PME_S5 pin. The following table defines the possible states of PFR_STS bit in the [PMES5_STS6](#) after a power failure for each configuration of the APF bits.

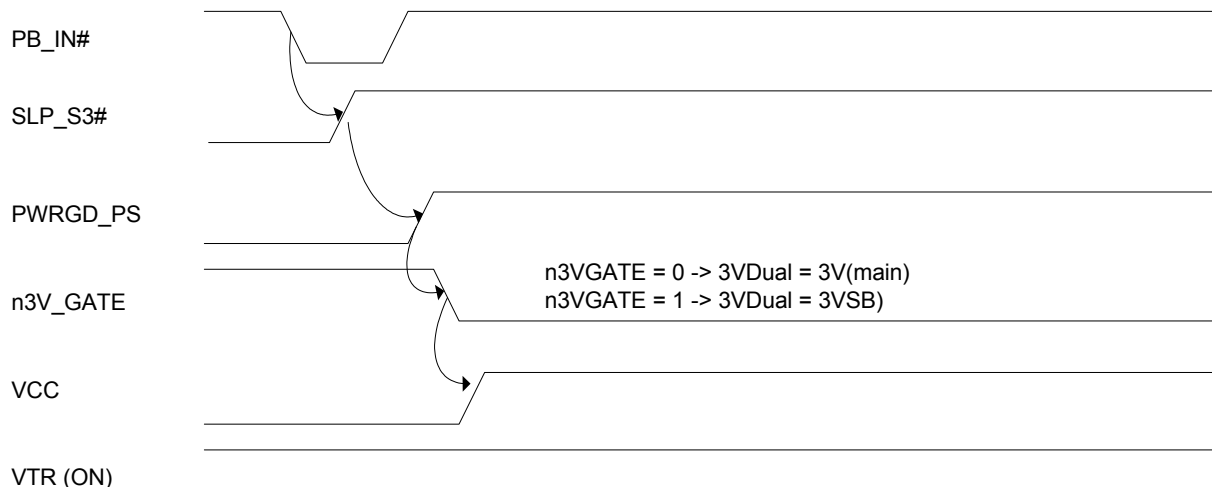
Table 18.3 Definition of APF Bits

APF[1:0]	DEFINITION OF APF BITS	AFTERG3 BIT (LOCATED IN ICH)	STATES OF PFR_STS BIT IN THE PMES5_STS6 REGISTER
00 11	Power Supply OFF	1	0
01	Power Supply ON	1	1
10	Power Supply set to Previous State (ON)	1	1
10	Power Supply set to Previous State (OFF)	1	0

Note: It is a requirement that the AFTERG3 bit located in the ICH controller be programmed to 1 for this AC Recovery logic to be used.

18.3.3 Power Supply Timing Diagrams

The following diagrams show the relative timing for the I/O pins associated with the Power Control logic. These are conceptual diagrams to show the flow of events.


Figure 18.6 Power Supply During Normal Operation

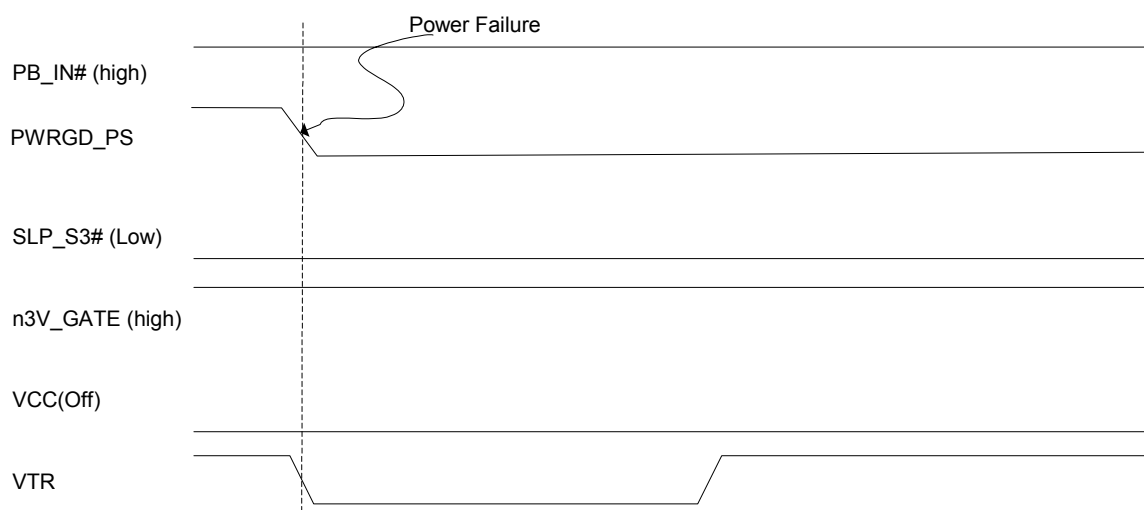


Figure 18.7 Power Supply After Power Failure (Return to Off)

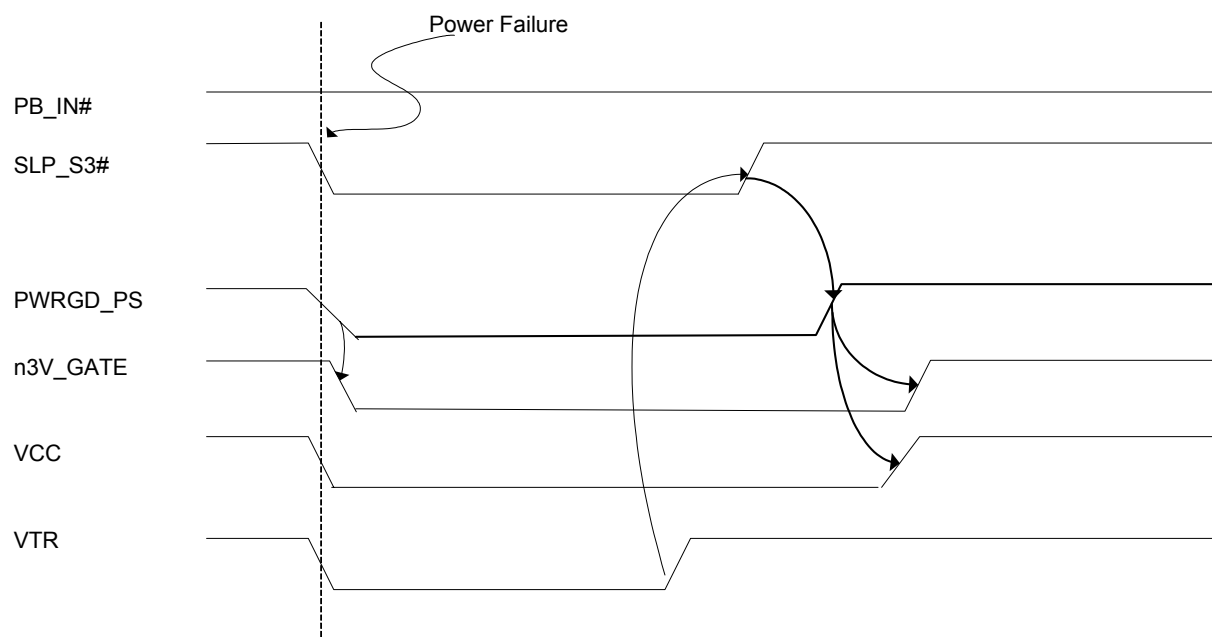


Figure 18.8 Power Supply After Power Failure (Return to On)

18.4 Resume Reset Signal Generation

nRSMRST signal is the reset output for the ICH resume well. This signal is used as a power on reset signal for the ICH.

SCH5017 detects when VTR voltage raises above [VTRIP](#), provides a delay before generating the rising edge of nRSMRST. See [Section 32.10, "Resume Reset Signal Generation," on page 347](#) for a detailed description of how the nRSMRST signal is generated.

18.5 Keyboard Power Button

The SCH5017 has logic to detect a keyboard make/break scan codes that may be used for wakeup (PME generation). The scan codes are programmed in the Keyboard Scan Code Registers, located in the runtime register block, from offset 0x5F to 0x63 from the base address located in the primary base I/O address in Logical Device A. These registers are powered by Vbat and are reset on a Vbat POR.

The following sections will describe the format of the keyboard data, the methods that may be used to decode the make codes, and the methods that may be used to decode the break codes.

The Wake on Specific Key Code feature is enabled for the assertion of the nIO_PME_S5 signal in S4 or S5 power states and for assertion of the nIO_PME_S3 signal when in S3 power state or below See [Section 15.4, "Wake on Specific Key Code," on page 149](#).

18.5.1 Keyboard Data Format

Data transmissions from the keyboard consist of an 11-bit serial data stream. A logic 1 is sent at an active high level. The following table shows the functions of the bits.

BIT	FUNCTION
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd parity)
11	Stop Bit (always 1)

The process to find a match for the scan code stored in the Keyboard Scan Code register meets the timing constraints as defined by the IBM Personal System/2™ Model 50 and 60 Technical Reference, dated April 1987. The timing for the keyboard clock and data signals are shown in [Chapter 32, "Timing Diagrams," on page 329](#). (See [Section 32.9, "Keyboard/Mouse Interface Timing," on page 346](#)).

18.5.1.1 Method for Receiving data is as follows:

The wake on specific key logic snoops the keyboard interface for a particular incoming scan code, which is used to wake the system through a PME event. These scan codes may be comprised of a single byte or multiple bytes. To determine when the first key code is being received, the wake on specific key logic begins sampling the data at the first falling edge of the keyboard clock for the start bit. The data is sampled on each falling edge of the clock. The hardware decodes the byte received and determines if it is valid (i.e., no parity error). Valid scan code bytes received are compared to the programmed scan code as determined by bits [3:2] SPEKEY Scan Code located in the [Keyboard PWRBTN/SPEKEY](#) Runtime register located at offset 0x64. If the scan code(s) received matches the value(s) programmed in the Keyboard Scan Code registers then a wake on specific key status event has occurred. The wake on specific key status event is mapped to the PME and Power Button logic.

Datasheet

The snooping logic always checks the incoming data byte for a parity error. The hardware samples the parity bit and checks that the 8 data bits plus the parity bit always have an odd number of 1's (odd parity). If a parity error is detected the state machine used to decode the incoming scan code is reset and begins looking for the first byte in the keyboard scan code sequence.

This process is repeated until a match is found. See [Section 18.5.2, "System for Decoding Scan Code Make Bytes Received from the Keyboard," on page 168](#) and [Section 18.5.3, "System for Decoding Scan Code Break Bytes Received from the Keyboard," on page 169](#).

If the scan code received matches the programmed make code stored in the Keyboard Scan Code registers and no parity error is detected, then it is considered a match. When a match is found and if the stop bit is 1, a PME wake event (KB_PB_STS-See [Figure 18.1](#)) will be generated within 100usec of the falling edge of clock 10 of the last byte of the sequence. This wake event may be used to generate the assertion of the nIO_PME_S3 signal when in S3 power state or below and nIO_PME_S5 signal in S4 or S5 power states. [Section 15.4, "Wake on Specific Key Code," on page 149](#) for description of the PME support for this PME event.

The state machine will reset and repeat the process until it is shut off by setting the SPEKEY_EN bit in the [CLOCKI32](#) register to '1'.

The SPEKEY_EN bit at bit 1 of the [CLOCKI32](#) register at 0xF0 in Logical Device A is used to control the "wake-on-specific feature. This bit is used to turn the logic for this feature on and off. It will disable the 32kHz clock input to the logic. The logic will draw no power when disabled. The bit is defined as follows:

0= "Wake on specific key" logic is on (default)

1= "Wake on specific key" logic is off

The state machine used to snoop the incoming data from the keyboard is synchronized by the clock high and low time. If the KCLK signal remains high or low for a nominal 125usec during the transmission of a byte, a timeout event is generated causing the snooping and scan code decoding logic to be reset, such that it will look for the first byte of the make or break scan code.

18.5.1.2 Description Of SCAN 1 and SCAN 2

SCAN 1:

Many standard keyboards (PC/XT, MFII, etc.) generate scan 1 make and break codes per key press. These codes may be generated as a single byte or multi-byte sequences. If a single byte is generated, the make code, which is used to indicate when a key is pressed, is a value between 0h and 7Fh. The break code, which is used to indicate when a key is released, is equal to the make code plus 80h (i.e. $80h \leq \text{Break Code} \leq FFh$). If a multi-byte sequence is sent it will send E0h before the make or break.

Example of Single Byte Scan 1: Make Code = 37h, Break Code=B7h

Example of Multi-byte Scan 1: Make Code = E0h 37h, Break Code = E0h B7h.

SCAN 2:

The scan 2 make and break codes used in AT and PS/2 keyboards, which are defined by the PC 8042 Keyboard Controller, use the same scan code when a key is pressed and when the key is released. A reserved release code, 0xF0, is sent by the keyboard immediately before the key specific portion of the scan code to indicate when that the key is released.

Example of Single Byte Scan 2: Make Code = 37h, Break Code=F0h 37h

Example of Multi-byte Scan 2: Make Code = E0h 37h, Break Code = E0h F0h 37h.

18.5.2 System for Decoding Scan Code Make Bytes Received from the Keyboard

Bit [3:2] of the SPEKEY Scan Code, located in [Keyboard PWRBTN/SPEKEY](#) register, is used to determine if the hardware is required to detect a single byte make code or a multi-byte make code. [Table 18.4](#) summarizes how single byte and multi-byte scan codes are decoded.

Keyboard Scan Code - Make Byte 1
37h

Figure 18.9 Sample Single-Byte Make Code

MSB	LSB
Keyboard Scan Code - Make Byte 1	Keyboard Scan Code - Make Byte 2
E0h	37h

Figure 18.10 Sample Multi-Byte Make Code

Note: In multi-byte scan codes the most significant byte (MSB) will be received first.

Table 18.4 Decoding Keyboard Scan Code for Make Code

SPEKEY SCAN CODE		NUMBER OF BYTES IN MAKE CODE	DESCRIPTION
Bit[3]	Bit[2]		
X	0	1 byte	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Make Byte 1 located in the Runtime Register block at offset 5Fh. If the data byte received matches the value stored in the register, a wake on specific key status event will be generated. This wake event may be used to generate the assertion of the nIO_PME_S3 signal and/or nIO_PME_S5 signal. Section 15.4, "Wake on Specific Key Code," on page 149. Note: If the value programmed in Keyboard Scan Code – Make Byte 1 is 00h it is treated as a don't care and any valid scan code being compared to this byte will be a match.
X	1	2 byte	The wake on specific key logic compares each valid data byte received with the value programmed in the Keyboard Scan Code – Make Byte 1 located in the Runtime Register block at offset 5Fh. If the data byte received matches the value stored in the register, the hardware compares the next byte received with the value programmed in the Keyboard Scan Code – Make Byte 2 located in the Runtime Register block at offset 60h. If the consecutive bytes received match the programmed values, a wake on specific key status event is generated. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine is reset and the process is repeated. If a specific key status event is generated then it may be used to generate the assertion of the nIO_PME_S3 signal and/or nIO_PME_S5 signal. Section 15.4, "Wake on Specific Key Code," on page 149 Note: If the value programmed in Keyboard Scan Code – Make Byte 1 or Keyboard Scan Code -Make Byte2 is 00h it is treated as a don't care and any valid scan code being compared to this byte will be a match.

Datasheet**Notes:**

- X' represents a don't care.
- By default, any time the KCLK signal is high or low for a nominal 125usec during the transmission of a byte the scan code decode cycle will be reset and the next byte received will be treated as the first byte received in the scan code byte sequence.

Once a valid make code is detected the wake on specific key logic will generate a KB_PB_STS wake event (see [Figure 18.1](#)). This wake event may be used to generate the assertion of the nIO_PME_S3 signal when in S3 power state or below and nIO_PME_S5 signal in S4 or S5 power states. [Section 15.4, "Wake on Specific Key Code," on page 149](#) for description of the PME support for this PME event

18.5.3 System for Decoding Scan Code Break Bytes Received from the Keyboard

To accommodate different keyboards, there are three options for determining when the wake on specific key logic deasserts the KB_PB_STS wake event (See in [Figure 18.1](#)) going to the sticky bits in [PMES5_STS3](#) and [PMES5_STS6](#). Deassertion of the KB_PB_STS internally does not deassert the PME status bit.

The Keyboard Power Button Release bits (Bits [4:5]) in [Keyboard PWRBTN/SPEKEY](#) register may select these KB_PB_STS options. See [Chapter 28, "Runtime Registers," on page 271](#). A detailed description of each option is shown below.

Option 1 (00): De-assert KB_PB_STS 0.5sec after it is asserted.

This option allows the user to program any scan code into the Keyboard Scan Code – Make Byte Register(s). When a valid scan code is received that matches the value programmed in the Keyboard Scan Code Register(s), a 0.5sec pulse is generated on the KB_PB_STS wake event. Regardless of the state of the SPEKEY bits in [PMES5_STS3](#) and [PMES5_STS6](#), no additional wake events will occur for 0.5sec.

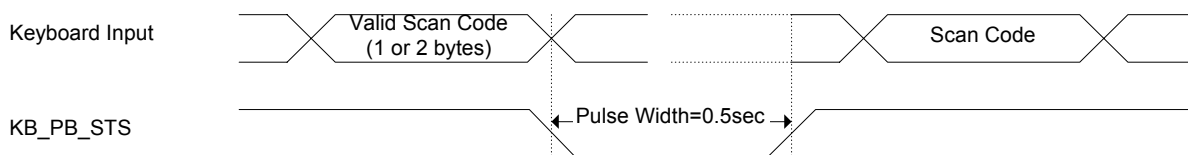


Figure 18.11 Option 1: KB_PB_STS wake event fixed pulse width

Option 2 (01): De-assert KB_PB_STS after Scan Code Not Equal Programmed Make Code

This option may be used by keyboards that emit single byte or multi-byte make codes for each key pressed. When a valid Scan Code is received that matches the value programmed in the Keyboard Scan Code – Make Byte Register(s), the KB_PB_STS wake event signal will be held asserted low until another valid Scan Code is received that is not equal to the programmed make code. Regardless of the state of the SPEKEY bits in [PMES5_STS3](#) and [PMES5_STS6](#), no additional wake events will occur until another valid Scan Code is received that is not equal to the programmed make code.

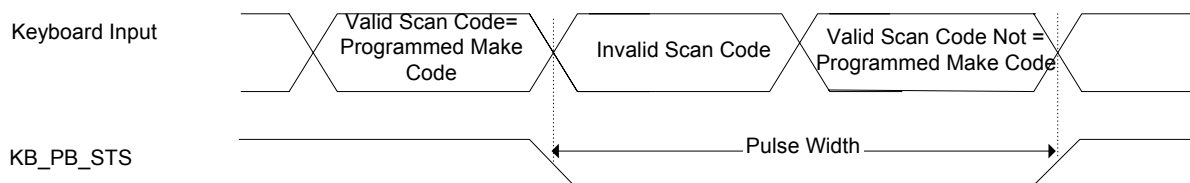


Figure 18.12 Option 2: Assert KB_PB_STS wake event until scan code not programmed make code

Notes:

- The Valid Scan Code may be 1 or 2 bytes depending on the SPEKEY ScanCode bits located in the [Keyboard PWRBTN/SPEKEY](#) Runtime register at offset 64h.
- A Valid Scan Code for single byte codes means that no parity error exists. A Valid Scan Code for Multi-byte Scan Codes requires that no parity error exists and that the first Byte received matches the value programmed in the Keyboard Scan Code – Make Byte 1 located in the Runtime Register block at offset 5Fh. This value is typically E0h for Scan 1 and Scan 2 type keyboards. (Example: The ACPI power scan 2 make code is E0h, 37h) [Section 18.5.1.2, "Description Of SCAN 1 and SCAN 2," on page 167](#)

Option 3 (10): De-assert KB_PB_STS after Scan Code Equal Break Code

This option may be used with single byte and multi-byte scan 1 and scan 2 type keyboards. The break code can be configured for a specific break code or for any valid break code.

the KB_PB_STS wake event signal will be held asserted low until a valid break code is detected. The break code can be configured for a specific break code or for any valid break code. Regardless of the state of the SPEKEY bits in [PMES5_STS3](#) and [PMES5_STS6](#), no additional wake events will occur until another until a valid break code is detected.

Note: [Table 18.5](#) defines how the scan code will be decoded for the Break Code. Once a valid break code is detected, the keyboard power button event will be de-asserted as shown in [Figure 18.13](#).

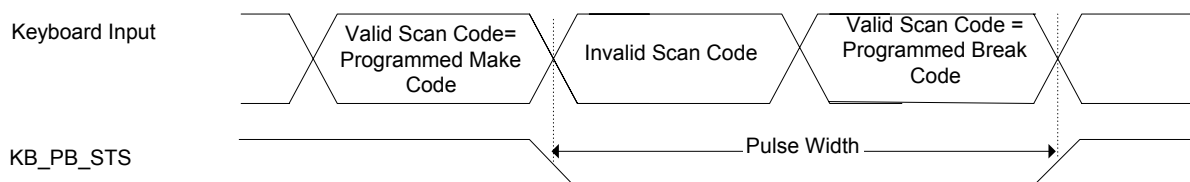


Figure 18.13 Option 3: De-assert KB_PB_STS when scan code equal break code

Note: The SPEKEY ScanCode bits are located in the [Keyboard PWRBTN/SPEKEY](#) register located at offset 64h.

Table 18.5 Decoding Keyboard Scan Code for Break Code

SPEKEY SCAN CODE		SCAN CODE	NUMBER OF BYTES IN BREAK CODE	DESCRIPTION
Bit[3]	Bit[2]			
0	0	Scan 1	1 Byte	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deassert the PME status bit.
0	1	Scan 1	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deassert the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.
1	0	Scan 2	2 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If this byte is a valid scan code and it matches the value programmed, the wake on specific key status event (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deassert the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.
1	1	Scan 2	3 Bytes	The wake on specific key logic will compare each valid data byte received with the Keyboard Scan Code – Break Byte 1 located in the Runtime Register block at offset 61h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 2 located in the Runtime Register block at offset 62h. If the data byte received matches the value stored in the register, the next byte received will be compared to Keyboard Scan Code – Break Byte 3 located in the Runtime Register block at offset 63h. If this byte is a valid scan code and it matches the value (KB_PB_STS) will be de-asserted. Deassertion of the KB_PB_STS internally does not deassert the PME status bit. If the values do not match, if a parity error occurs, or if a timeout occurs, the state machine will be reset and repeat the process.

Note: To de-assert wake on specific key status event (KB_PB_STS) on any valid break key the register containing the LSB of the break code should be programmed to 00h. If a Keyboard Scan Code – Break Byte register is programmed to 00h then any valid scan code will be a match. The value 00h is treated as a Don't Care.

18.6 Wake on Specific Mouse Event

The device can generate S3 or S5 wake events (nIO_PME_S3 or nIO_PMES5 pins) based on detection of specific Mouse button clicks on a Mouse connected to the Mouse port interface (MDAT and MCLK pins). The following specific Mouse events can be used for wake-up events:

1. Any button click (left/right/middle) or any movement
2. Any one click of left/right/middle button
3. one click of left button
4. one click of right button
5. two times click of left button
6. two times click of right button

In addition to the Idle detection logic there is Start Bit Time-out logic which detects any time MCLK stays high for more than 115-145us.

Chapter 19 Intruder Detection Support

A switch connected to the chassis cover indicates if the cover is on or off. When the cover is removed, the nINTRD_IN input will transition from high-to-low or low-to-high depending on the type of switch used (normally open or normally closed).

Whenever the nINTRD_IN input goes high-to-low or low-to-high, the INTRUSION bit is set in the INTRD register. The INTRUSION bit is set when an intrusion event occurs. The INTRUSION bit will remain set until cleared by software. This bit and input logic are powered by VBAT so that an intrusion condition is detected and stored even if VTR is removed.

The INTRD_STS bit indicates the current (inverted) state of the nINTRD_IN pin. The INTRD_STS bit is battery backed up. This bit will reflect the inverse of the state of the nINTRD_IN pin.

The INTRD_STS and INTRUSION bits are in the Intruder Detection register (LD0A runtime register at an offset 0x52). This register is powered by VTR and battery backed up.

19.1 Intrusion Bit

The INTRUSION bit is to be set on any transition of INTRUD_IN (low-to-high or high-to-low). This provides the flexibility to use normally "open" or "closed" switches and also change the circuit. Any transition on the nINTRD_IN pin will set the INTRUSION bit and the PME and SMI status bits.

Note: if a normally open switch is used, when the cover is closed this input will be externally pulled-up to VBAT. When the cover is opened this input will be connected to GND.

APPLICATION NOTE: The nINTRD_IN pin requires an external pull-up to VBAT. The recommended use of this pin is with a normally open switch. The use of a normally closed switch will cause excessive battery drain.

The INTRUSION bit will default to '1' on VBAT POR (battery removed and replaced or battery voltage below approximately 1.2V). The INTRUSION bit will be set to '1' if an intrusion event occurs or if a VBAT POR occurs.

Writing '0' to the INTRUSION bit will clear it, regardless of the state of the nINTRD_IN pin. Writing '1' to the INTRUSION bit has no effect.

19.2 Intruder PME and SMI Generation

This wake event may be used to generate the assertion of the nIO_PME_S3 signal when in S3 power state or below and nIO_PME_S5 signal in S4 or S5 power states.

There are SMI status and enable bits and PME status and enable bits for the intrusion event. See the SMI and PME runtime registers for the location and description of these bits ([PMES3_STS6](#), [PMES3_EN6](#), [PMES5_STS6](#), [PMES5_EN6](#), [SMI_STS1](#), [SMI_EN1](#)). The SMI and PME status bits are set under VCC power, VTR power or on VTR POR, as they "shadow" the INTRUSION bit. The SMI and PME status bits are cleared on a write of '1'.

User Note: Following an intrusion event, the PME and SMI status bits are cleared on a write of '1'. The INTRUSION bit does not have to be cleared in order to clear the PME and SMI status bits. However, the PME and SMI status bits will not be set by another intrusion event until the INTRUSION bit is cleared.

These bits function in one of three cases:

- **Case 1.** An intrusion occurs under battery power only or a VBAT POR occurs. In this case, the event will be latched under battery power and the "INTRUSION" PME and SMI status bits will be set when VTR returns. Therefore, the PME and SMI status bits will have two possible default values on VTR POR, depending on whether or not the intrusion event occurred under battery power. The INTRUSION bit in [PMES5_EN6](#) defaults to set on Vbat POR; therefore, when VTR

returns, an S5 PME (via nIO_PME_S5 pin assertion.) After the first cycle through all the power state, software can clear the INTRUSION enable bit in **PMES5_EN6** to block Intrusion events from generating a S5 PME. The state of the INTRUSION enable bit in **PMES5_EN6** is maintained through all power states by RTC power. Both **PMES3_EN6** and **SMI_EN1** INTRUSION bits are cleared on VTR POR, so there will be no S3 PME (via nIO_PME_S3 assertion) or SMI generated. When VCC goes active, and the OS sets the enable bits, a S3 PME and/or SMI will be generated. If the corresponding PME enable bit is set, a PME will be generated under VCC power. If the corresponding SMI enable bit is set, an SMI will be generated under VCC power. Therefore, in this case, setting the enable bit (low-to-high edge) will trigger the generation of the S3 PME and SMI.

- Case 2. An intrusion occurs under VTR power (VCC=0). In this case, the “INTRUSION” S5 PME, S3 PME and SMI status bits will be set. If the corresponding S3 or S5 PME enable bit is set, a S3 and/or S5 PME will be generated under VTR power. In this case, setting the status bit (low-to-high edge) will trigger the generation of the S3 or S5 PME. If the corresponding SMI enable bit is set, an SMI will be generated when VCC goes active. In this case, setting the status bit (low-to-high edge) will trigger the generation of the SMI, however the SMI pin will not go active until VCC goes active.
- Case 3. An intrusion occurs under VCC power. In this case, the “INTRUSION” S3 PME, S5 PME and SMI status bits will be set. If the corresponding PME enable bit is set, a S3 and/or S5 PME will be generated under VCC power. If the corresponding SMI enable bit is set, an SMI will be generated under VCC power. In this case, setting the status bit (low-to-high edge) will trigger the generation of the PME and SMI.

Chapter 20 Low Battery Detection Logic

The low battery detection logic monitors the battery voltage to detect if this voltage drops below 2.2V and/or 1.2V. If the device is powered by Vbat only and the battery voltage is below approximately 1.2V, a VBAT POR will occur upon a VTR POR. If the device detects the battery voltage is below approximately 2.2V while it is powered by Vbat only or VTR (VCC=0V) the LOW_BAT PME and SMI Status bits will be set upon a VCC POR. When the external diode voltage drop is taken into account, these numbers become 1.5V and 2.5V, respectively.

The LOW_BAT PME event is indicated and enabled via the [PMES3_STS6](#) and [PMES3_EN6](#) registers. See [Chapter 28, "Runtime Registers," on page 271](#) for a description of these registers.

The LOW_BAT SMI event is indicated and enabled via the [SMI_STS1](#) and [SMI_EN1](#) registers. See the [Runtime Registers](#) section for a description of these registers.

The following figure illustrates external battery circuit.

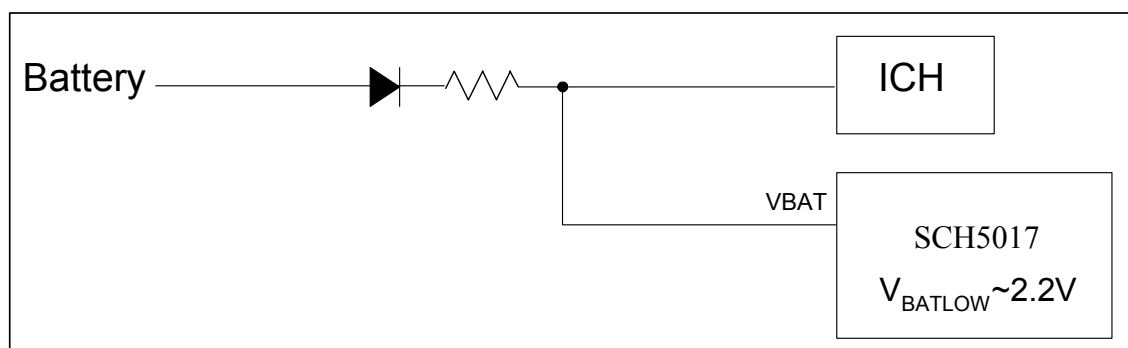


Figure 20.1 External Battery Circuit

Note that the battery voltage of 2.2V nominal is at the VBAT pin of the device, not at the source.

20.1 VBAT POR

When VBAT drops below approximately 1.2V while both VTR and VCC are off, a VBAT POR will occur upon a VTR POR.

The INTRUSION bit is set to '1' upon a VBAT POR.

The LOW_BAT PME and SMI Status bits is set to '1' upon a VBAT POR. Since the PME enable bit is not battery backed up and is cleared on VTR POR, the VBAT POR event is not a wakeup event. When VCC returns, if the PME or SMI enable bit (and other associated enable bits) are set, then the corresponding event will be generated.

20.2 Low Battery

20.2.1 Under Battery Power

If the battery voltage drops below approximately 2.2V under battery power (VTR and VCC off) then the LOW_BAT PME and SMI Status bits will be set upon a VCC POR. This is due to the fact that the LOW_BAT event signal is only active upon a VCC POR, and therefore the low battery event is not a wakeup event. When VCC returns, if the PME or SMI enable bit (and other associated enable bits) are set, then a corresponding event will be generated.

20.2.2 Under VTR Power

If the battery voltage drops below approximately 2.2V under VTR power (VCC off) then the LOW_BAT PME and SMI Status bits will be set upon a VCC POR. The corresponding enable bit (and other associated enable bits) must be set to generate a PME or an SMI.

If the PME enable bit (and other associated enable bits) were set prior to VCC going away, then the low battery event will generate a PME when VCC becomes active again. It will not generate a PME under VTR power and will not cause a wakeup event.

If the SMI enable bit (and other associated enable bits) were set prior to VCC going away, then the low battery event will generate an SMI when VCC becomes active again.

20.2.3 Under VCC Power

The LOW_BAT PME and SMI bits are not set when the part is under VCC power. They are only set upon a VCC POR. See [Section 20.2.2](#).

Chapter 21 Battery Backed Security Key Register

Located at the Secondary Base I/O Address of Logical Device A is a 32 byte CMOS memory register dedicated to security key storage. This security key register is battery powered and has the option to be read protected, write protected, and lockable. The Secondary Base I/O Address is programmable at offsets 0x62 and 0x63. See [Table 29.1, "Configuration Register Summary," on page 303](#). [Table 21.1, "Security Key Register Summary"](#) is a complete list of the Security Key registers.

Table 21.1 Security Key Register Summary

REGISTER OFFSET (HEX)	VBAT POR	REGISTER
00	0x00	Security Key Byte 0
01	0x00	Security Key Byte 1
02	0x00	Security Key Byte 2
03	0x00	Security Key Byte 3
04	0x00	Security Key Byte 4
05	0x00	Security Key Byte 5
06	0x00	Security Key Byte 6
07	0x00	Security Key Byte 7
08	0x00	Security Key Byte 8
09	0x00	Security Key Byte 9
0A	0x00	Security Key Byte 10
0B	0x00	Security Key Byte 11
0C	0x00	Security Key Byte 12
0D	0x00	Security Key Byte 13
0E	0x00	Security Key Byte 14
0F	0x00	Security Key Byte 15
10	0x00	Security Key Byte 16
11	0x00	Security Key Byte 17
12	0x00	Security Key Byte 18
13	0x00	Security Key Byte 19
14	0x00	Security Key Byte 20
15	0x00	Security Key Byte 21
16	0x00	Security Key Byte 22
17	0x00	Security Key Byte 23
18	0x00	Security Key Byte 24
19	0x00	Security Key Byte 25

Table 21.1 Security Key Register Summary (continued)

REGISTER OFFSET (HEX)	VBAT POR	REGISTER
1A	0x00	Security Key Byte 26
1B	0x00	Security Key Byte 27
1C	0x00	Security Key Byte 28
1D	0x00	Security Key Byte 29
1E	0x00	Security Key Byte 30
1F	0x00	Security Key Byte 31

Access to the Security Key register block is controlled by bits [2:1] of the Security Key Control (SKC) Register located in the Configuration Register block, Logical Device A, at offset 0xF2. The following table summarizes the function of these bits.

Table 21.2 Description of Security Key Control (SKC) Register Bits[2:1]

BIT[2] (WRITE-LOCK)	BIT[1] (READ-LOCK)	DESCRIPTION
0	0	Security Key Bytes[31:0] are read/write registers
0	1	Security Key Bytes[31:0] are Write-Only registers
1	0	Security Key Bytes[31:0] are Read-Only registers
1	1	Security Key Bytes[31:0] are not accessible. All reads/write access is denied.

Note: When Bit[1] (Read-Lock) is '1' all reads to this register block will return 00h.

- As an added layer of protection, bit [0] SKC Register Lock bit has been added to the Security Key Control Register. This lock bit is used to block write access to the Write-Lock and Read-Lock bits defined in the table above. Once this bit is set it can only be cleared by a VTR POR, VCC POR, and PCI Reset. See [Table 29.12, "PME. Logical Device A \[Logical Device Number = 0X0A\]," on page 317](#) for the definition of the Security Key Register.

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Chapter 22 Speaker Warning Output

The SCH5017 contains a alarm annunciation output on the SPEAKER pins. The SPEAKER pin outputs a warning tone for the following events:

- Voltage over limit.
- Temperature over limit.
- Fan speed over limit.
- Chassis opened.
- Software controlled register written.

This pin is an open drain output and the default state is low. When activated the speaker output is as follows:

Repeated 512 Hz square wave (duty cycle 50%) for 0.5 second then 1.024 KHz square wave (duty cycle 50%) for 0.5 second until the enable bit or status bit is cleared.

The input events for the Speaker Generator Circuit shall be the Hardware Monitor Interrupt signal (nHWM_INT-See [Section 25.6, "Interrupt Signal," on page 198](#)), the INTRD_STS bit in INTRD register, and the SW_EVENT bit in the SPKR Register. The SPKR Register also contains an enable bit for intruder detect event and an enable bit for the HW monitor event, as well as, a global output enable bit and an event status bit.

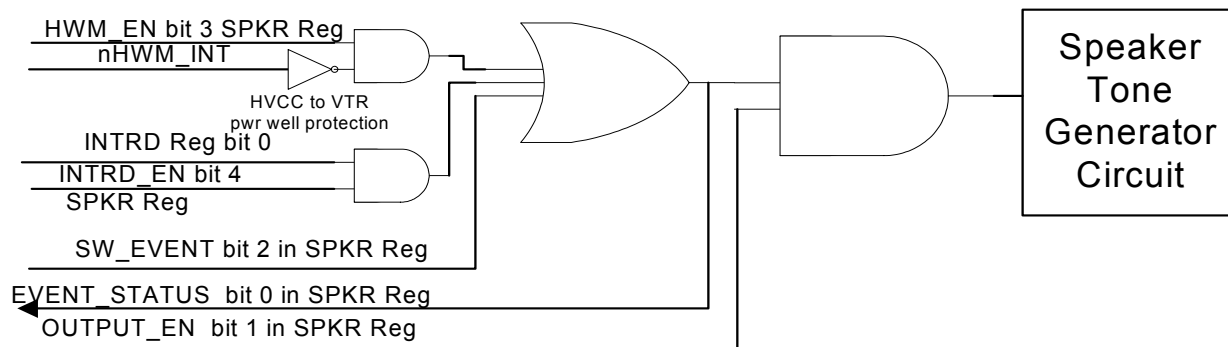
When an Speaker event occurs, the speaker output shall generate a minimum of 3 second waveform output. For example, if the nHWM_INT is intermittent every several seconds (caused temperature right at upper limit), then the speaker will retrigger and make three lower and three higher tones for total duration of 3 to 4 seconds and wait for next speaker event.

The speaker output shall complete each 0.5 second tone once started.

[Table 22.1](#) and [Figure 22.1](#) describe the Speaker interface and circuit. The EVENT_STATUS, SW_EVENT, HWM_EN and INTRD_EN bits in the SPKR Register control Speaker event routing to the Speaker Generator Circuit as shown in [Figure 22.1](#). Therefore, when enabled, an event will generate a minimum 3 second waveform speaker output as described above. The speaker output shall complete the remainder of the 0.5 second tone if software Disables an active speaker event.

Table 22.1 Speaker Interface

NAME	DIRECTION	DESCRIPTION
SPEAKER	Output	Speaker Output. Provides audio warning of HW Monitor or Intruder events and may be enabled by software.



Note: This figure is for illustration purposes only and not meant to imply specific implementation details

Figure 22.1 Speaker Enable Circuit

Chapter 23 SMBus Interface

The host processor communicates with the Fan Monitoring device through a series of read/write registers via the SMBus interface. SMBus is a serial communication protocol between a computer host and its peripheral devices.

23.1 Slave Address

The default Slave Address is 0101110b. If this address is desired, the designer should not ground the Address Enable# pin and should not apply a strapping resistor to the Address Select pin.

If multiple devices are implemented in a system or another SMBus device requires address 0101110b, FANTACH4 and PWM3 must be disabled. In this case, addressing is implemented as follows:

The board designer will apply a 10K Ω pull-down resistor to ground on the Address Enable# pin. Upon power up, the SCH5017 device will be placed into Address Enable mode and assign itself an SMBus address according to the Address Select input. The device will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the SCH5017 address. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection.

Table 23.1 SMBus Slave Address Options

ADDRESS ENABLE#	ADDRESS SELECT	BOARD IMPLEMENTATION	SMBUS ADDRESS [7:1]
1	X	Address Enable# pulled to HVTR through resistor (Note: Resistor value will be dependent on PWM circuit implemented.)	0101 110b (default)
0	0	Address Enable# pulled to ground through 10k Ω resistor Address Select Pulled to ground through a 10k Ω resistor	0101 100b
0	1	Address Enable# pulled to ground through 10k Ω resistor Address Select pulled to HVTR through a 10k Ω resistor	0101 101b

In this way, there can be up to three SCH5017 devices on the SMBus at any time. Multiple SCH5017 devices can be used to monitor additional processors and temperature zones.

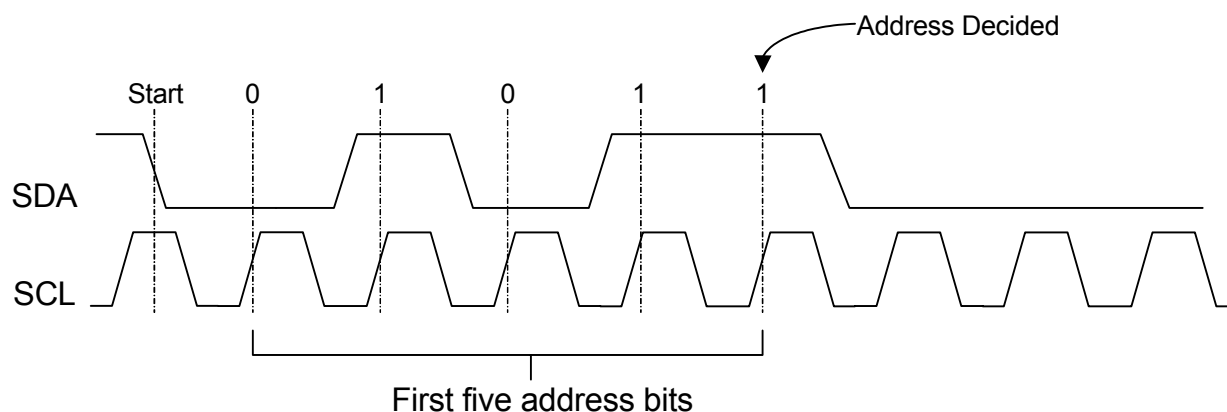


Figure 23.1 Address Selection on SCH5017

23.2 Slave Bus Interface

The SCH5017 device SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports four protocols.

The Write Byte, Read Byte, Send Byte, and Receive Byte protocols are the only valid SMBus protocols for the device. This part responds to other protocols as described in the Invalid Protocol Section. Reference the System Management Bus Specification, Rev 2.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in section 11 Register Set on page 31.

23.3 Bus Protocols

Typical Write Byte, Read Byte, Send Byte, and Receive Byte protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the Hardware Monitor Block driving data on the SDA line; otherwise, host data is on the SDA line.

The slave address is the unique SMBus Interface Address for the Hardware Monitor Block that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

Byte Protocols

A write byte transfer will always consist of the SMBus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. The normal read protocol consists of a write to the Hardware Monitor Block with the SMBus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the SMBus Interface Address byte, followed by the data byte read from the Hardware Monitor Block. This can be accomplished by using the Read Byte protocol or by using the Send Byte protocol followed by the Receive Byte protocol.
2. If the Internal Address Register is known to be at the desired Address, simply read the Hardware Monitor Block with the SMBus Interface Address byte, followed by the data byte read from the Hardware Monitor Block. This corresponds to the Receive Byte protocol.

Write Byte

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in [Table 23.2](#) is performed correctly. Only one byte is transferred at time for a Write Byte protocol.

Table 23.2 SMBus Write Byte Protocol

Field	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Reg. Data	Ack	Stop
Bits	1	7	1	1	8	1	8	1	1

Read Byte

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in [Table 23.3](#) is performed correctly. Only one byte is transferred at time for a Read Byte protocol.

Table 23.3 SMBus Read Byte Protocol

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1	7	1	1	8	1	1

Send Byte

The Send Byte protocol is used to set the Internal Address Register to the correct register in the Hardware Monitor Block. No data is transferred for a Send Byte protocol. The Send Byte can be followed by the Receive Byte protocol described below in order to read data from the register. The send byte protocol cannot be used to write data - if data is to be written to a register then the write byte protocol must be used as described in subsection above. The send byte protocol is shown in [Table 23.4](#).

Table 23.4 SMBus Send Byte Protocol

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Stop
Bits:	1	7	1	1	8	1	1

Receive Byte

The Receive Byte protocol is used to read data from the registers when the register address is known to be at the desired address (using the Internal Address Register). This is used when the register address has been written to the desired address using the Send Byte protocol. This can be used for successive reads of the same register. The data will only be read if the protocol shown in [Table 23.5](#) is performed correctly. Only one byte is transferred at time for a Receive Byte protocol.

Table 23.5 SMBus Receive Byte Protocol

Field:	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1

23.4 Invalid Protocol Response Behavior

Registers that are accessed with an invalid protocol will not be updated. A register will only be updated following a valid protocol. The only valid protocols are the Write Byte, Read Byte, Send Byte, and Receive Byte protocols, which are described above.

The SCH5017 device responds to three SMBus slave addresses:

1. The SMBus slave address that supports the valid protocols defined in the previous sections is determined by the level on the Address Select and Address Enable pins as shown in [Section 23.1, "Slave Address,"](#) on page 181.
2. SMBus Alert Response (0001 100). The SMBus will only respond to the SMBus Alert Response Address if the SMBus Alert Response interrupt was generated to request a response from the Host. The SMBus Alert Response is defined in [Section 23.10, "SMBus Alert Response Address,"](#) on page 184.

Attempting to communicate with the Hardware Monitor Block over SMBus with an invalid slave address, or invalid protocol will result in no response, and the SMBus Slave Interface will return to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. See [Section 23.4.1, "Undefined Registers"](#) for response to undefined registers.

23.4.1 Undefined Registers

Reads to undefined registers return 00h. Writes to undefined registers have no effect and return no error.

23.5 General Call Address Response

The SCH5017 will not respond to a general call address of 0000_000.

23.6 Slave Device Time-Out

The SCH5017 supports the slave device timeout as per the SMBus Specification, v2.0.

According to SMBus specification, v2.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25ms ($T_{\text{TIMEOUT, MIN}}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35ms ($T_{\text{TIMEOUT, MAX}}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition

23.7 Stretching the SCLK Signal

The SCH5017 supports stretching of the SCLK by other devices on the SMBus. The Hardware Monitor Block does not stretch the SCLK.

23.8 SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing diagram shown in the section titled [SMBus Interface on page 349](#).

23.9 Bus Reset Sequence

The SMBus Slave Interface will reset and return to the idle state upon a START field followed immediately by a STOP field.

23.10 SMBus Alert Response Address

The SCH5017 device responds to the SMBus Alert Response Address, 0001 100, if the INTEN bit (register 7Ch bit 2) is set and one or more status events bits are high. The interrupt signal (nHWM_INT), which is located on a dedicated pin, can be used as the SMBALERT#. See the section describing the [Interrupt Status Registers on page 195](#) and the section describing the [Interrupt Pin \(nHWM_INT\) on page 198](#) for more details on interrupts.

The device can signal the host that it wants to talk by pulling the SMBALERT# low, if a status bit is set in one of the interrupt status registers and properly enabled onto the nHWM_INT pin. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through a modified Receive Byte operation with the Alert Response Address (ARA).

The SCH5017 device, which pulled SMBALERT# low, will acknowledge the Alert Response Address and respond with its device address. The 7-bit device address provided by the SCH5017 device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

Table 23.6 Modified SMBus Receive Byte Protocol Response to ARA

	Start	Alert Response Address	Rd	Ack	SCH5017 Slave Address	Nack	Stop
Field:							
Bits:	1	7	1	1	8	1	1

After acknowledging the slave address, the SCH5017 device will disengage the SMBALERT# pull-down by clearing the INT enable bit. If the condition that caused the interrupt remains, the Fan Control device will reassert the SMBALERT# on the next monitoring cycle, provided the INT enable bit has been set back to '1' by software.

Note: The SCH5017 device will respond to the SMBus Alert Response address if all the following conditions exist:

- The INTEN bit (register 7Ch bit 2) is set
- An individual status bit is set in one of the interrupt status registers
- The corresponding group enable bit is set. Each interrupt event must be enabled into the interrupt status registers, and the status bits must be enabled onto the nHWM_INT signal via the group enable bits for each type of event (i.e., temperature, voltage and fan). See the section titled [Interrupt Status Registers on page 195](#).



Chapter 24 SMBus Isolation Circuitry

Table 24.1 and Figure 24.1 describe the SMBus Isolation interface and circuit.

Table 24.1 SMB Isolation interface

NAME	BUFFER	POWER WELL	DESCRIPTION
SDA	IOD	HVTR	HWM SMBus DATA
SCLK	IOD	HVTR	HWM SMBus CLOCK
SDA1	nSW	VTR	SMBus DATA 1 POWER STATE ISOLATION 1 System Management Bus bi-directional Data.
SCLK1	nSW	VTR	SMBus DATA 1 POWER STATE ISOLATION 1 System Management Bus Clock.
SDA2	nSW	VTR	SMBus DATA 2 POWER STATE ISOLATION 2 System Management Bus bi-directional Data.
SCLK2	nSW	VTR	SMBus DATA 2 POWER STATE ISOLATION 2 System Management Bus Clock.
PWRGD_PS	ISPU_400	VTR	Power Good Input from Power Supply

The SMBus Isolation circuitry can be used to isolate the VCC powered SMBus signals from the VTR powered SMBus signals during power down modes. The SMB data pins and the SMB clock pins function as inputs shorted together through the isolation resistor. External pull-up resistors are required on the SMBus signals.

Figure 24.1 illustrates the SMB Architecture through the SCH5017 SMBus Isolation circuit. The SCH5017 SMBus Isolation circuit consists of the HW Monitor SMBus slave open drain pins which are powered by the same power as the HW Monitor (HVTR), two double pole n-channel switches, and control logic to enable the switches.

SCH5017 detects VTR voltage powerup. (See definition of [VTRIP](#) on page 347). The switch is controlled by the presence of VTR power, the PWRGD_PS input signal and [SMB_ISO](#) register control bits. The switches are not connected as long as VTR not present (< [VTRIP](#)). Figure 24.2 illustrates the control logic for the switches.

The two pairs of SMBus pins (SCLK1/SDAT1, SCLK2/SDAT2) are individually software selectable to connect to the SMBus pins SCLK and SDAT. The selection allows for the two SMBus bus segments to be isolated from the SCLK and SDAT pins, individually connected (one or the other) to the SCLK and SDAT pins or both connected to the SCLK and SDAT pins.

The Vbat POR default value of Runtime Register 6Ah (SMB_ISO) will cause the SMBus Isolation switches to default to be closed at the first VTR power-up after a Vbat POR.

Table 24.2 and Table 24.3 describe the SMBus Isolation Switch Operation. The S1_DEF and S2_DEF bits in the [SMB_ISO](#) register control the default powerup state at VTR POR and are maintained by Vbat. The current flow is controlled by the external signals on the SMB pins. The switch provides a 25ohm maximum resistance to ground.

Table 24.2 SMB Isolation Switch 1 Operation

PWRGD_PS PIN	VTR	SMB_ISO REG		SCLK1/SDAT1 PINS
		S1_SEL	S1_DEF	
0	X	X	X	Isolated
0	0 Volts	X	X	Isolated
0	VTR_POR	'1'	0	Connected (24.1)
0	VTR_POR	'0'	1	Isolated
1	VTR powered	SW write '0'	X	Isolated
1	VTR powered	SW write '1'	X	Connected

Note 24.1 This is the VBAT POR default condition.

Table 24.3 SMB Isolation Switch 2 Operation

PWRGD_PS PIN	VTR	SMB_ISO REG		SCLK2/SDAT2 PINS
		S2_SEL	S2_DEF	
0	X	X	X	Isolated
0	0 Volts	X	X	Isolated
0	VTR_POR	'1'	0	Connected (24.1)
0	VTR_POR	'0'	1	Isolated
1	VTR powered	SW write '0'	X	Isolated
1	VTR powered	SW write '1'	X	Connected

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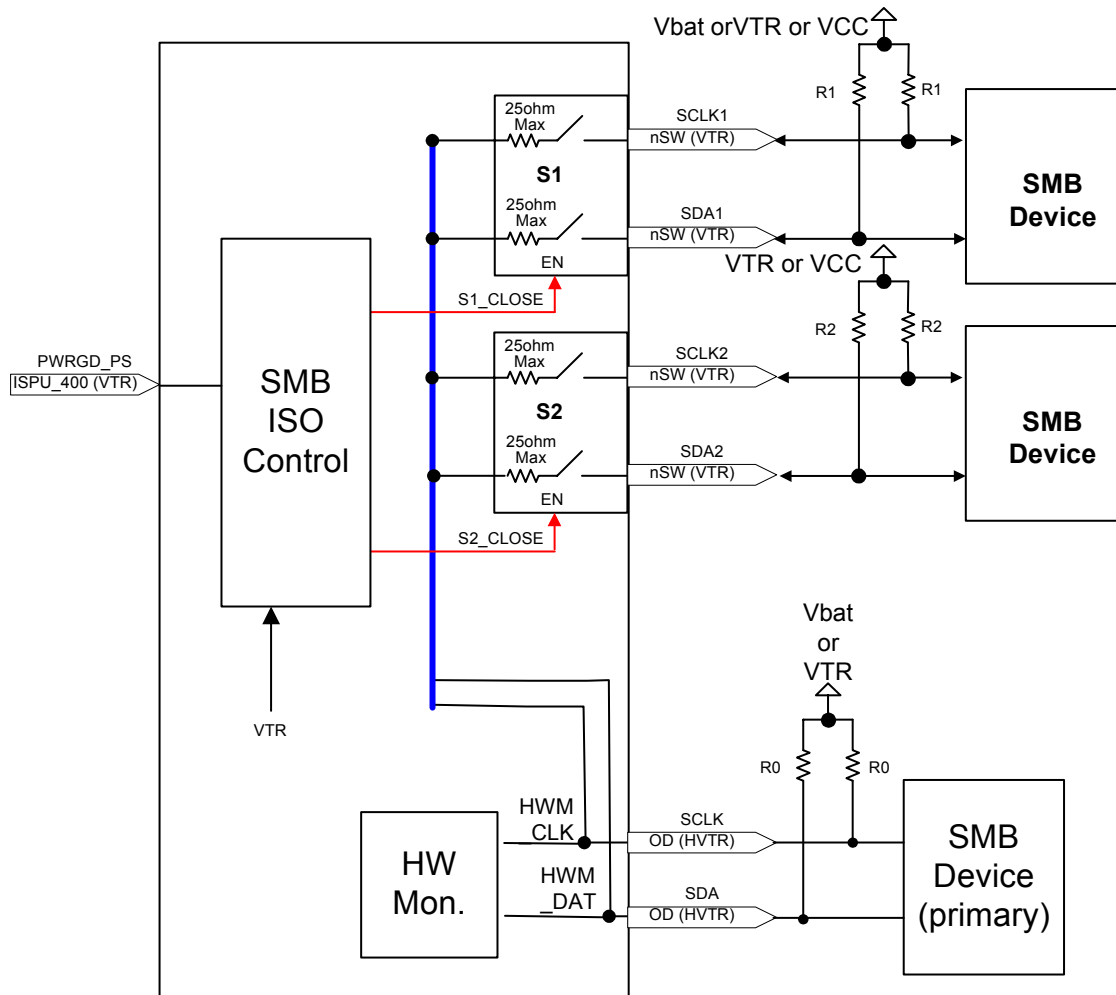
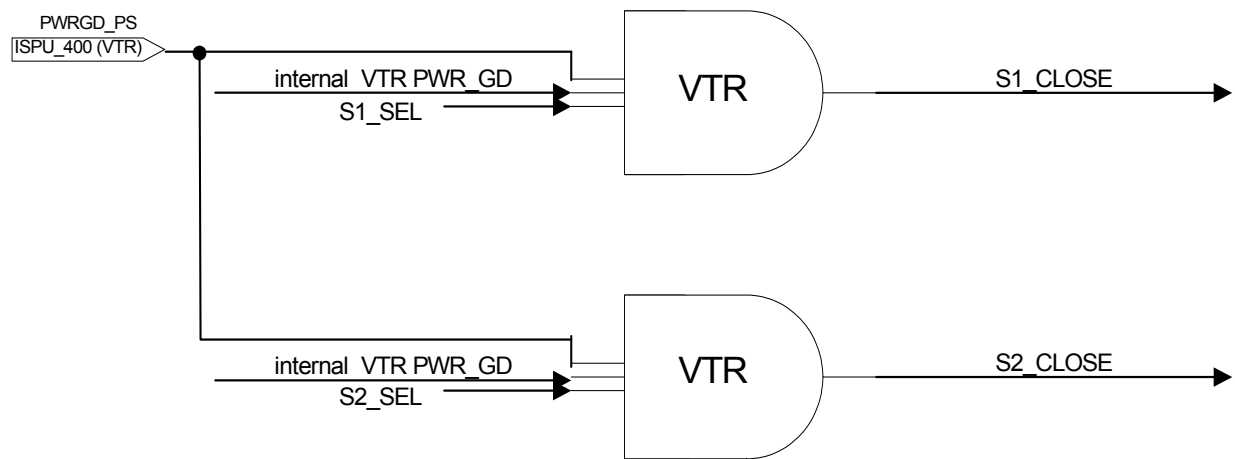


Figure 24.1 SMBus Architecture Using Isolation Circuit

Notes:

- Figure 24.1 and Figure 24.2 are for illustration purposes only and not meant to imply specific implementation details
- The switches are implemented as an n-channel switches that will not pass a full voltage swing. It provides a current path to ground. The board designer should treat each signal pair to the switch as a separate bus with a resistance in the path. The maximum resistance of the switch between any bus to any other bus is 25ohms (when the switch is on). When the switch is off the impedance is Hi-Z and the current is zero. The design requires pull-ups on each of the busses shown above. It is recommended that the pullups be selected so that the total maximum current on each bus does not exceed 2mA to limit the voltage drop across the switch.
- The Hardware Monitor SMBus interface is a slave-only interface. Typically, the SMBus master is connected to the HWM SMBus clock and data pins, although this is not a requirement. This is shown in Figure 24.1 as the primary SMB Device.


Figure 24.2 SMB ISO Control

Chapter 25 Hardware Monitoring

The following sub-sections describe the SCH5017 Hardware Monitoring features.

25.1 Input Monitoring

The SCH5017 device's monitoring function is started by writing a '1' to the START bit in the Ready/Lock/Start Register (0x40). Measured values from the analog inputs and temperature sensors are stored in Reading Registers. The values in the reading registers can be accessed via the SMBus interface. These values are compared to the programmed limits in the Limit Register. The out-of-limit and diode fault conditions are stored in the Interrupt Status Registers.

Note: All limit and parameter registers must be set before the START bit is set to '1'. Once the start bit is set, these registers become read-only.

25.2 Resetting the SCH5017

25.2.1 VTR Power On Reset

All the registers in the Hardware Monitor Block, except the reading registers, reset to a default value when VTR power is first applied to the block. The default state of the register is shown in the Register Summary Table located in [Chapter 27, "Hardware Monitoring Register Set," on page 229](#). The default state of Reading Registers are not shown because these registers have indeterminate power on values.

Note: Usually the first action after power up is to write limits into the Limit Registers.

25.2.2 VCC Power On Reset

The Hardware Monitoring logic uses the PWRGD_PS signal from the SIO logic to indicate when a VCC POR has occurred. When the PWRGD_PS signal is low the hardware monitoring logic is held in reset. When the PWRGD_PS signal is asserted high the logic is enabled and some of the registers and bits are reset to their default values. The following is a list of the registers and bits reset on a VCC POR.

- FANTACH Reading Registers 1-6 at locations 28h-2Fh, A9h-ACh
- Bit[1] LOCK of the Ready/LOCK/START register at offset 40h
- Interrupt Status Registers 1-3 at locations 41h, 42h, and 83h.
- Bit[3] TRDY of the Configuration register at offset 7Fh.
- Bit[0] START of the Ready/Lock/Start register at offset 40h if START_Default bit, which is located in the same register, is enabled.

Notes:

- The START bit in the Ready/Lock/Start register may be reset by VTR only or by VTR and VCC depending on the setting of the START_Default bit located in the same register. See [Section 27.2.11, "Register 40h: Ready/Lock/Start Monitoring," on page 239](#) where the START_default bit is defined.
- When VCC is off the PWM pins are held low. When a VCC POR occurs the state of the PWM pins will be determined by the configuration of the registers. On the first power cycle, following a VTR POR, the fans will be set to full on.

25.2.3 Soft Reset (Initialization)

Setting bit 7 of [Register 7Fh: Configuration Register on page 256](#) performs a soft reset on all the Hardware Monitoring registers except the reading registers. This bit is self-clearing.

25.3 Monitoring Modes

The Hardware Monitor Block supports two Monitoring modes: Continuous Mode and Cycle Mode. These modes are selected using bit 1 of [Register 7Ch: Special Function Register on page 254](#). The following subsections contain a description of these monitoring modes.

The hardware monitor conversion clock is 45KHz $\pm$ 10%. Temperature conversions take 96 clocks, each (2.133ms nom.); voltage conversions take 68 clocks, each (1.511ms nom). The time to complete a conversion cycle depends upon the number of inputs in the conversion sequence to be measured (see [Table 25.3, "ADC Conversion Sequence," on page 193](#)) and the amount of averaging per input, which is selected using the AVG[2:0] bits in the Special Function register (see [Register 7Ch: Special Function Register on page 254](#)).

For each mode, there are four options for the number of measurements that are averaged for each temperature and voltage reading. These options are selected using bits[7:5] of [Register 7Ch: Special Function Register on page 254](#). These bits are defined as follows:

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the measurements that are performed by the hardware monitor before the reading registers are updated ([Table 25.1](#)). The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

Table 25.1 AVG[2:0] BIT DECODER

SFTR[7:5]			MEASUREMENTS PER READING			
AVG2	AVG1	AVG0	REMOTE DIODE 1	REMOTE DIODE 2	INTERNAL DIODE	ALL VOLTAGE READINGS (+5VTR, +5V, +12V, VCCP, VTR, VBAT (IF ENABLED), AND VCC)
0	0	0	128	128	8	8
0	0	1	16	16	1	1
0	1	X	16	16	16	16
1	X	X	32	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

To calculate conversion cycle timing for a given averaging mode:

- Compute total number of temperature conversions (TEMP_CONV)
- Compute total number of voltage conversions (VOLT_CONV)
- Calculate Time to complete all conversions is:

$$\text{Total Conversion Time} = (\text{TEMP_CONV}) * 96 / (45\text{kHz} \pm 10\%) + (\text{VOLT_CONV}) * 68 / (45\text{kHz} \pm 10\%)$$

Example: To calculate the nominal (default) conversion time FOR AVG[2:0] = 001b.

$$\text{Total Conversion Time} = (\text{TEMP_CONV}) * 96 / (45\text{kHz}) + (\text{VOLT_CONV}) * 68 / (45\text{kHz})$$

$$\text{Total Conversion Time} = (16 + 16 + 1) * 96 / (45\text{kHz}) + (6 * 1) * 68 / (45\text{kHz})$$

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Total Conversion Time = (33)*2.133ms+ (6)*1.511ms = ~79ms

[Table 25.2](#) illustrates the min., nom., and max. conversion cycle timing for each of the four averaging modes, with and without the Vbat Monitoring Enable bit set.

Table 25.2 Conversion Cycle Timing

VBAT MONITORING ENABLE BIT	AVG[2:0]	TOTAL TEMPERATURE CONVERSIONS	TOTAL VOLTAGE CONVERSIONS	CONVERSION CYCLE TIME (MSEC)		
				MIN.	NOM.	MAX.
0	000	(2x128)+(1x8)=264	6x8=48	578	636	706
0	001	(2x16)+(1x1)=33	6x1=6	72	79	88
0 (default)	01X (default)	3x16=48	6x16=96	225	247	275
0	1XX	3x32=96	6x32=192	450	495	550
1	000	(2x128)+(1x8)=264	7x8=56	589	648	720
1	001	(2x16)+(1x1)=33	7x1=7	74	81	90
1	01X	3x16=48	7x16=112	247	272	302
1	1XX	3x32=96	7x32=224	494	543	604

Notes:

- The hardware monitor conversion clock is 45KHz $\pm$ 10%.
- Temperature conversions take 96 clocks, each (2.133ms nom.); Voltage conversions take 68 clocks, each (1.511ms nom).

25.3.1 Continuous Monitoring Mode

In the continuous monitoring mode, the sampling and conversion process is performed continuously for each voltage and temperature reading after the Start bit is set high. The time for each voltage and temperature reading is shown above for each measurement option.

The continuous monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the START bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown below (see [Table 25.3](#)). Sampling of all values occurs in a nominal 247 ms (default - see [Table 25.2](#)).

Table 25.3 ADC Conversion Sequence

SAMPLING ORDER	REGISTER
1	Remote Diode Temp Reading 1
2	Ambient Temperature reading
3	VCC reading
4	+12V reading
5	+5V reading
6	VTR Voltage
7	Vbat Voltage (Note 25.1)

Table 25.3 ADC Conversion Sequence (continued)

SAMPLING ORDER	REGISTER
8	Vccp (processor) reading
9	Remote Diode Temp Reading 2
10	+5VTR reading

Note 25.1 The Vbat input is only evaluated when the Vbat Monitoring Enable bit is set. (See [Monitoring Vbat on page 194](#))

When the continuous monitoring function is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 247 ms (default - see [Table 25.2](#)). Each measured value is compared to values stored in the Limit registers. When the measured value violates the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See [Auto Fan Control Operating Mode on page 208](#).

The results of the sampling and conversions can be found in the Reading Registers and are available at any time.

25.3.2 Cycle Monitoring Mode

In cycle monitoring mode, the part completes all sampling and conversions, then waits approximately one second to repeat the process. It repeats the sampling and conversion process typically every 1.2 seconds (1.4 sec max - default averaging enabled). The sampling and conversion of each voltage and temperature reading is performed once every monitoring cycle. This is a power saving mode.

The cycle monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a "round robin" sampling of the inputs, in the order shown above.

When the cycle monitoring function is started, it cycles through each measurement in sequence, and it produces a converted voltage and temperature reading for each input. The state machine waits approximately one second before repeating this process. Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled [Auto Fan Control Operating Mode on page 208](#).

The results of each sampling and conversion can be found in the Reading Registers and are available at any time, however, they are only updated once per conversion cycle.

25.4 Monitoring Vbat

The Vbat input is different than the other voltage inputs in that it is only monitored when the Vbat Monitoring Enable bit is set, which is located in the Ready/Lock/Start register at offset 40h.

Note: There is no DC loading when the Vbat input is not being monitored or when the HVTR power well is Off.

Following a HVTR POR, the Vbat Monitoring Enable bit will be '0' and the START bit will be '0'. When the START bit is '0' the device is not monitoring. When the START bit is set to '1' the hardware monitor begins monitoring the thermal and voltage inputs in a Round Robin algorithm. Once the device is monitoring, the Vbat input will only be monitored when the Vbat Monitoring Enable bit is set to '1'. If the Vbat Monitoring Enable bit is '0' the state machine controlling the ADC Mux will skip the Vbat input. This has the following result:

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- If Vbat Monitoring Enable bit is set to 0 there are a total of 9 active inputs to the ADC (3 temperature and 6 voltage)
- If Vbat Monitoring Enable bit is set to 1 there are a total of 10 active inputs to the ADC (3 temperature and 7 voltage)

Note: See [Table 25.2, "Conversion Cycle Timing,"](#) on page 193.

When the hardware writes a new value to the Vbat Reading Register the Vbat Monitoring Enable will be cleared. The following is a definition of the Vbat Monitoring Enable bit.

Vbat Monitoring Enable bit

The Vbat Monitoring Enable bit determines if Vbat will be monitored on the next available monitoring cycle.

This is a read/write bit. Writing this bit to a '1' will enable monitoring of the Vbat input for one monitoring cycle. Writing this bit to a '0' has no effect. This bit is cleared on an HVTR POR or when the Vbat Reading register is updated. Software can poll this bit for a '0' after setting it to a '1' to determine when the Vbat Reading register has been updated.

0=Vbat input is not being monitored (default)

1=Vbat input is being monitored

APPLICATION NOTE: The Vbat Monitoring Enable bit can be polled to determine when the VBAT reading register is updated with the current battery measurement. When this bit is written to '1' by the software and subsequently cleared to '0' by the hardware, the VBAT reading register contains the updated value.

The Vbat monitoring input is only enabled as a 3.3V input when HVTR is powered and the Vbat Monitoring Enable bit is set to '1'. Once a Vbat measurement is taken, the Vbat monitoring logic is disabled. When the Vbat Monitoring logic is enabled, the Vbat reading register will return a reading value, where C0h (3/4 full scale) represents 3.3V.

The Vbat monitoring enable signal is asserted only during the period of time that Vbat is being monitored. This signal is disabled when the remaining temperature and voltage inputs are being monitored, thereby reducing the current drain on the battery. See [DC Electrical Characteristics on page 321](#) for the average and peak Vbat Current ratings for the SCH5017.

25.5 Interrupt Status Registers

The Hardware Monitor Block contains three interrupt status registers:

- [Register 41h: Interrupt Status Register 1 on page 241](#)
- [Register 42h: Interrupt Status Register 2 on page 242](#)
- [Register 83h: Interrupt Status Register 3 on page 259](#)

These registers are used to reflect the state of all temperature, voltage and fan violation of limit error conditions and diode fault conditions that the Hardware Monitor Block monitors.

When an error occurs during the conversion cycle, its corresponding bit is set (if enabled and not masked) in its respective interrupt status register. The bit remains set until the register is read by software, at which time the bit will be cleared to '0' if the associated error event no longer violates the limit conditions or if the diode fault condition no longer exists. Reading the register will not cause a bit to be cleared if the source of the status bit remains active.

These registers are read only – a write to these registers has no effect. These registers default to 0x00 on VCC POR and Initialization.

See the description of the Interrupt Status registers in [Chapter 27, "Hardware Monitoring Register Set,"](#) on page 229.

The following sections define the Interrupt Enable Bits and the Interrupt Masking Bits. Setting or clearing these bits affects the operation of the Interrupt Status bits.

25.5.1 Interrupt Enable Bits

Each interrupt event can be enabled into the interrupt status registers. See the figure below for the status and enable bits used to control the interrupt bits and nHWM_INT pin. Note that a status bit will not be set if the individual enable bit is not set.

The following is a list of the Interrupt Enable registers:

- [Register 7Eh: Interrupt Enable 1 Register on page 255](#)
- [Register 80h: Interrupt Enable 2 Register on page 257](#)
- [Register 82h: Interrupt Enable 3 Register on page 258](#)

Note: Clearing the individual enable bits will clear the corresponding individual status bit.

Clearing the individual enable bits. There are two cases and in both cases it is not possible to change the individual interrupt enable while the start bit is set.

1. The interrupt status bit will never be set when the individual interrupt enable is cleared. Here the interrupt status bit will not get set when you set the start bit. Regardless of whether the limits are violated during a measurement.
2. An interrupt status bit had been set from a previous condition. So you clear the start bit and then clear the individual interrupt enable. The associated interrupts status bit will not be cleared immediately, but will be cleared when the start bit is set when the associated reading register is updated.

25.5.2 Interrupt Masking Bits

Each voltage interrupt event can be masked when the system enters a Sleep S3. Masking an interrupt prevents the corresponding status bit from being set when the voltage violates the limits if the system is in an S3 sleep state. See [Table 25.1, "Interrupt Control," on page 197](#) for how the masking bits effect the status and enable bits used to control the interrupt bits and nHWM_INT pin. The Sleep S3 masking bits are located in [Register A0h: SLP_S3# INT Mask Register on page 264](#).

Since VTR will power the H/W Monitoring block, it may be desired to prevent unwanted or false interrupts when the system enters a sleep state (S3). When entering the S3 sleep state, selected power supplies are turned off intentionally. Normally, software would be required to disable the corresponding voltage monitoring interrupts before the system turns these power supplies off. In SCH5017, the hardware has the ability to Mask Interrupts in the Sleep S3 state. The hardware uses a combination of the masking bits and the SLP_S3# and SLP_S5# pins to determine when the status bits should be prevented from being set.

The interrupt masking register is: SLP_S3# INT Mask Register.

- The SLP_S3# INT Mask Register is used to prevent selected individual voltage status bits that are enabled from being set when the SLP_S3# pin is low and the SLP_S5# is high.

The following table shows the state of the SLP_S3# and SLP_S5# pins in the various sleep states.

SIGNAL NAME	S1	S3	S4/S5
SLP_S3#	High	Low	Low
SLP_S5#	High	High	Low

Note: If a voltage Mask bit is enabled (set to '1') in the SLP_S3# INT Mask Register and the SLP_S3# pin is low and the SLP_S5# pin is high, the corresponding status bit will not be set by a voltage event, regardless of the individual enable bit's setting.

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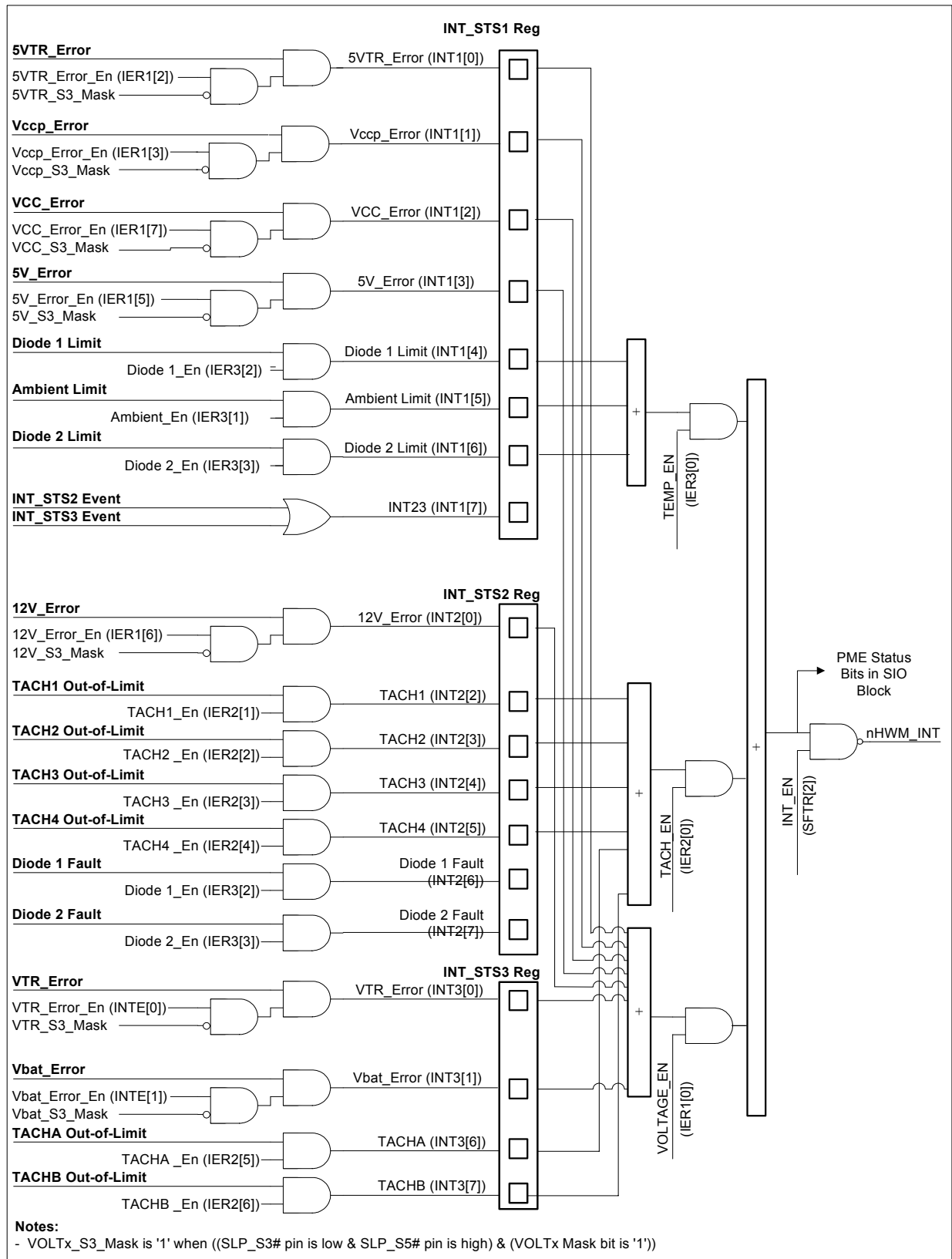


Figure 25.1 Interrupt Control

Note: The diode fault bits are not mapped directly to the nHWM_INT pin. A diode fault condition forces the diode reading register to a value of 80h, which will generate a Diode Error condition. See section [Diode Fault on page 198](#).

25.5.3 Diode Fault

The SCH5017 Chip automatically sets the associated diode fault bit to 1 when any of the following conditions occur on the Remote Diode pins:

- The positive and negative terminal are an open circuit.
- Positive terminal is connected to VCC
- Positive terminal is connected to ground
- Negative terminal is connected to VCC
- Negative terminal is connected to ground

The occurrence of a fault will cause 80h to be loaded into the associated reading register, except for the case when the negative terminal is connected to ground. A temperature reading of 80h will cause the corresponding diode error bit to be set. This will cause the nHWM_INT pin to become active if the individual, group (TEMP), and global enable (INTEN) bits are set.

Notes:

- The individual remote diode enable bits and the TEMP bit are located in [Register 7Eh: Interrupt Enable 1 Register on page 255](#). The INTEN bit is located in bit[2] of [Register 7Ch: Special Function Register on page 254](#).
- When 80h is loaded into the Remote Diode Reading Register the PWM output(s) controlled by the zone associated with that diode input will be forced to full on. See [Thermal Zones on page 202](#).

If the diode is disabled, the fault bit in the interrupt status register will not be set. In this case, the occurrence of a fault will cause 00h to be loaded into the associated reading register. The limits must be programmed accordingly to prevent unwanted fan speed changes based on this temperature reading. If the diode is disabled and a fault condition does not exist on the diode pins, then the associated reading register will contain a “valid” reading (e.g. a reading that is not produced by a fault condition).

25.6 Interrupt Signal

The hardware monitoring interrupt signal, which is used to indicate out-of-limit temperature, voltage events, and/or fan errors, can be generated via a dedicated pin (nHWM_INT) or through PME Status bits located in the Runtime Register block.

To enable temperature event, voltage events and/or fan events onto the nHWM_INT pin or the PME status bits the following group enable bits must be set:

- To enable out-of-limit temperature events set bit[0] of the Interrupt Enable 3 (TEMP) register (82h) to ‘1’.
- To enable out-of-limit voltage events set bit[0] of the Interrupt Enable 1(VOLT) register (7Eh) to ‘1’
- To enable Fan tachometer error events set bit[0] of the Interrupt Enable 2(Fan Tachs) register (80h) to ‘1’.

25.6.1 Interrupt Pin (nHWM_INT)

The nHWM_INT function is used as an interrupt output for out-of-limit temperature, voltage events, and/or fan errors.

- The nHWM_INT signal is located on a dedicated pin.
- To enable the interrupt pin to go active, set bit 2 of the Special Function Register (7Ch) to ‘1’.

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Note: If the nHWM_INT pin is not enabled the pin will be tristate.

See [Figure 25.1 on page 197](#). The following description assumes that the interrupt enable bits for all events are set to enable the interrupt status bits to be set and no events are being masked.

If the internal or remote temperature reading violates the low or high temperature limits, nHWM_INT will be forced active low (if all the corresponding enable bits are set: individual enable bits (D1_EN, D2_EN, and/or AMB_EN), group enable bit (TEMP_EN) and the global enable bit (INTEN)). This pin will remain low while the Internal Temp Error bit or one or both of the Remote Temp Error bits in Interrupt Status 1 Register is set and the corresponding enable bit(s) are set.

The nHWM_INT pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding diode error bit to be set. This will cause the nHWM_INT pin to become active if enabled.

The nHWM_INT pin can be enabled to indicate out-of-limit voltages. Bit[0] of the Interrupt Enable 1(VOLT) register (7Eh) is used to enable this option. When this bit is set, if one or more of the voltage readings violates the low or high limits, nHWM_INT will be forced active low (if all the corresponding enable bits are set: individual enable bits (see [Register 7Eh: Interrupt Enable 1 Register on page 255](#) and [Register 82h: Interrupt Enable 3 Register on page 258](#)), group enable (VOLT_EN), and global enable (INT_EN)). This pin will remain low while the associated voltage error bit in the Interrupt Status Register 1 or Interrupt Status Register 2 is set.

The nHWM_INT pin can be enabled to indicate fan errors. Bit[0] of the Interrupt Enable 2 (Fan Tachs) register (80h) is a Tach group enable and is used to enable this option for all the tachs. Each tach also has an individual enable bit (see [Register 80h: Interrupt Enable 2 Register on page 257](#)). This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The nHWM_INT pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the nHWM_INT pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to '1' again.

The nHWM_INT pin can also be deasserted by issuing an Alert Response Address Call. See the description in the section titled [SMBus Alert Response Address on page 184](#).

The nHWM_INT pin may only become active while the monitor block is operational.

25.6.2 Interrupt as a PME event

The hardware monitoring interrupt signal is routed to the SIO PME block. For a description of these bits see the section defining PME events. This signal is unaffected by the nHWM_INT pin enable (See [Figure 25.1 Interrupt Control on page 197](#).)

The PME status bits are located in the following Runtime Registers located in the SIO block:

- PMES3_STS1 register at offset 04h
- PMES5_STS1 register at offset 0Ch.

When a voltage, temperature, or fan tachometer event causes a status bit to be set, the HW_Monitor PMW status bits will be set as long as the corresponding group enable bit is set.

25.7 Low Power Modes

The Hardware Monitor Block can be placed in a low-power mode by writing a '0' to Bit[0] of the Ready/Lock/Start Register (0x40). The low power mode that is entered is either sleep mode or shutdown mode as selected using Bit[0] of the Special Function Register (7Ch). These modes do not reset any of the registers of the Hardware Monitor Block. In both of these modes, the PWM pins are at 100% duty cycle.

Table 25.4 Low Power Mode Control Bits

START	LPMD	DESCRIPTION
0	0	Sleep Mode
0	1	Shutdown Mode
1	x	Monitoring

Notes:

- START and LPMD bits cannot be modified when the LOCK bit is set.
- START bit is located in the Ready/Lock/Start register (40h). LPMD bit is located in the Special Function Register (7Ch)
- All Limit and Parameter registers must be set before the START bit is set to '1'. Once the start bit is set, these registers become read-only.

25.7.1 Sleep Mode

This is a low power mode in which bias currents are on and the 90kHz clock source is on, but the A/D converter and monitoring cycle are turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

25.7.2 Shutdown Mode

This is a low power mode in which bias currents are off, the 90kHz clock source is off, and the A/D converter and monitoring cycle are turned off. Serial communication is only possible with Bits[2:0] of the Special Function Register at 7Ch and Bits [7:0] of the Configuration Register at 7Fh, which become write-only registers in this mode.

25.8 Analog Voltage Measurement

The Hardware Monitor Block contains inputs for directly monitoring the power supplies (+12 V, +5 V, +5VTR, +Vccp, Vbat, VTR, and VCC). These inputs are scaled internally to an internal reference source, converted via an 8 bit successive approximation register ADC (Analog-to-Digital Converter), and scaled such that the correct value refers to 3/4 scale or 192 decimal (except the Vccp and Vbat inputs). This removes the need for external resistor dividers and allows for a more accurate means of measurement since the voltages are referenced to a known value. Since any of these inputs can be above VCC or below Ground, they are not diode protected to the power rails. The measured values are stored in the Reading registers and compared with the Limit registers. The status bits in the Interrupt Status Register 1 and 2 are set if the measured values violate the programmed limits.

The Vccp voltage input measures the processor voltage, which will lie in the range of 0V to 3.0V.

The Vbat voltage input measures the battery voltage (only when enabled), which is a nominal 3V input.

The following table shows the values of the analog inputs that correspond to the min and max output codes of the A/D converter. For a complete list of the ADC conversions see [Appendix A, "ADC Voltage Conversion," on page 353](#).

Table 25.5 Min/Max ADC Conversion Table

INPUT VOLTAGE	+12V	+5V (Note 25.2)	+3.3V (Note 25.3)	+VCCP
Min Value (Corresponds to A/D output 00000000)	<0.062	<0.026	<0.017	<0.012
Max Value (Corresponds to A/D output 11111111)	>15.938	>6.640	>4.383	>2.988

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Note 25.2 The device supports monitoring of a +5V main power supply input and a +5VTR Standby Power supply input. These inputs are nominal +5V inputs

Note 25.3 This device supports monitoring of the SIO VCC, VTR, and Vbat power supplies. These analog inputs are nominal +3.3V analog inputs. The SIO VCC and VTR power supplies are nominal 3.3V power supplies. The Vbat power supply is a nominal 3V power supply.

25.9 Voltage ID

VID0-VID5 digital inputs are used to store processor Voltage ID codes (for processor operating voltage) in the [Register 43h: VID on page 243](#). These VIDs can be read out by the management system using the SMBus interface.

25.10 Temperature Measurement

Temperatures are measured internally by bandgap temperature sensor and externally using two sets of diode sensor pins (for measuring two external temperatures). See subsections below.

Note: The temperature sensing circuitry for the two remote diode sensors is calibrated for a 3904 type diode.

25.10.1 Internal Temperature Measurement

Internal temperature can be measured by bandgap temperature sensor. The measurement is converted into digital format by internal ADC. This data is converted in two's complement format since both negative and positive temperature can be measured. This value is stored in Internal Temperature Reading register (26h) and compared to the Temperature Limit registers (50h – 51h). If this value violates the programmed limits in the Internal High Temperature Limit register (51h) and the Internal Low Temperature Limit register (50h) the corresponding status bit in Interrupt Status Register 1 is set.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See the section titled [Auto Fan Control Operating Mode on page 208](#).

25.10.2 External Temperature Measurement

The Hardware Monitor Block also provides a way to measure two external temperatures using diode sensor pins (Remote x+ and Remote x-). The value is stored in the register (25h) for Remote1+ and Remote1- pins. The value is stored in the Remote Temperature Reading register (27h) for Remote2+ and Remote2- pins. If these values violate the programmed limits in the associated limit registers, then the corresponding Remote Diode 1 (D1) or Remote Diode 2 (D2) status bits will be set in the Interrupt Status Register 1.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See [Auto Fan Control Operating Mode on page 208](#).

There are Remote Diode (1 or 2) Fault status bits in Interrupt Status Register 2 (42h), which, when one, indicate a short or open-circuit on remote thermal diode inputs (Remote x+ and Remote x-). Before a remote diode conversion is updated, the status of the remote diode is checked. In the case of a short or open-circuit on the remote thermal diode inputs, the value in the corresponding reading register will be forced to 80h. Note that this will cause the associated remote diode limit exceeded status bit to be set (i.e. Remote Diode x Limit Error bits (D1 and D2) are located in the Interrupt Status Register 1 at register address 41h).

The temperature change is computed by measuring the change in Vbe at two different operating points of the diode to which the Remote x+ and Remote x- pins are connected. But accuracy of the measurement also depends on non-ideality factor of the process the diode is manufactured on.

25.10.3 Temperature Data Format

Temperature data can be read from the three temperature registers:

- Internal Temp Reading register (26h)
- Remote Diode 1 Temp Reading register (25h)
- Remote Diode 2 Temp Reading register (27h)

The following table shows several examples of the format of the temperature digital data, represented by an 8-bit, two's complement word with an LSB equal to 1.0 °C.

Table 25.6 Temperature Data Format

Temperature	Reading (dec)	Reading (hex)	Digital Output
-127°C	-127	81h	1000 0001
⋮	⋮	⋮	⋮
-50 °C	-50	CEh	1100 1110
⋮	⋮	⋮	⋮
-25 °C	-25	E7h	1110 0111
⋮	⋮	⋮	⋮
-1 °C	-1	FFh	1111 1111
0 °C	0	00h	0000 0000
+1 °C	1	01h	0000 0001
⋮	⋮	⋮	⋮
+25 °C	25	19h	0001 1001
⋮	⋮	⋮	⋮
+50°C	50	32h	0011 0010
⋮	⋮	⋮	⋮
+127°C	127	7Fh	0111 1111
SENSOR ERROR	128	80h	1000 0000

25.11 Thermal Zones

Each temperature measurement input is assigned to a Thermal Zone to control the PWM outputs in Auto Fan Control mode. These zone assignments are as follows:

- Zone 1 = Remote Diode 1 (Processor) or Remote Diode 2
- Zone 2 = Ambient Temperature Sensor or Remote Diode 2
- Zone 3 = Remote Diode 2

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Bit[1] of the Configuration register at offset 7Fh is used to select either the Ambient Temperature Sensor (default) or Remote Diode 2 as the thermal input for Zone 2. The auto fan control logic uses the zone temperature reading to control the duty cycle of the PWM outputs. The following is a definition of the Zone 2 Select bit.

Bit[1] Zone 2 Select

0= Zone 2 is controlled by Ambient Temperature Sensor (default)

1= Zone 2 is controlled by Remote Diode 2

Zone 1 Select

Bit [3] in the Special Function register is used to select either Remote Diode 1 or Remote Diode 2 as the source for the Zone 1 Reading value.

Bit[3] Zone 1 Select

This bit controls the temperature sensor for Zone 1 as it pertains to the auto fan control. This bit has no effect on the Remote Diode 1 or Remote Diode 2 sensor status events.

0= Zone 1 is controlled by Remote Diode 1 (default)

1= Zone 1 is controlled by Remote Diode 2

See [Section 26.1.7.4, "Zone Selection,"](#) on page 214.



Chapter 26 Fan Control

The following sections describe the various fan control and monitoring modes in the part.

This Fan Control device is capable of driving multiple DC fans via five PWM outputs and monitoring up to six fans equipped with tachometer outputs. All the PWM outputs control a fan by generating an 8-bit duty cycle at a programmed frequency. All the PWM outputs support both low frequency and high frequency PWMs. The low frequency range is from 11.0Hz to 87.7Hz and the high frequency range is from 15kHz to 30kHz. The six pins dedicated to monitoring the operation of each fan are the FANTACH[1:4, A:B] pins. Fans equipped with Fan Tachometer outputs may be connected to these pins to monitor the speed of the fan.

PWM1, PWM2, and PWM3 may be associated with any or all of FANTACHs 1-4. These PWMs are capable of operating in Manual Mode or Auto Mode. FANTACHS1-4 may monitor the fans in Mode 1 or Mode 2. Mode 1 requires that the fan always generates a valid tach pulse and Mode 2 only monitors the associated FANTACH(s) when the PWM is ON.

PWMA and PWMB may operate in Manual Mode only. PWMA is associated with FANTACHA and PWMB is associated with FANTACHB. FANTACHS A and B are implemented as a TACH Pulse Counter (TPC). These tach inputs use a small, low frequency sampling pulse to monitor the tach inputs. These sampling pulses allow the device to get accurate tach measurements without inducing noise into the system or effecting the speed of the fans. These tach inputs are capable of monitoring fans driven by the associated PWM outputs or fans controlled externally. The TPC monitoring logic returns a tach reading in tach pulses per update rate. This value is easily converted to Rotations per Minute (RPM). The reading can also enable a Mode 1 legacy feature that converts the reading to a 16-bit value that has the same form as FANTACHs 1-4. This allows backward compatibility for software designed to monitor FANTACHs 1-4.

26.1 Fan Control for PWMs[1:3] and FANTACHs[1:4]

The following section outlines how to configure and operate PWMs[1:3] and FANTACHs[1:4]. For PWMs[A,B] and FANTACHs[A,B] see [Fan Control for PWMs\[A,B\] and FANTACHs\[A,B\] on page 225](#).

26.1.1 Limit and Configuration Registers

At power up, all the registers are reset to their default values and PWM[1:3] are set to "Fan always on Full" mode. Before initiating the monitoring cycle for either manual or auto mode, the values in the limit and configuration registers should be set.

The limit and configuration registers are:

- Registers 54h – 5Bh: TACHx Minimum
- Registers 5Fh – 61h: Zone x Range/FANx Frequency
- Registers 5Ch – 5Eh: PWMx Configuration
- Registers 62h – 63h: Min/Off, PWM x Ramp Rate Control
- Registers 64h – 66h: PWMx Minimum Duty Cycle
- Registers 67h – 69h: Zone x Low Temp LIMIT (See [Note 26.2 on page 206](#))
- Registers 6Ah – 6Ch: Zone x Temp Absolute Limit – all fans in Auto Mode are set to full
- Register 81h: TACH_PWM Association
- Registers 90h – 93h: Tachx Option Registers
- Registers 94h – 96h: PWMx Option Registers

The limit and configuration registers are defined in [Chapter 27, Hardware Monitoring Register Set](#).

Notes:

Note 26.1 The START bit in Register 40h Ready/Lock/Start Register must be set to '1' to start temperature monitoring functions.

Note 26.2 The three Zone x Low Temp Limit (67h, 68h and 69h) must be written to a value that is not 80h in order for autofan (including manual mode) to operate. If all three Zone x Low Temp Limit (67h, 68h and 69h) are not re-programmed to a value that is not 80h, autofan will not operate and the fans will be full-on (100% duty cycle).

Note 26.3 Setting the PWM Configuration register to Auto Mode will not take effect until after the START bit is set

26.1.2 PWM Operation Following a Power Cycle

26.1.2.1 VTR Power-On Reset

All the HWM registers will retain their value through a sleep cycle unless otherwise specified. All the hardware monitoring registers are reset to their default values following a VTR POR and a few registers and bits are reset to their default values following a VCC POR. See [Section 25.2, "Resetting the SCH5017," on page 191](#).

Note: Usually the first action after power up is to write limits into the Limit Registers.

Following an AC power failure, the START bit is '0' and the PWM pins go to a 100% duty cycle when PWRGD_PS goes active after VCC comes up. Also see [Note 26.2 on page 206](#).

26.1.2.2 VCC Power-On Reset

Although the hardware monitor is powered by VTR it is only operational when VCC is active. The hardware monitor uses the PWRGD_PS signal to indicate when VCC is valid. When PWRGD_PS is low the PWM pins will be driven low. When the PWRGD_PS signal transitions to the active state, the operation of the PWM pins will be determined by the configuration registers.

If the START bit is '0' following a VCC POR, the PWM pins will be forced to the full on state (100% duty cycle) . If the START bit is '1' the PWM pins will remain low until the temperature registers have been updated with valid readings. The TRDY bit, which is located in Bit[3] of [Register 7Fh: Configuration Register](#), is used to indicate the temperature readings are valid. Once the TRDY bit becomes active the PWM pins will be set to their configured state as determined by the auto fan control logic.

Notes:

- By default, the START bit is only reset by a VTR POR. The START bit may be reset on a VCC POR if bit[5] START_default is set to '1' in [Register 40h: Ready/Lock/Start Monitoring on page 239](#).
- If the auto fan logic determines the fans need to be turned on from the off state, the PWM pins will enter spinup until either the associated tach inputs are operating within the programmed limits or until the spinup time expires, whichever comes first. See [Section 26.1.7, "Spin Up," on page 211](#) for a more detailed description of this operation.

26.1.3 Device Set-Up for PWMs[1:3] and FANTACHS[1:4]

BIOS will follow the steps listed below to configure the fan registers on this device. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the limit and parameter registers during configuration, the SCH5017 will continue to operate based on default values until the Start bit, in the Ready/Lock/Start register, is set. Once the Start bit is set, the SCH5017 will operate according to the values that were set by BIOS in the limit and parameter registers.

1. Set limits and parameters (not necessarily in this order)
 - a. [5F-61h] Set PWM frequencies and Auto Fan Control Range.
 - b. [62-63h] Set Ramp Rate Control and min/off

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- c. [5C-5Eh] Set the fan spin-up delays.
- d. [5C-5Eh] Match each PWM output with a corresponding thermal zone.
- e. [67-69h] Set the zone temperature low limits. (See [Note 26.2 on page 206](#))
- f. [6A-6Ch] Set the zone temperature absolute limits.
- g. [64-66h] Set the PWM minimum duty cycle.
- h. [81h] Associate a Tachometer input to a PWM output Register
- i. [90-93h] Select the TACH Mode of operation (Mode 1 or Mode 2)
- j. [90-93h] Set the number of edges per tach reading
- k. [90-93h] Set the ignore first 3 edges of tach input bit
- l. [90-93h] Set the SLOW bit if tach reading should indicate slow fan event as FFFEh and stalled fan event as FFFFh.
- m. [94-96h] Set the TACH Reading Update rate
- n. [94-96h] Set the tach reading guard time (Mode 2 Only)
- o. [94-96h] Set the TACH reading logic for Opportunistic Mode (Mode 2 Only)
- p. [94-96h] Set the SZEN bit, which determines if the PWM output will ramp to Off or jump to Off.
2. [40h] Set bit 0 (Start) to start monitoring.
3. [40h] Set bit 1 (Lock) to lock the limit and parameter registers (optional)

26.1.4 PWM Fan Speed Control

Note: The following description applies to PWM1, PWM2, and PWM3.

The PWM outputs are held low when the PWRGD_PS input is low. When PWRGD_PS transitions to the high state, the PWM is released and allowed to operate as configured. Note that there is an option to force a spinup when the PWRGD_PS signal transitions on. See [Spin Up on page 211](#).

The PWM pin reflects a duty cycle that is determined based on 256 PWM duty cycle intervals. The minimum duty cycle is “off”, when the pin is low, or “full on” when the pin is high for 255 intervals and low for 1 interval. The INVERT bit (bit 4 of the PWMx Configuration registers at 80h-82h) can be used to invert the PWM output, however, the default operation (following a VCC POR) of the part is based on the PWM pin active high to turn the fans “on”. When the INVERT bit is set, as long as power is not removed from the part, the inversion of the pin will apply thereafter.

When describing the operation of the PWMs, the terms “Full on” and “100% duty cycle” means that the PWM output will be high for 255 clocks and low for 1 clock (INVERT bit = 0). One exception to this is during fan spin-up when the PWM pin will be forced high for the duration of the spin-up time.

The PWM pins go to 100% duty cycle under the following conditions:

- Setting the OVERRIDE bit (register 40h, bit 3) to 1, forces all PWMs go to 100% (pin is high)
- During Spinup: each PWM goes to 100% duty cycle for the duration of spinup (pin is high). Note that spinup reduction may reduce the programmed spinup time.
- The START bit is ‘0’ (pin is high).
- The START bit is 1 and the TRDY bit (register 0E8h bit 3) is 0 (pin is high). The TRDY bit will go to 1 upon completion of an update cycle. That is, the PWMs stay at the selected duty cycle until all temperature reading registers have been updated once.
- If the temperature of a sensor exceeds its absolute temperature, all PWMs go to 100% (pin is high for 255 clocks and low for 1 clock). Note that for this to occur, the zone must be associated to a PWM and configured to control the PWM in auto mode. The PWM pins will go to 100% immediately upon a zone exceeding its absolute temperature, however, when the zone drops below its absolute temperature, ramp rate control will apply for all PWMs. See [Section 26.1.7.6, "Ramp Rate Control Logic," on page 216](#).
- For a temperature reading of 80h, the associated PWM pin will go to 100% (pin is high for 255 clocks and low for 1 clock). Note 80h is an error condition representing a diode fault.

- Max PWM set to FFh (pin is high for 255 clocks and low for 1 clock).

26.1.4.1 VTR Power-On Reset PWM Operation

Following an AC power failure, the START bit is '0' and the PWM pins go to 100% duty cycle when PWRGD_PS goes active after VCC comes up. Also see [Note 26.2 on page 206](#).

26.1.4.2 VCC Power-On Reset PWM Operation

The PWM pins are held low when the PWRGD_PS input is low.

For a main power cycle (return from sleep state), if the START bit has not been cleared by software, then when PWRGD_PS transitions to the high state, the PWM pins are released from being clamped low and are allowed to operate as configured. If configured for autofan mode, the device automatically adjusts the PWM duty cycle based on temperature.

APPLICATION NOTE: The START bit is only reset on VTR POR. So when VCC goes down, the START bit will remain set. This ensures that autofan remains active following reboots. When power is restored, the spinup sequence is completed, and then autofan speed control becomes active.

26.1.5 Manual Fan Control Operating Mode (Test Mode)

When operating in Manual Fan Control Operating Mode, software controls the speed of the fans by directly programming the PWM duty cycle. The operation of the fans can be monitored based on reading the temperature and tachometer reading registers and/or by polling the interrupt status registers. The SCH5017 offers the option of generating an interrupt indicated by the nHWM_INT signal located on the PWM2 and FANTACH3 pins.

To control the PWM outputs in manual mode:

- To set the mode to operate in manual mode, write '111' to bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWMx Configuration.
- The speed of the fan is controlled by the duty cycle set for that PWM output. The duty cycle must be programmed in Registers 30h-32h: Current PWM Duty

To monitor the fans:

Fans equipped with Tachometer outputs can be monitored via the FANTACHx input pins. See [Section 26.1.9, "Fan Speed Monitoring," on page 219](#).

If an out-of-limit condition occurs, the corresponding status bit will be set in the Interrupt Status registers. Setting this status bit will generate an interrupt signal on the nHWM_INT pin (if enabled). Software must handle the interrupt condition and modify the operation of the device accordingly. Software can evaluate the operation of the Fan Control device through the Temperature and Fan Tachometer Reading registers.

When in manual mode, the current PWM duty cycle registers can be written to adjust the speed of the fans, when the start bit is set. These registers are not writable when the lock bit is set.

Note: The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

26.1.6 Auto Fan Control Operating Mode

The SCH5017 implements automatic fan control. In Auto Fan Mode, this device automatically adjusts the PWM duty cycle of the PWM outputs, according to the flow chart on the following page (see [Figure 26.1 Automatic Fan Control Flow Diagram on page 209](#)).

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PWM outputs are assigned to a thermal zone based on the PWMx Configuration registers (see [Section 25.11, "Thermal Zones," on page 202](#)). It is possible to have more than one PWM output assigned to a thermal zone. For example, PWM outputs 2 and 3, connected to two chassis fans, may both be controlled by thermal zone 2. At any time, if the temperature of a zone exceeds its absolute limit, all PWM outputs go to 100% duty cycle to provide maximum cooling to the system (except those fans that are disabled or in manual mode).

It is possible to have a single fan controlled by multiple zones, turning on when either zone requires cooling based on its individual settings.

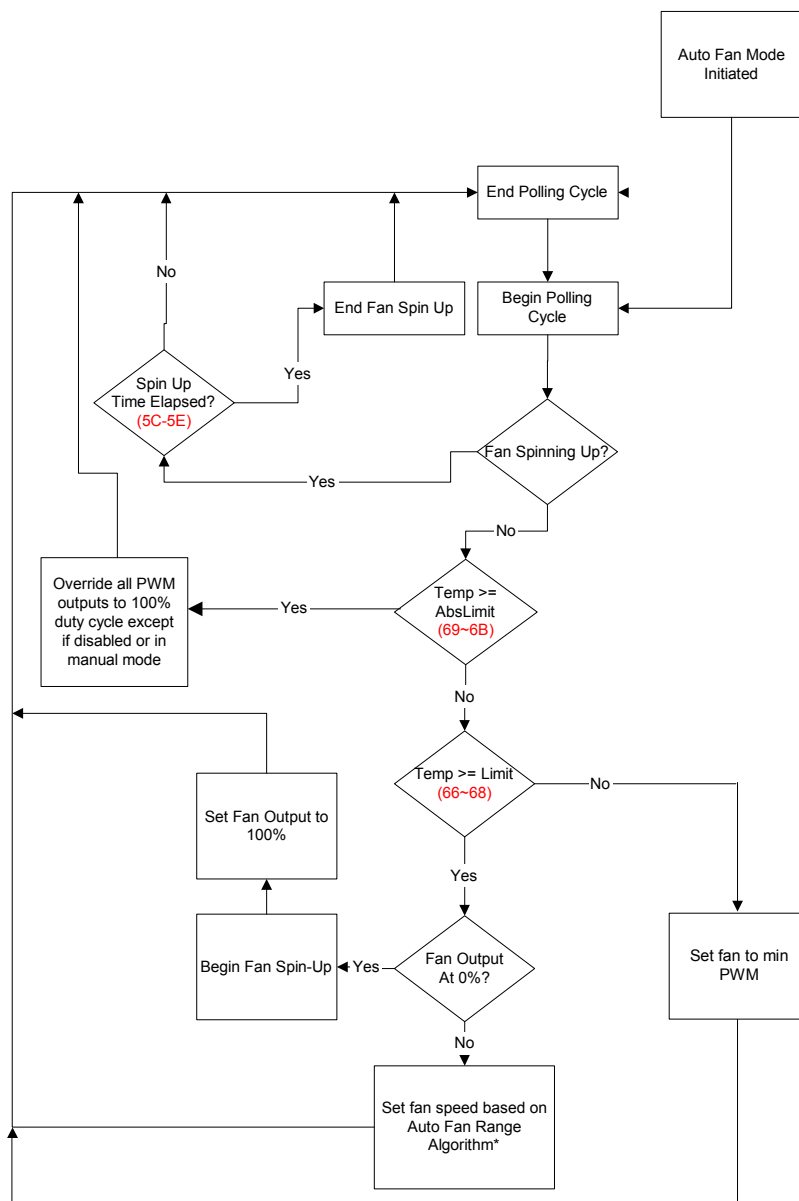


Figure 26.1 Automatic Fan Control Flow Diagram

*See [Registers 5C-5Eh: PWM Configuration on page 246](#) for details.

When in Auto Fan Control Operating Mode the hardware controls the fans directly based on monitoring of temperature and speed.

To control the fans, there are several parameters that must be programmed.

Set the minimum temperature that will turn the fans on. This value is programmed in Registers 67h-69h: Zone x Low Temp Limit (Auto Fan Mode Only). See [Note 26.2 on page 206](#).

Note:

The speed of the fan is controlled by the duty cycle set for that device. The duty cycle for the minimum fan speed must be programmed in Registers 64h-66h: PWMx Minimum Duty Cycle. This value corresponds to the speed of the fan when the temperature reading is equal to the minimum temperature LIMIT setting. As the actual temperature increases and is above the Zone LIMIT temperature and below the Absolute Temperature Limit, the PWM will be determined by a linear function based on the Auto Fan Speed Range bits in Registers 5Fh-61h.

Set the absolute temperature for each zone in Registers 6Ah-6Ch: Zone x Temp Absolute Limit (Auto Fan Mode only). If the actual temperature is equal to or exceeds the absolute temperature in one or more of the associated zones, all Fans operating in auto mode will be set to Full on, regardless of which zone they are operating in (except those that are disabled or configured for Manual Mode). Note: fans can be disabled via the PWMx Configuration registers and the absolute temperature safety feature can be disabled by writing 80h into the Zone x Temp Absolute Limit registers.

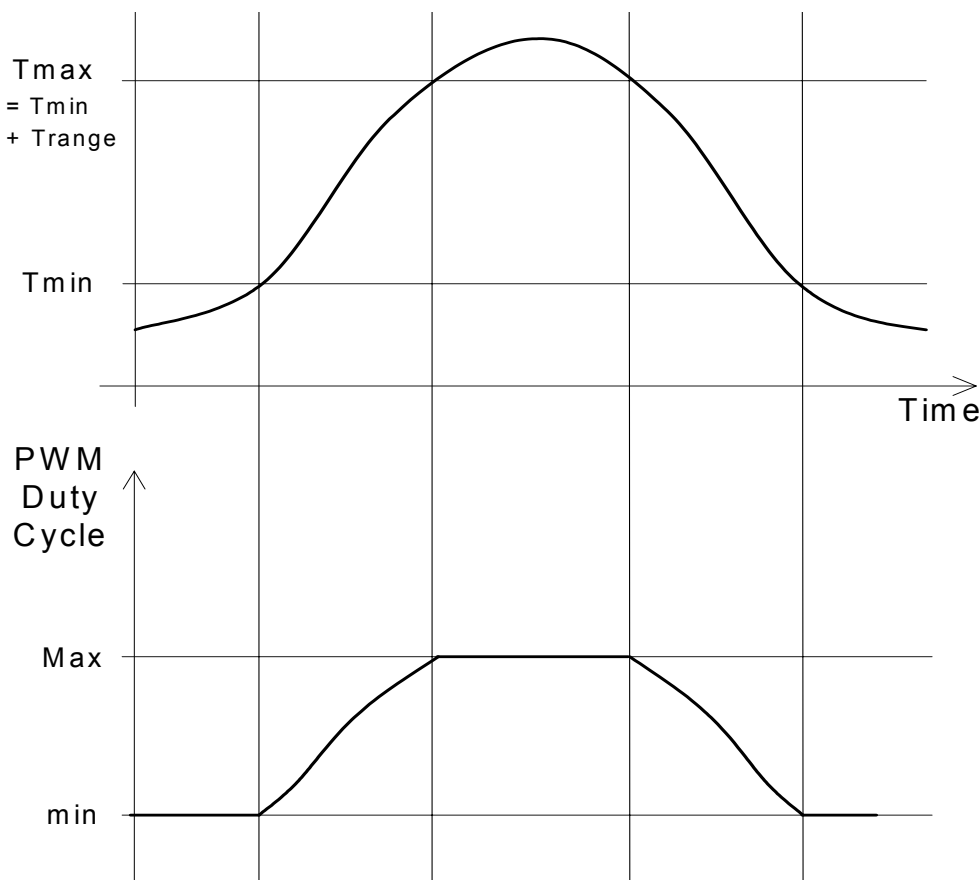
To set the mode to operate in auto mode, set Bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: PWM Configuration Bits[7:5]='000' for PWM on Zone 1; Bits[7:5]='001' for PWM on Zone 2; Bits[7:5]='010' for PWM on Zone 3. If the "Hottest" option is chosen (101 or 110), then the PWM output is controlled by the zone that results in the highest PWM duty cycle value.

Notes:

- Software can be alerted of an out-of-limit condition by the nHWM_INT pin if an event status bit is set and the event is enabled and the interrupt function is enabled onto the nHWM_INT pin.
- Software can monitor the operation of the Fans through the Fan Tachometer Reading registers and by the PWM x Current PWM duty registers. It can also monitor current temperature readings through the Temperature Limit Registers if hardware monitoring is enabled.
- Fan control in auto mode is implemented without any input from external processor.

In auto "Zone" mode, the speed is adjusted automatically as shown in the figure below. Fans are assigned to a zone(s). It is possible to have more than one fan assigned to a thermal zone or to have multiple zones assigned to one fan.

[Figure 26.2 on page 211](#) shows the control for the auto fan algorithm. The part allows a minimum temperature to be set, below which the fan will run at minimum speed. The minimum speed is programmed in the PWMx Minimum Duty cycle registers (64h-66h) and may be zero. A temperature range is specified over which the part will automatically adjust the fan speed. The fan will go to a duty cycle computed by the auto fan algorithm. As the temperature rises, the duty cycle will increase until the fan is running at full-speed when the temperature reaches the minimum plus the range value. The effect of this is a temperature feedback loop, which will cause the temperature to reach equilibrium between the minimum temperature and the minimum temperature plus the range. Provided that the fan has adequate cooling capacity for all environmental and power dissipation conditions, this system will maintain the temperature within acceptable limits, while allowing the fan to run slower (and quieter) when less cooling is required.

Datasheet**Figure 26.2 Automatic Fan Control****26.1.7 Spin Up**

When a fan is being started from a stationary state (PWM duty cycle = 00h), the part will cause the fan to “spin up” by going to 100% duty cycle for a programmable amount of time to overcome the inertia of the fan (i.e., to get the fan turning). Following this spin up time, the fan will go to the duty cycle computed by the auto fan algorithm.

During spin-up, the PWM duty cycle is reported as 0%.

26.1.7.1 Spinup Reduction

To limit the spin-up time and thereby reduce fan noise, the part uses feedback from the tachometers to determine when each fan has started spinning properly. The following tachometer feedback is included into the auto fan algorithm during spin-up.

Auto Fan operation during Spin Up:

The PWM goes to 100% duty cycle until the tachometer reading register is below the minimum limit (see [Figure 26.3](#)), or the spin-up time expires, whichever comes first. This causes spin-up to continue until the tachometer enters the valid count range, unless the spin up time expires. If the spin up expires before the tachometer enters the valid range, an interrupt status bit will be set once spin-up expires. Note that more than one tachometer may be associated with a PWM, in which case all tachometers associated with a PWM must be in the valid range for spin-up to end.

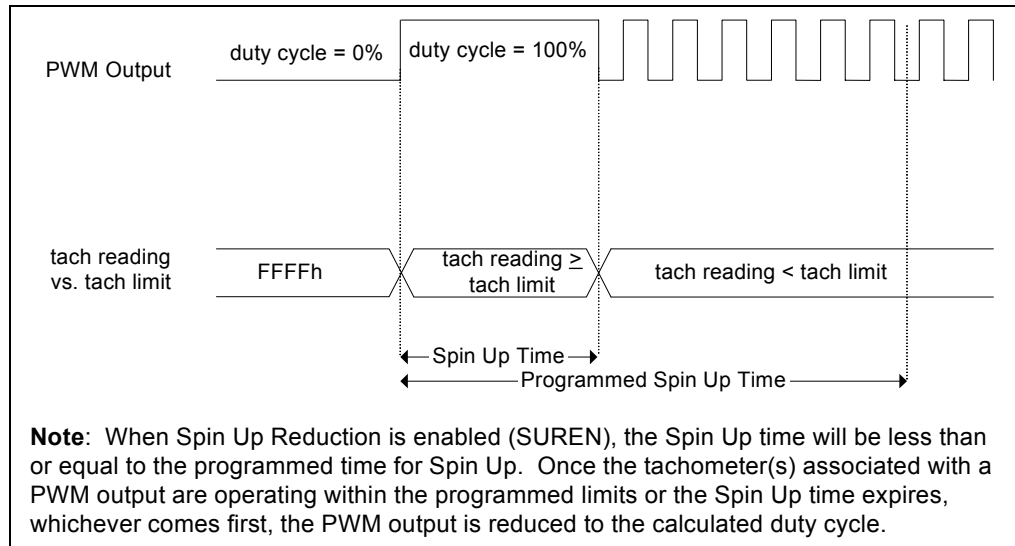


Figure 26.3 Spin Up Reduction Enabled

This feature defaults to enabled; it can be disabled by clearing bit 4 of the Configuration register (7Fh). If disabled, the all fans go to 100% duty cycle for the duration of their associated spin up time. Note that the Tachometer x minimum registers must be programmed to a value less than FFFFh in order for the spin up reduction to work properly.

Notes:

- The tachometer reading register always gives the actual reading of the tachometer input.
- No interrupt bits are set during spin-up.

26.1.7.2 Spinup After Main Power Cycle (PWRGD_PS)

Spinup is a feature of the auto fan control mode. Any time the PWM pin transitions from a 0% duty cycle to a non zero duty cycle the PWM pin will be forced high for the duration of spinup or until the fan are spinning within normal operating parameters as determined by the Tach Limit registers. See [Spin Up on page 211](#) for a more detailed description of spinup. This feature can also be initiated by the PWRGD_PS signal transitioning high following a main (VCC) power cycle if the TRDY bit is set to one before the PWM Clamp is released.

To ensure this device will operate with a variety of fans, there is a programmable bit to determine if the START bit gets reset to its default value on a VCC POR or VTR POR. By default, the START bit is reset on a VTR POR.

[Figure 26.4](#) and [Figure 26.5](#) show the operation of the PWMs after a VCC POR when the START bit is 0, and when it is 1.

Note: The following cases assume the OVRID bit in the Ready/Lock/Start register (40h) is set to 0.

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Case 1: PWM Operation Following PWRGD_PS Active after VTR POR.
START bit = 0.

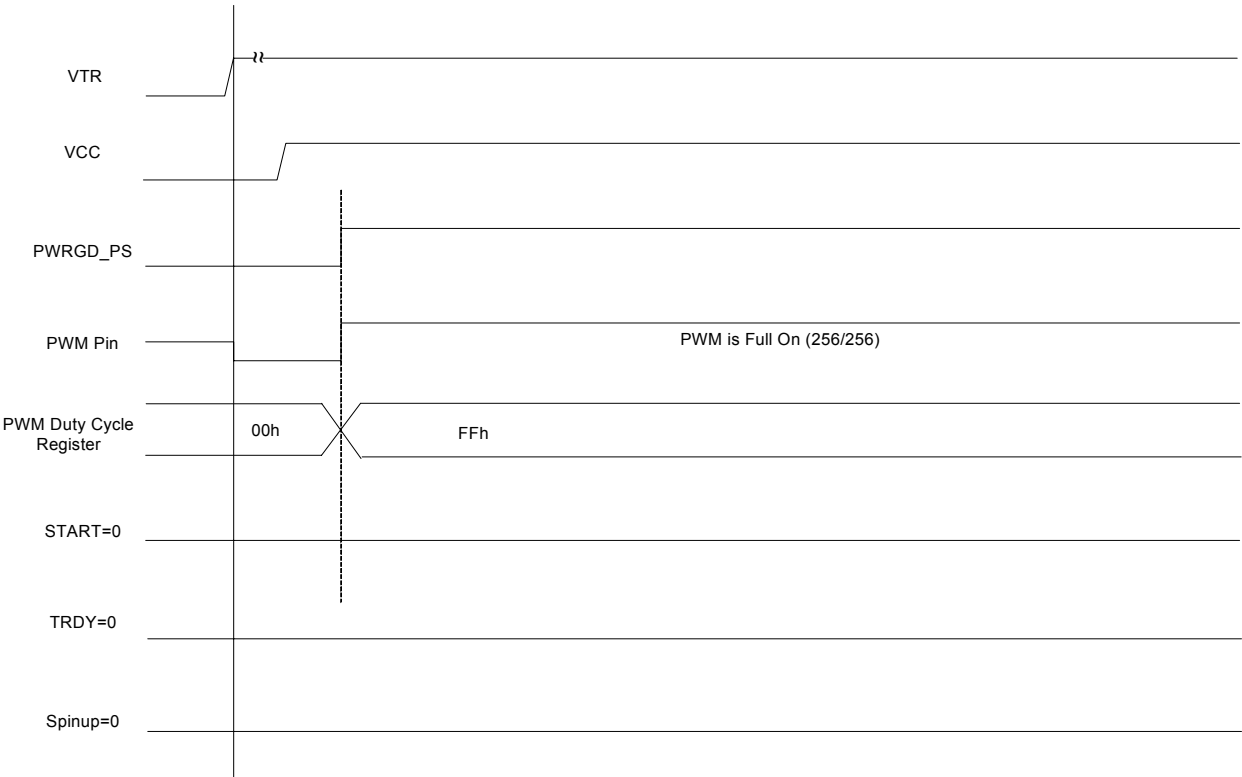


Figure 26.4 PWM Operation Following a VCC POR (START=0)

**Case 2: PWM Operation Following PWRGD_PS Active after VCC POR Only.
START bit = 1.**

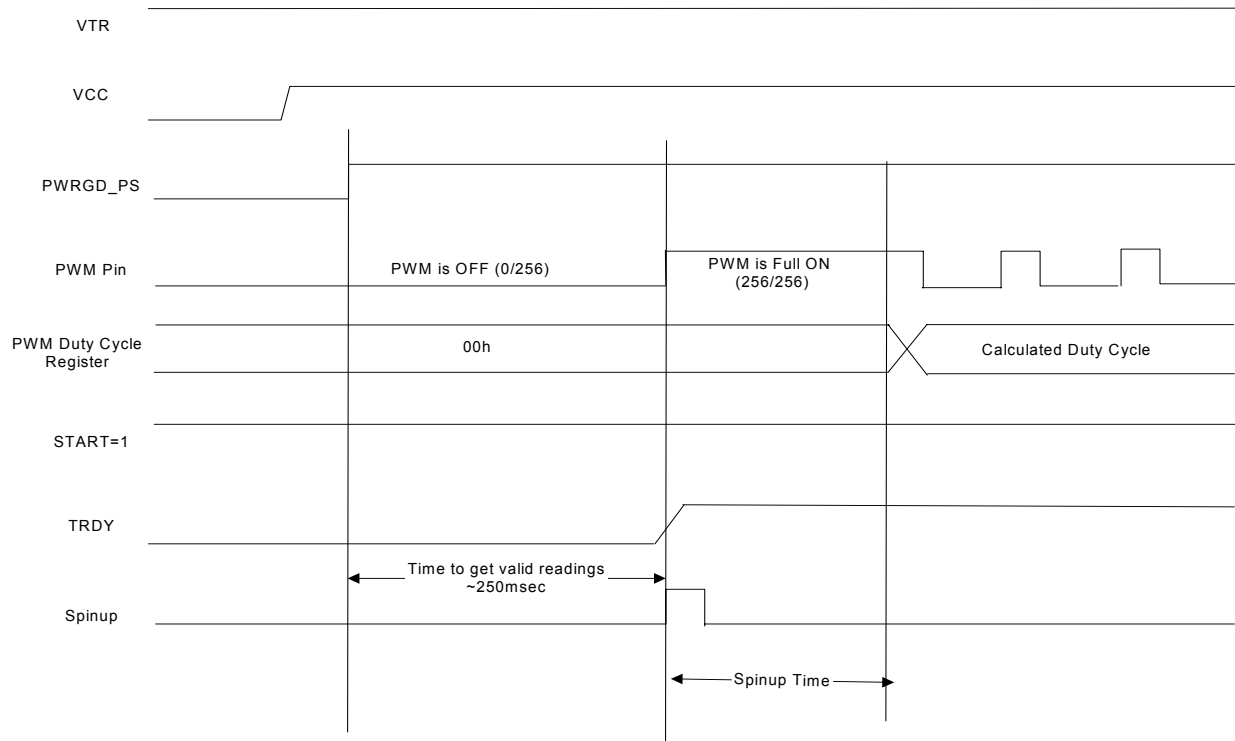


Figure 26.5 PWM Operation Following a VCC POR (START=1)

26.1.7.3 Hottest Option

If the “Hottest” option is chosen (101 or 110), then the fan is controlled by the limits and parameters associated with the zone that requires the highest PWM duty cycle value, as calculated by the auto fan algorithm.

26.1.7.4 Zone Selection

In SCH5017, the zones may be assigned in the following manner:

- Zone 1 = Remote Diode 1 or Remote Diode 2
- Zone 2 = Ambient Temperature Sensor or Remote Diode 2
- Zone 3 = Remote Diode 2

These options allow the two or three different fan control characteristic curves to be defined for one temperature by programming different parameters for two or three different zones, with the same temperature input (remote diode 2).

26.1.7.5 Two and Three Piece Linear Fan Function

A 2-piece [Linear Fan Function](#) can be approximated using the hottest of zones 2 and 3 option in combination with the Zone 2 Select bit.

Note: The ambient temperature is not used for autofan control in this case.

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The Hottest of Zones option is used to achieve the 2-piece linear function. If the PWM is controlled by multiple zones, the duty cycle is computed for each zone and the zone that produces the greatest duty cycle is used to control the PWM output.

The Zone 2 Select bit is used to determine the thermal input used for the Zone 2 reading. Zone 2 may be linked to Remote Diode 2 or the Ambient Temperature. Note that once Zone 2 is configured it applies for all the PWM outputs.

The Zone 2 Select bit is set to cause the remote diode 2 temperature reading to be used as the Zone 2 input temperature.

In [Figure 26.6](#), the first line is the PWM duty cycle for the PWM if it is controlled by Zone 2 only. The second line shows the PWM duty cycle for the PWM if it is controlled by Zone 3 only. If the hottest of zones 2 & 3 option is selected then the resulting PWM duty cycle will be the shaded region on the lines. Notice that the hottest option always selects the zone that produces the greatest duty cycle.

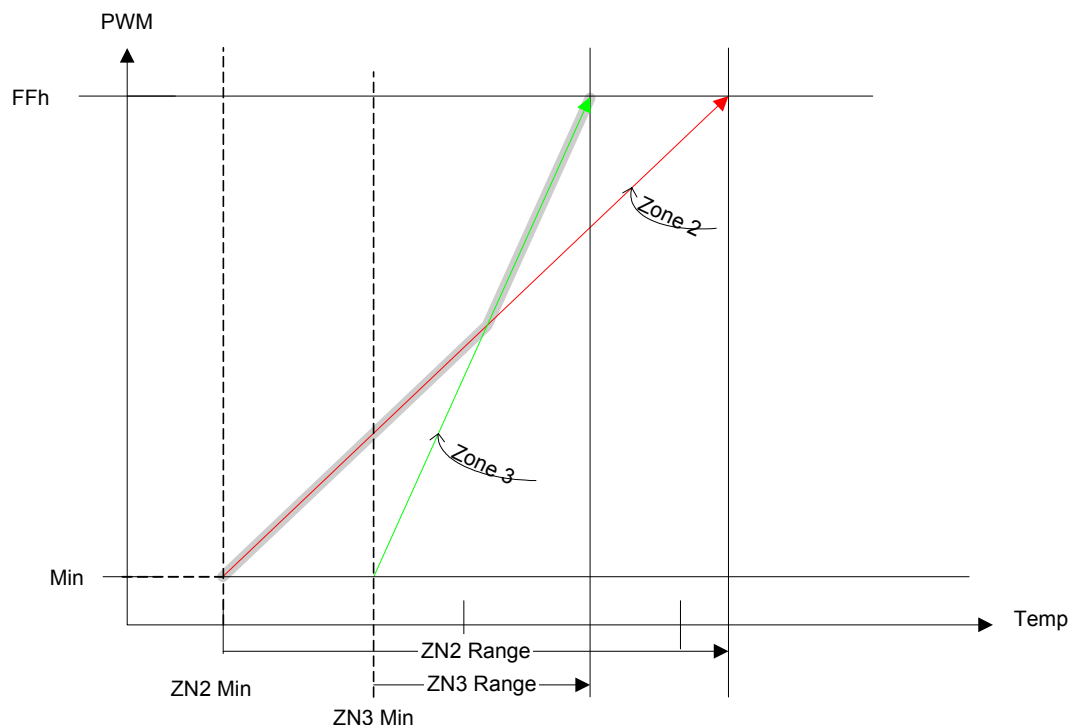


Figure 26.6 Two-piece linear function

A 3-piece [Linear Fan Function](#) can be approximated using the hottest of zones 1, 2 and 3 option in combination with the Zone 1 and Zone 2 Select bits.

Note: The remote diode 1 and the ambient temperature are not used for autofan control in this case.

The Zone 2 Select bit is set to cause the remote diode 2 temperature reading to be used as the Zone 2 input temperature. The Zone 1 Select bit is set to cause the remote diode 2 temperature reading to be used as the Zone 1 input temperature.

In [Figure 26.7](#), the first line is the PWM duty cycle for the PWM if it is controlled by Zone 1 only. The second line shows the PWM duty cycle for the PWM if it is controlled by Zone 2 only. The third line shows the PWM duty cycle for the PWM if it is controlled by Zone 3 only. If the hottest of zones 1, 2 & 3 option is selected then the resulting PWM duty cycle will be the shaded region on the lines. Notice that the hottest option always selects the zone that produces the greatest duty cycle.

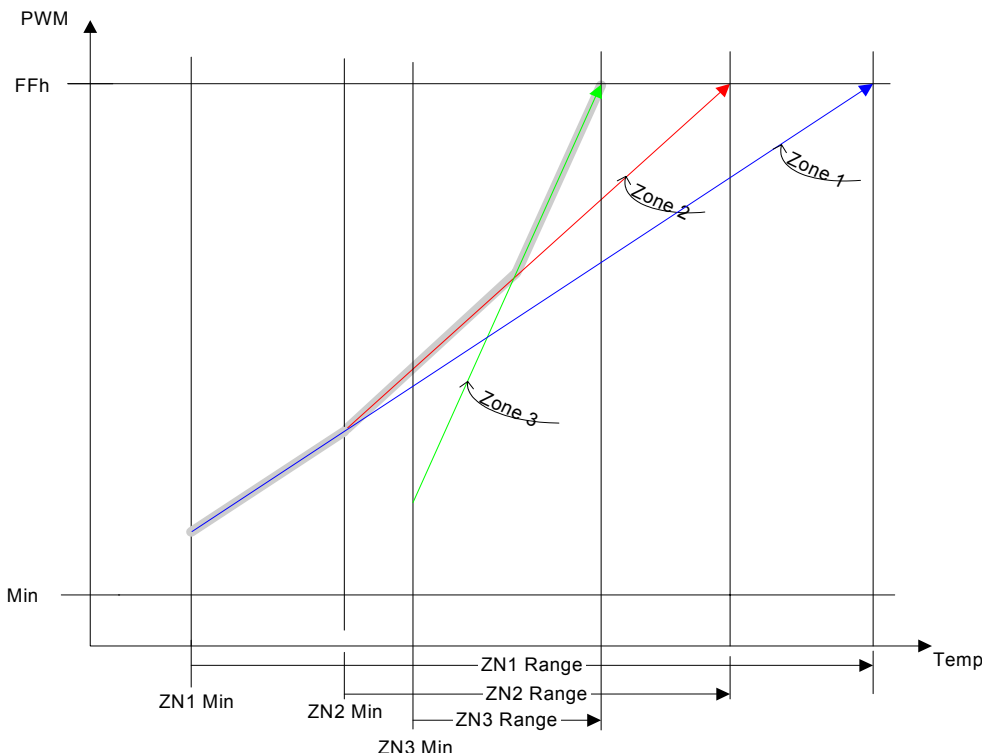


Figure 26.7 Three-piece linear function

Notes: For the two or three piece linear function:

- Max PWM is fixed at FFh
- Min PWM is programmable
- Each zone has four temperature attributes that are unique to the zone (not the PWM)
 - Zone Reading
 - Zone Low Limit
 - Zone Absolute Limit
 - Zone Range
- Zone 1, Zone 2 and Zone 3 may have different attributes.

26.1.7.6 Ramp Rate Control Logic

The Ramp Rate Control Logic, if enabled, limits the amount of change in the PWM duty cycle over a specified period of time. This period of time is programmable in the Ramp Rate Control registers located at offsets 62h and 63h.

RAMP RATE CONTROL DISABLED: (DEFAULT)

The Auto Fan Control logic determines the duty cycle for a particular temperature. If PWM Ramp Rate Control is disabled, the PWM output will be set to this calculated duty cycle.

RAMP RATE CONTROL ENABLED:

If PWM Ramp Rate Control is enabled, the PWM duty cycle will Ramp up or down to the new duty cycle computed by the auto fan control logic at the programmed Ramp Rate. The PWM Ramp Rate Control logic compares the current duty cycle computed by the auto fan logic with the previous ramp rate duty cycle. If the current duty cycle is greater than the previous ramp rate duty cycle the ramp

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rate duty cycle is incremented by '1' at the programmed ramp rate until it is greater than or equal to the current calculated duty cycle. If the current duty cycle is less than the previous ramp rate duty cycle, the ramp rate duty cycle is decremented by '1' until it is less than or equal to the current duty cycle. If the current PWM duty cycle is equal to the calculated duty cycle the PWM output will remain unchanged.

Internally, the PWM Ramp Rate Control Logic will increment/decrement the internal PWM Duty cycle by '1' at a rate determined by the Ramp Rate Control Register. The actual duty cycle output is changed once per the period of the PWM output, which is determined by the frequency of the PWM output. (See [Figure 26.8 Illustration of PWM Ramp Rate Control on page 218.](#))

- If the period of the PWM output is less than the step size created by the PWM Ramp Rate, the PWM output will hold the duty cycle constant until the Ramp Rate logic increments/decrements the duty cycle by '1' again. For example, if the PWM frequency is 87.7Hz ($1/87.7\text{Hz} = 11.4\text{msec}$) and the PWM Step time is 206msec, the PWM duty cycle will be held constant for a minimum of 18 periods ($206/11.4 = 18.07$) until the Ramp Logic increments/decrements the actual PWM duty cycle by '1'.
- If the period of the PWM output is greater than the step size created by the PWM Ramp Rate, the ramp rate logic will force the PWM output to increment/decrement the actual duty cycle in increments larger than $1/255$. For example, if the PWM frequency is 11Hz ($1/11\text{Hz} = 90.9\text{msec}$) and the PWM Step time is 5msec, the PWM duty cycle output will be incremented 18 or 19 out of 255 (i.e., $90.9/5 = 18.18$) until it reaches the calculated duty cycle. Note: The step size may be less if the calculated duty cycle minus the actual duty cycle is less than 18.

Note: The calculated PWM Duty cycle reacts immediately to a change in the temperature reading value. The temperature reading value may be updated once in 247msec (default) (see [Table 25.2, "Conversion Cycle Timing," on page 193](#)). The internal PWM duty cycle generated by the Ramp Rate control logic gradually ramps up/down to the calculated duty cycle at a rate pre-determined by the value programmed in the PWM Ramp Rate Control bits. The PWM output latches the internal duty cycle generated by the Ramp Rate Control Block every $1/(\text{PWM frequency})$ seconds to determine the actual duty cycle of the PWM output pin.

PWM Output Transition from OFF to ON

When the calculated PWM Duty cycle generated by the auto fan control logic transitions from the 'OFF' state to the 'ON' state (i.e., Current PWM duty cycle > 00h), the internal PWM duty cycle in the Ramp Rate Control Logic is initialized to the calculated duty cycle without any ramp time and the PWMx Current Duty Cycle register is set to this value. The PWM output will latch the current duty cycle value in the Ramp Rate Control block to control the PWM output.

PWM Output Transition from ON to OFF

Each PWM output has a control bit to determine if the PWM output will transition immediately to the OFF state (default) or if it will gradually step down to Off at the programmed Ramp Rate. These control bits (SZEN) are located in the PWMx Options registers at offsets 94h-96h.

Table 26.1 PWM Ramp Rate

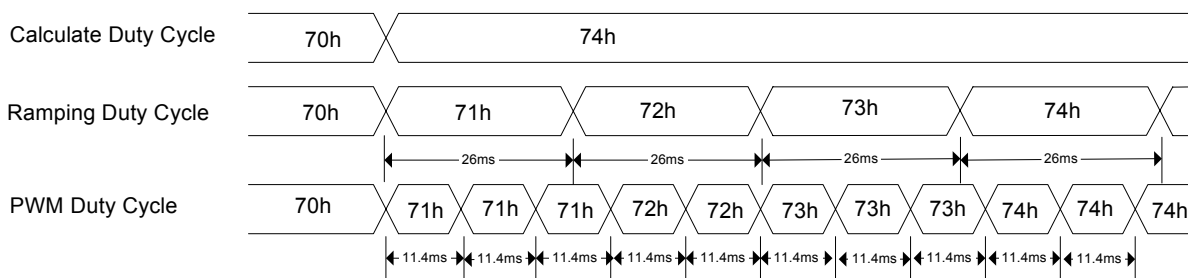
RRX- [2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39

Table 26.1 PWM Ramp Rate (continued)

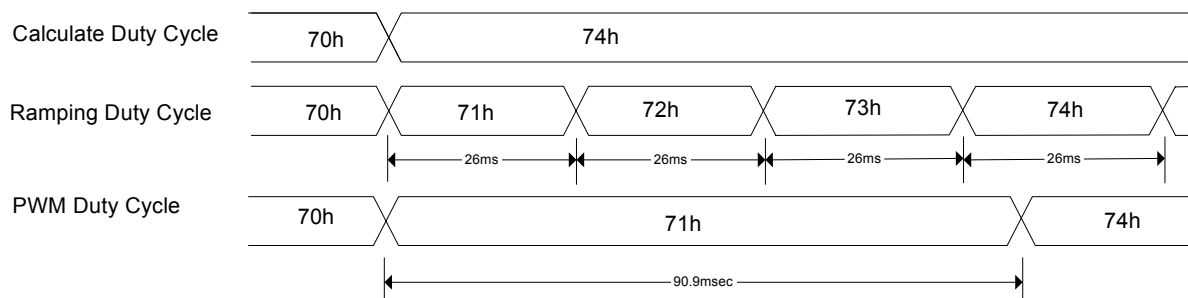
RRX- [2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100
111	0.8	1.275	5 msec	200

Example 1: PWM period < Ramp Rate Step Size

PWM frequency = 87.7Hz (11.4msec) & PWM Ramp Rate = 38.46Hz (26msec)


Example 2: PWM period > Ramp Rate Step Size

PWM frequency = 11Hz (90.9msec) & PWM Ramp Rate = 38.46Hz (26msec)


Figure 26.8 Illustration of PWM Ramp Rate Control
Notes:

- The PWM Duty Cycle latches the Ramping Duty Cycle on the rising edge of the PWM output.
- The calculated duty cycle, ramping duty cycle, and the PWM output duty cycle are asynchronous to each other, but are all synchronized to the internal 90kHz clock source.

It should be noted that the actual duty cycle on the pin is created by the PWM Ramp Rate Control block and latched on the rising edge of the PWM output. Therefore, the current PWM duty cycle may lag the PWM Calculated Duty Cycle.

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26.1.8 PWM Frequencies Supported

The SCH5017 supports low frequency and high frequency PWMs. All the frequencies are derived from the 14.318MHz clock input.

The frequency of the PWM output is determined by the Frequency Select bits[3:0] as shown in [Table 27.9, "PWM Frequency Selection," on page 249](#).

26.1.9 Fan Speed Monitoring

Note: The following description only pertains to FANTACHs[1:4]. See [Fan Control for PWMs\[A,B\] and FANTACHs\[A,B\] on page 225](#) for a description of the Fan Speed Monitoring for FANTACHS A and B.

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the Fan Tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

The tachometers will operate in one of two modes:

- Mode 1: Standard tachometer reading mode. This mode is used when the fan is always powered when the duty cycle is greater than 00h.
- Mode 2: Enhanced tachometer reading mode. This mode is used when the PWM is pulsing the fan.

26.1.9.1 TACH Inputs

The tachometer inputs are implemented as digital input buffers with logic to filter out small glitches on the tach signal.

26.1.9.2 Selecting the Mode of Operation:

The mode is selected through the Mode Select bits located in the Tach Option register. This Mode Select bit is defined as follows:

- 0=Mode 1 (default): Standard tachometer reading mode
- 1=Mode 2: Enhanced tachometer reading mode.

Default Mode of Operation:

- Mode 1
- Slow interrupt disabled (Don't force FFFh)
- Tach interrupt enabled via enable bit
- Tach Limit = FFFFh
- Tach readings updated once a second

26.1.9.3 Mode 1 – Always Monitoring

Mode 1 is the simple case. In this mode, the Fan is always powered when it is 'ON' and the fan tachometer output ALWAYS has a valid output. This mode is typically used if a linear DC Voltage control circuit drives the fan. In this mode, the fan tachometer simply counts the number of 90kHz pulses between the programmed number of edges (default = 5 edges). The fan tachometer reading registers are continuously updated.

The counter is used to determine the period of the Fan Tachometer input pulse. The counter starts counting on the first edge and continues counting until it detects the last edge or until it reaches FFFFh. If the programmed number of edges is detected on or before the counter reaches FFFFh, the reading register is updated with that count value. If the counter reaches FFFFh and no edges were detected a stalled fan event has occurred and the Tach Reading register will be set to FFFFh. If one or more edges are detected, but less than the programmed number of edges, a slow fan event has occurred and the Tach Reading register will be set to either FFFh or FFFFh depending on the state of the Slow

Tach bits located in the TACHx Options registers at offsets 90h - 93h. Software can easily compute the RPM value using the tachometer reading value if it knows the number of edges per revolution.

Notes:

- If the PWM output associated with a tach input is configured for the high frequency option then the tach input must be configured for Mode 1.
- Some enhanced features added to support Mode 2, are available to Mode 1 also. They are: programmable number of tach edges and force tach reading register to FFFEh to indicate a SLOW fan.
- Five edges or two tach pulses are generated per revolution.
- If a tach input is left unconnected it must be configured for Mode 1.

26.1.9.4 Mode 2 –Monitor Tach input When PWM is ‘ON’

Pln this mode, the PWM is used to pulse the Fan motor of a 3-wire fan. 3-wire fans use the same power supply to drive the fan motor and to drive the tachometer output logic. When the PWM is ‘ON’ the fan generates valid tach pulses. When the PWM is not driving the Fan, the tachometer signal is not generated and the tach signal becomes indeterminate or tristate. Therefore, Mode 2 only makes tachometer measurements when the associated PWM is driving high during an update cycle. As a result, the Fan tachometer measurement is “synchronized” to the PWM output, such that it only looks for tach pulses when the PWM is ‘ON’.

Note: Any fan tachometer input may be associated with any PWM output (see [Linking Fan Tachometers to PWMs on page 224](#).)

During an update cycle, if an insufficient number of tachometer pulses are detected during this time period, the following applies: If at least one edge but less than the programmed number of edges is detected, the fan is considered slow. If no edge is detected, the fan is considered stopped.

Notes:

- The interrupt status bits are set, if enabled, to indicate that a slow or stopped fan event has occurred when the tach reading registers are greater than the tach limit registers.
- At some duty cycles, the programmed number of edges will appear during some PWM High times, but not all. If opportunistic mode is enabled, the tach logic will latch the count value any time it detects the programmed number of edges and reset the update counter. (See Bit[5] of [Section 27.2.47, "Registers 94h-96h: PWMx Option Registers," on page 262](#).) An interrupt will only be generated if no valid readings were made during the programmed update time.

ASSUMPTIONS (REFER TO FIGURE 26.9, "PWM AND TACHOMETER CONCEPT"):

The Tachometer pulse generates 5 transitions per fan revolution (i.e., two fan tachometer periods per revolution, edges 2→6). One half of a revolution (one tachometer period) is equivalent to three edges (2→4 or 3→5). One quarter of a revolution (one-half tachometer period) is equivalent to two edges. To obtain the fan speed, count the number of 90Khz pulses that occurs between 2 edges i.e., 2→3, between 3 edges i.e., 2→4, or between 5 edges, i.e. 2→6 (the case of 9 edges is not shown). The time from 1-2 occurs through the guard time and is not to be used. For the discussion below, an edge is a high-to-low or low-to-high transition (edges are numbered – refer to [Figure 26.9 PWM and Tachometer Concepton page 221](#)).

The Tachometer circuit begins monitoring the tach when the associated PWM output transitions high and the guard time has expired. Each tach circuit will continue monitoring until either the ‘on’ time ends or the programmed number of edges has been detected, whichever comes first.

The Fan Tachometer value may be updated every 300ms, 500ms, or 1000ms.

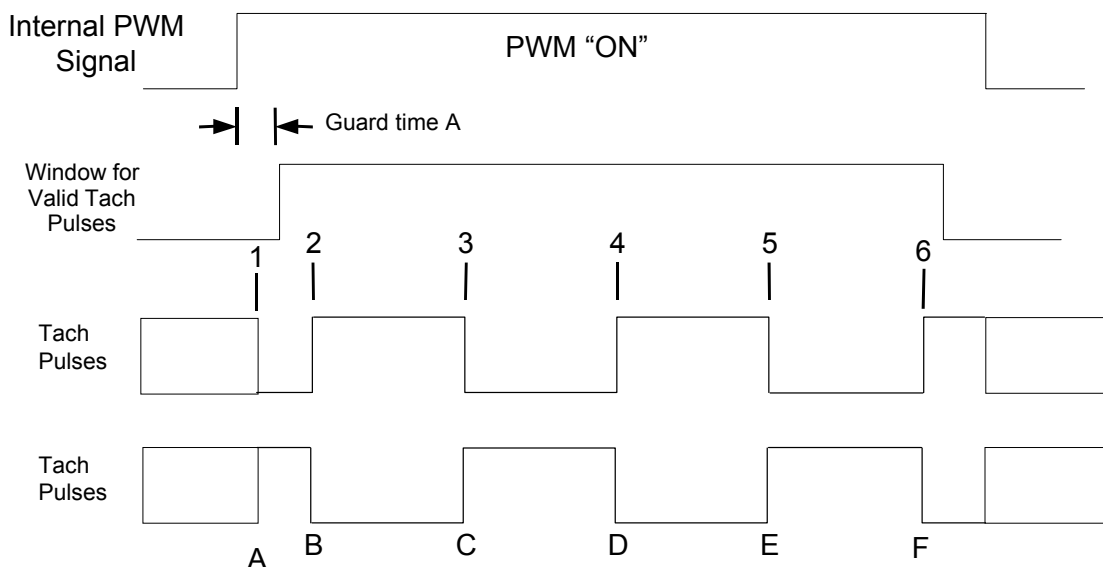


Figure 26.9 PWM and Tachometer Concept

FAN TACHOMETER OPTIONS FOR MODE 2

- 2, 3, 5 or 9 “edges” to calculate the fan speed ([Figure 26.9](#))
- Guard time A is programmable (8-63 clocks) to account for delays in the system ([Figure 26.9](#))
- Suggested PWM frequencies for modes 2 are: 11.0 Hz, 14.6 Hz, 21.9 Hz, 29.3 Hz, 35.2 Hz, 44.0 Hz, 58.6 Hz, 87.7Hz
- Option to ignore first 3 tachometer edges after guard time
- Option to force tach reading register to FFFh to indicate a slow fan.

26.1.9.5 Fan Tachometer Reading Registers:

The Tachometer Reading registers are 16 bits, unsigned. When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second. The value FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (this could be triggered by a counter overflow). These registers are read only – a write to these registers has no effect.

Notes:

- The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional.
- FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).
- The Tachometer registers are read only – a write to these registers has no effect.
- Mode 1 should be enabled and the tachometer limit register should be set to FFFFh if a tachometer input is left unconnected.

26.1.9.6 Programming Options for Each Tachometer Input

The features defined in this section are programmable via the TACHx Option registers located at offsets 90h-93h and the PWMx Option registers located at offsets 94h-96h.

TACH READING UPDATE TIME

In Mode 1, the Fan Tachometer Reading registers are continuously updated. In Mode 2, the fan tachometer registers are updated every 300ms, 500msec, or 1000msec. This option is programmed via bits[1:0] in the PWMx Option register. The PWM associated with a particular TACH(s) determines the TACH update time.

PROGRAMMED NUMBER OF TACH EDGES

In modes 1 & 2, the number of edges is programmable for 2, 3, 5 or 9 edges (i.e., ½ tachometer pulse, 1 tachometer pulse, 2 tachometer pulses, 4 tachometer pulses). This option is programmed via bits[2:1] in the TachX Option register.

Note: The “5 edges” case corresponds to two tachometer pulses, or 1 RPM for most fans. Using the other edge options will require software to scale the values in the reading register to correspond to the count for 1 RPM.

GUARD TIME (MODE 2 ONLY)

The guard time is programmable from 8 to 63 clocks (90kHz). This option is programmed via bits[4:3] in the TachX Option register.

IGNORE FIRST 3 TACHOMETER EDGES (MODE 2 ONLY)

Option to ignore first 3 tachometer edges after guard time. This option is programmed for each tachometer via bits[2:0] in the TACHx Option register. Default is do not ignore first 3 tachometer edges after guard time.

26.1.9.7 Summary of Operation for Modes 1 & 2

The following summarizes the detection cases:

- **No edge occurs during the PWM ‘ON’ time:** indicate this condition as a stalled fan
–The tachometer reading register contains FFFFh.
- **One edge (or less than programmed number of edges) occurs during the PWM ‘ON’ time:** indicate this condition as a slow fan.
–If the SLOW bit is enabled, the tachometer reading register will be set to FFFEh to indicate that this is a slow fan instead of a seized fan. Note: This operation also pertains to the case where the tachometer counter reaches FFFFh before the programmed number of edges occurs.
–If the SLOW bit is disabled, the tachometer reading register will be set to FFFFh. In this case, no distinction is made between a slow or seized fan.

Note: The Slow Interrupt Enable feature (SLOW) is configured in the TACHx Options registers at offsets 90h to 93h.

- **The programmed number of edges occurs:**
–Mode 1: If the programmed number of edges occurs before the counter reaches FFFFh latch the tachometer count
–Mode 2: If the programmed number of edges occurs during the PWM ‘ON’ time: latch the tachometer count (see **Note** below).

Notes:

- Whenever the programmed number of edges is detected, the edge detection ends and the state machine is reset. The tachometer reading register is updated with the tachometer count value at this time. See [Section 26.1.9.9, "Detection of a Stalled Fan," on page 224](#) for the one exception to this behavior.

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- In the case where the programmed number of edges occurs during the 'on' time, the tachometer value is latched when the last required edge is detected.

26.1.9.8 Examples of Minimum RPMs Supported

The following tables show minimum RPMs that can be supported with the different parameters. The first table uses 3 edges and the second table uses 2 edges.

Table 26.2 Minimum RPM Detectable Using 3 Edges

PWM FREQUENCY	PULSE WIDTH AT DUTY CYCLE (PWM "ON" TIME)			MINIMUM RPM AT DUTY CYCLE (Note 26.5) (30/T _{TachPulse})		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 26.4)	25%	50%	100%
87.7	2.85	5.7	11.36	10865	5347	2662
58.6	4.27	8.53	17	7175	3554	1774
44	5.68	11.36	22.64	5366	2662	1330
35.2	7.1	14.2	28.3	4279	2126	1063
29.3	8.53	17.06	34	3554	1768	885
21.9	11.42	22.83	45.48	2648	1319	661
14.6	17.12	34.25	68.23	1761	878	440
11	22.73	45.45	90.55	1325	661	332

Note 26.4 100% duty cycle is 255/256

Note 26.5 $RPM = 60 / T_{\text{Revolution}}$, $T_{\text{TachPulse}} = T_{\text{Revolution}} / 2$. Using 3 edges for detection, $T_{\text{TachPulse}} = (\text{PWM "ON" Time} - \text{Guard Time})$. Minimum RPM values shown use minimum guard time (88.88uSec).

Table 26.3 Minimum RPM Detectable Using 2 Edges

PWM FREQUENCY	PULSE WIDTH AT DUTY CYCLE (PWM "ON" TIME)			MINIMUM RPM AT DUTY CYCLE (Note 26.7) (30/T _{TachPulse})		
(HZ)	25% (MSEC)	50% (MSEC)	100% (MSEC) (Note 26.6)	25%	50%	100%
87.7	2.85	5.7	11.36	5433	2673	1331
58.6	4.27	8.53	17	3588	1777	887
44	5.68	11.36	22.64	2683	1331	665
35.2	7.1	14.2	28.3	2139	1063	532
29.3	8.53	17.06	34	1777	884	442
21.9	11.42	22.83	45.48	1324	660	330
14.6	17.12	34.25	68.23	881	439	220
11	22.73	45.45	90.55	663	331	166

Note 26.6 100% duty cycle is 255/256

Note 26.7 $RPM = 60 / T_{\text{Revolution}}$, $T_{\text{TachPulse}} = T_{\text{Revolution}} / 2$. Using 2 edges for detection, $T_{\text{TachPulse}} = 2 * (\text{PWM "ON" Time-Guard Time})$. Minimum RPM values shown use minimum guard time (88.88usec).

26.1.9.9 Detection of a Stalled Fan

There is a fan failure bit (TACHx) in the interrupt status register used to indicate that a slow or stalled fan event has occurred. If the tach reading value exceeds the value programmed in the tach limit register the interrupt status bit is set. See Interrupt Status register 2 at offset 42h.

Notes:

- The reading register will be forced to FFFFh if a stalled event occurs (i.e., stalled event = no edges detected.)
- The reading register will be forced to either FFFFh or FFFEh if a slow fan event occurs. (i.e., slow event: $0 < \#edges < \text{programmed } \#edges$). If the control bit, SLOW, located in the TACHx Options registers at offsets 90h - 93h, is set then FFFEh will be forced into the corresponding Tach Reading Register to indicate that the fan is spinning slowly.
- The fan tachometer reading register stays at FFFFh in the event of a stalled fan. If the fan begins to spin again, the tachometer logic will reset and latch the next valid reading into the tachometer reading register.

26.1.9.10 Fan Interrupt Status Bits

The status bits for the fan events are in Interrupt Status Register 2 (42h). These bits are set when the reading register is above the tachometer minimum and the Interrupt Enable 2 (Fan Tachs) register bits are configured to enable Fan Tach events. No interrupt status bits are set for fan events (even if the fan is stalled) if the associated tachometer minimum is set to FFFFh (registers 54h-5Bh).

Note: The Interrupt Enable 2 (Fan Tachs) register at offset 80h defaults to enabled for the individual tachometer status events bits. The group Fan Tach nHWM_INT bit defaults to disabled. This bit needs to be set if Fan Tach interrupts are to be generated on the external nHWM_INT pin.

See [Figure 25.1 Interrupt Control](#) on page 197.

26.1.10 Linking Fan Tachometers to PWMs

The TACH/PWM Association Register at offset 81h is used to associate a Tachometer input with a PWM output. This association has three purposes:

1. The auto fan control logic supports a feature called SpinUp Reduction. If SpinUp Reduction is enabled (SUREN bit), the auto fan control logic will stop driving the PWM output high if the associated TACH input is operating within normal parameters. (Note: SUREN bit is located in the Configuration Register at offset 7Fh)
2. To measure the tachometer input in Mode 2, the tachometer logic must know when the associated PWM is 'ON'.
3. Inhibit fan tachometer interrupts when the associated PWM is 'OFF'.

See the description of the PWM_TACH register. The default configuration is:

PWM1 -> FANTACH1.

PWM2 -> FANTACH2.

PWM3 -> FANTACH3 & FANTACH4.

Note: If a FANTACH is associated with a PWM operating in high frequency mode (see [Registers 5Fh – 61h: Zone x Range/FANx Frequency](#) on page 205) the tach monitoring logic must be

configured for Mode 1 (see Bit[3] Mode in [Registers 90h-93h: FANTACHX Option Registers on page 262](#)).

26.2 Fan Control for PWMs[A,B] and FANTACHs[A,B]

The following sections describe the operation of PWMA, PWMB, FANTACHA, and FANTACHB.

26.2.1 Limit and Configuration Registers

At power up, all the registers are reset to their default values and PWMA and PWMB are set to Full Fan (duty cycle =FFh). The following is a list of the registers implemented to support PWMA, PWMB, FANTACHA, and FANTACHB

- [Section 27.2.58, "Registers A5h - A6h: PWM\[A,B\] Current Duty Cycle," on page 265](#)
- [Section 27.2.59, "Registers A7h - A8h: PWMx Frequency," on page 266](#)
- [Section 27.2.60, "Registers A9h - ACh: Fan Tachometer Reading," on page 266](#)
- [Section 27.2.61, "Registers ADh - B0h: Fan Tachometer Low Limit \(MSB, LSB\)," on page 267](#)
- [Section 27.2.64, "Registers B6h - B7h: TPC Tachx Option Register," on page 268](#)
- [Section 27.2.65, "Registers B8h - B9h: Max RPM for TACHs A,B," on page 269](#)

26.2.2 PWM Fan Speed Control

Note: PWMA and PWMB are alternate functions on GP57 and GP55 respectively.

PWMA and PWMB are software controllable PWMs. These PWM outputs generate a duty cycle based on the programmed value in the PWMx Current Duty Cycle registers at the programmed frequency. The PWM duty cycle is an 8-bit value, where the programmed value represents the percentage of ON time. In other words, the programmed value divided by 256 represent the fraction of the PWM period that the pin is active. The duty cycle period is determined by the programmed frequency, which is selected in the PWMx Frequency registers. These PWMs support both low and high frequency fans. See [Section 27.2.59, "Registers A7h - A8h: PWMx Frequency," on page 266](#).

PWMA and PWMB are associated to FANTACHA and FANTACHB respectively. If the associated FANTACHs have sampling enabled, a small pulse (1-2 90kHz clocks wide) will be driven onto the PWM output. This additional pulse does not effect the speed of the fan nor does it induce any additional system noise.

26.2.3 Fan Speed Monitoring

Notes:

- FANTACHA and FANTACHB are alternate functions on GP56 and GP54 respectively.
- FANTACHA will be associated with PWMA and FANTACHB will be associated with PWMB. Both of these tachometer inputs may also be configured to monitor tachometer inputs of fans controlled externally to the chip.

Each FANTACH input has a Reading Register, Limit Register, Interrupt Status bit, and Interrupt Enable bit in addition to special configuration bits. The following sections describe how fan speed monitoring has been enabled for FANTACHs A and B.

FANTACHA and FANTACHB have been implemented as Tach Pulse Counters (TPC), which allows them to return a reading value that represents the number of pulses counted over a specified period of time.

The TPC Tach monitor has been designed to support the 3-wire fan implementation, where the PWM control circuit is operated at low frequencies and is used to break the ground connection on the fan. Yet, this tach monitoring operation is capable of monitoring three or four wire fans that are being

controlled by the associated PWM at both low and high frequencies and it can be used to monitor a fan that is being driven by an external device if the tach signal is always valid.

The Tach Pulse Counter (TPC) samples the level of the tach input signal. The sampling rate may be set to the maximum sampling rate or it may dynamically adjust the sampling rate to the speed of the fan. If dynamic sampling is enabled, then when the PWM is operating at high duty cycles, the sampling pulses will be generated at or near the maximum sampling rate for that fan, but they are dominated by the PWM ON time. Sampling pulses are only apparent when the PWM pin is driving low. When the PWM is operating at low duty cycles and dynamic sampling is enabled, the sampling pulses will be generated at a much lower frequency. These small pulses generated at low frequencies essentially have no effect on the speed of the fan and they are not audible.

Using this sampling method it can be determined how many tach pulses were received over a specified interval of time. The TPC Tach logic will accumulate the number of tach pulses over a programmed interval, which is determined by the Tach Update Rate bits located in [Registers B6h - B7h: TPC Tachx Option Register](#). This accumulated value will be returned as 16-bit value that gets loaded into the TACH Reading Registers (MSB,LSB) if Bit[5]: TACH Value of [Registers B6h - B7h: TPC Tachx Option Register](#) is set to zero. If this bit is set to one, the TPC value will be converted to return the reading in legacy mode, where the 16-bit reading value represents the number of 90kHz pulses per revolution.

Note: The TPC TACH Monitor supports fans that generate two, three, or four tach pulses per revolution at ~50% duty cycle. The legacy mode option (reading in clocks per rotation) is limited to fans that emit 2 pulses per revolution with a ~50% duty cycle.

APPLICATION NOTE: Tach interrupts should be disabled prior to changing the tach reading from TPC mode to number of 90kHz pulses or from 90kHz pulses to TPC mode.

The TPC Tach monitoring circuit can be configured to sample the tach input at a fixed frequency or it can be configured to dynamically adjust the sampling rate based on the expected tach frequency. [Table 27.18, "Program Value for TACH Max RPM and Max Sampling Rates," on page 269](#) shows how to configure the device for the expected maximum frequency. If dynamic sampling rates are enabled, the fan being monitored must be controlled by the associated PWM output. Bit[4] of [Registers B6h - B7h: TPC Tachx Option Register](#) is used to enable or disable dynamic sampling. If the tachometer pulse is always valid the sampling feature may be disabled via Bit[3] of [Registers B6h - B7h: TPC Tachx Option Register](#).

If sampling is enabled, then the associated PWM will be turned on for 1-2 90kHz clocks as determined by the sampling rate. The duration of the sampling pulse is determined by Bit[2] of [Registers B6h - B7h: TPC Tachx Option Register](#).

The TPC Tach monitor can be programmed to update the TACH Reading registers at a rate of 0.5 seconds, 1.0 second, or 2 seconds. This update rate is selectable by Bits[1:0] of the [Registers B6h - B7h: TPC Tachx Option Register](#).

If the TPC Tach monitor is configured to return the reading in TPC mode, software must multiply the resulting value by a fixed value as shown in the equation below to convert the reading to RPMs.

$$RPMs = TachReading \times Multiplier$$

The following table shows how to choose the Multiplier to convert the TPC reading to Rotations per Minute (RPM).

Table 26.4 TPC TACH Reading Converted to RPMs

TACH UPDATE RATE (SEC)	MULTIPLIER TO CONVERT TPC READING TO RPM VALUE
0.5	60
1.0	30
2.0	15

26.2.3.1 Detection of a Slow or Stalled Fan

Each FANTACH input has an associated limit register and interrupt status bit. If the FANTACH Reading violates the programmed minimum limit the corresponding interrupt status bit is set, indicating that a slow or stalled tach event has occurred. Software can determine the operation of the fan by reading the FANTACH Reading register.

The low limit registers for FANTACHA and FANTACHB are located in the HWM Registers at locations ADh to B0h. See [Section 27.2.61, "Registers ADh - B0h: Fan Tachometer Low Limit \(MSB, LSB\)," on page 267](#) for a description of these registers.

The FANTACHA and FANTACHB interrupt status bits are located in [Register 83h: Interrupt Status Register 3](#). These status bits can be enabled by their individual enable bits located in [Register 80h: Interrupt Enable 2 Register](#).

Note: For a FANTACH interrupt event to be generated on the pin once the status bit is set both the FANTACH group enable bit and the global interrupt enable bit must be set. The FANTACH group enable bit is located in [Register 80h: Interrupt Enable 2 Register](#). The global Interrupt Enable is located in Bit[2] of [Register 7Ch: Special Function Register on page 254](#).

If the reading value is reported in the number of 90kHz clocks and the FANTACH reading register exceeds the value in the corresponding FANTACH Minimum Limit register an interrupt bit will be set. If the reading value is reported as the tach pulse counter (TPC) and the FANTACH reading register is less than the value in the corresponding FANTACH Minimum Limit register an interrupt bit will be set.

Note: Tach interrupts are not blocked when the corresponding PWM duty cycle is 00h.

APPLICATION NOTE: Before turning a fan off the corresponding tach interrupt should be disabled to prevent unwanted interrupts.

Interrupts will never be generated for a fan:

- In legacy mode, if its tachometer minimum is set to FFFFh.
- In TPC mode, if its tachometer minimum is set to 0000h.

Notes:

- In legacy mode, the fan tachometer reading register stays at FFFEh in the event of a stalled fan. In legacy mode, FFFEh indicates that the fan is slow or not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow). This is the maximum tachometer count value in legacy mode. In TPC mode, the fan tachometer reading register stays at 0000h in the event of a stalled fan. If the fan begins to spin again, the tachometer logic will reset and latch the next valid reading into the tachometer reading register.
- See [Figure 25.1 Interrupt Control on page 197](#) for a detailed diagram of how the interrupts are controlled.
- Hardware Monitoring interrupts, like the FANTACH interrupts, may generate an interrupt event on the nHWM_INT pin or a PME event. See the PME registers. [PMES3_STS1](#) and [PMES5_STS1](#), in the [Chapter 28, "Runtime Registers," on page 271](#).



Chapter 27 Hardware Monitoring Register Set

The following sections list and define the registers implemented in the Hardware Monitoring block. These registers are accessible via the SMBus interface.

27.1 Register Summary

Definition for the Lock column:

Yes = Register is made read-only when the Lock bit is set; No = Register is **not** made read-only when the Lock bit is set.

Notes:

- All the HWM registers/bits are reset to their default value on a VTR POR unless otherwise specified. Registers/bits reset on a VCC POR are shaded in light gray in the table below.
- Reserved bits are shaded dark gray. These bits are defined as: reads return 0, writes are ignored.

Table 27.1 HWM Register Summary

Reg Addr	Read/Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock
00h-0Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
10h	R/W	SMSC Test Register		7	6	5	4	3	2	1	0	00h	No
10h-1Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
1Dh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
1Eh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
1Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
20h	R	+5VTR Reading		7	6	5	4	3	2	1	0	N/A	No
21h	R	Vccp Reading		7	6	5	4	3	2	1	0	N/A	No
22h	R	VCC Reading		7	6	5	4	3	2	1	0	N/A	No
23h	R	+5V Reading		7	6	5	4	3	2	1	0	N/A	No
24h	R	+12V Reading		7	6	5	4	3	2	1	0	N/A	No
25h	R	Remote Diode 1 Temp Reading		7	6	5	4	3	2	1	0	N/A	No
26h	R	Internal Temp Reading		7	6	5	4	3	2	1	0	N/A	No
27h	R	Remote Diode 2 Temp Reading		7	6	5	4	3	2	1	0	N/A	No
28h	R	FANTACH1 Reading LSB		7	6	5	4	3	2	1	0	FFh Note 27.8	No
29h	R	FANTACH1 Reading MSB		15	14	13	12	11	10	9	8	FFh Note 27.8	No
2Ah	R	FANTACH2 Reading LSB		7	6	5	4	3	2	1	0	FFh Note 27.8	No
2Bh	R	FANTACH2 Reading MSB		15	14	13	12	11	10	9	8	FFh Note 27.8	No
2Ch	R	FANTACH3 Reading LSB		7	6	5	4	3	2	1	0	FFh Note 27.8	No
2Dh	R	FANTACH3 Reading MSB		15	14	13	12	11	10	9	8	FFh Note 27.8	No
2Eh	R	FANTACH4 Reading LSB		7	6	5	4	3	2	1	0	FFh Note 27.8	No
2Fh	R	FANTACH4 Reading MSB		15	14	13	12	11	10	9	8	FFh Note 27.8	No
30h	R/W Note 27.1	PWM1 Current Duty Cycle		7	6	5	4	3	2	1	0	N/A	Yes Note 27.1
31h	R/W Note 27.1	PWM2 Current Duty Cycle		7	6	5	4	3	2	1	0	N/A	Yes Note 27.1
32h	R/W Note 27.1	PWM3 Current Duty Cycle		7	6	5	4	3	2	1	0	N/A	Yes Note 27.1
33h-3Dh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
3Eh	R	Company ID		7	6	5	4	3	2	1	0	5Ch	No
3Fh	R	Version / Stepping		VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	89h Note 27.11	No
40h	R/W Note 27.2	Ready/Lock/Start		RES	RES	START Default Note 27.9	Vbat Mon	OVRID	READY Note 27.10	LOCK Note 27.8	START Note 27.9	00h	Yes Note 27.2
41h	R-C Note 27.3	Interrupt Status Register 1		INT23	D2	AMB	D1	5V	VCC	Vccp	5VTR	00h Note 27.8	No
42h	R-C Note 27.3	Interrupt Status Register 2		ERR2	ERR1	FANTA CH4	FANTA CH3	FANTA CH2	FANTA CH1	RES	12V	00h Note 27.8	No
43h	R	VID Register		RES	RES	VID5	VID4	VID3	VID2	VID1	VID0	N/A	No
44h	R/W	5VTR Low Limit		7	6	5	4	3	2	1	0	00h	No
45h	R/W	5VTR High Limit		7	6	5	4	3	2	1	0	FFh	No
46h	R/W	Vccp Low Limit		7	6	5	4	3	2	1	0	00h	No
47h	R/W	Vccp High Limit		7	6	5	4	3	2	1	0	FFh	No
48h	R/W	VCC Low Limit		7	6	5	4	3	2	1	0	00h	No
49h	R/W	VCC High Limit		7	6	5	4	3	2	1	0	FFh	No
4Ah	R/W	5V Low Limit		7	6	5	4	3	2	1	0	00h	No
4Bh	R/W	5V High Limit		7	6	5	4	3	2	1	0	FFh	No
4Ch	R/W	12V Low Limit		7	6	5	4	3	2	1	0	00h	No
4Dh	R/W	12V High Limit		7	6	5	4	3	2	1	0	FFh	No
4Eh	R/W	Remote Diode 1 Low Temp		7	6	5	4	3	2	1	0	81h	No
4Fh	R/W	Remote Diode 1 High Temp		7	6	5	4	3	2	1	0	7Fh	No
50h	R/W	Internal Low Temp		7	6	5	4	3	2	1	0	81h	No
51h	R/W	Internal High Temp		7	6	5	4	3	2	1	0	7Fh	No

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Table 27.1 HWM Register Summary (continued)

Reg Addr	Read/Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock
52h	R/W	Remote Diode 2 Low Temp		7	6	5	4	3	2	1	0	81h	No
53h	R/W	Remote Diode 2 High Temp		7	6	5	4	3	2	1	0	7Fh	No
54h	R/W	FANTACH1 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No
55h	R/W	FANTACH1 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No
56h	R/W	FANTACH2 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No
57h	R/W	FANTACH2 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No
58h	R/W	FANTACH3 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No
59h	R/W	FANTACH3 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No
5Ah	R/W	FANTACH4 Minimum LSB		7	6	5	4	3	2	1	0	FFh	No
5Bh	R/W	FANTACH4 Minimum MSB		15	14	13	12	11	10	9	8	FFh	No
5Ch	R/W	PWM 1 Configuration		ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes
5Dh	R/W	PWM 2 Configuration		ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes
5Eh	R/W	PWM 3 Configuration		ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes
5Fh	R/W	Zone 1 Range/PWM 1 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh	Yes
60h	R/W	Zone 2 Range/PWM 2 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh	Yes
61h	R/W	Zone 3 Range/PWM 3 Frequency		RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh	Yes
62h	R/W	PWM1 Ramp Rate Control		RES1	RES1	RES1	RES	RR1E	RR1-2	RR1-1	RR1-0	E0h	Yes
63h	R/W	PWM 2, PWM3 Ramp Rate Control		RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h	Yes
64h	R/W	PWM 1 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes
65h	R/W	PWM 2 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes
66h	R/W	PWM 3 MINIMUM Duty Cycle		7	6	5	4	3	2	1	0	80h	Yes
67h	R/W	Zone 1 Low Temp Limit (Note 27.12)		7	6	5	4	3	2	1	0	80h	Yes
68h	R/W	Zone 2 Low Temp Limit (Note 27.12)		7	6	5	4	3	2	1	0	80h	Yes
69h	R/W	Zone 3 Low Temp Limit (Note 27.12)		7	6	5	4	3	2	1	0	80h	Yes
6Ah	R/W	Zone 1 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes
6Bh	R/W	Zone 2 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes
6Ch	R/W	Zone 3 Temp Absolute Limit		7	6	5	4	3	2	1	0	64h	Yes
6Dh	R/W	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	44h	Yes
6Eh	R/W	SMSC Test Register		TST3	TST2	TST1	TST0	RES	RES	RES	RES	40h	Yes
6Fh	R/W	XOR Test Tree Enable		RES	RES	RES	RES	RES	RES	RES	XEN	00h	Yes
70h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No
71h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No
72h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No
73h	R	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	No
74h	R/W	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	Yes
75h	R	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	No
76h	R/W	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	Yes
77h	R	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	No
78h	R/W	SMSC Test Register		RES	RES	RES	RES	TST3	TST2	TST1	TST0	09h	Yes
79h	R/W	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	Yes
7Ah	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	No
7Bh	R/W	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	Yes
7Ch	R/W Note 27.4	Special Function Register		AVG2	AVG1	AVG0	SMSC Note 27.5	ZN1_SEL	INTEN	MON-MD	LPMD Note 27.5	40h	Yes Note 27.4
7Dh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
7Eh	R/W	Interrupt Enable 1 (Voltages)		VCC	12V	5V	VTR	VCCP	5VTR	VBAT	VOLT	ECh	Yes
7Fh	R/W	Configuration		INIT	SMSC Note 27.7	SMSC Note 27.7	SUREN	TRDY Note 27.8	VID5 /FANTACH3	ZN2 Sel	SMSC	10h	Yes
80h	R/W	Interrupt Enable 2 (Fan Tachs)		RES	FAN-TACHB	FAN-TACHA	FANTACH4	FANTACH3	FANTACH2	FANTACH1	FAN-TACH	7Eh	Yes
81h	R/W	TACH_PWM Association		T4H	T4L	T3H	T3L	T2H	T2L	T1H	T1L	A4h	Yes
82h	R/W	Interrupt Enable 3 (Temp)		RES	RES	RES	RES	D2EN	D1EN	AMB	TEMP	0Eh	Yes

Table 27.1 HWM Register Summary (continued)

Reg Addr	Read/Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock
83h	R	Interrupt Status Register 3		FAN-TACHB	FAN-TACHA	RES	RES	RES	RES	Vbat	VTR	00h Note 27.8	No
84h	R	A/D Converter LSbs Reg 5		VTR.3	VTR.2	VTR.1	VTR.0	VB.T.3	VB.T.2	VB.T.1	VB.T.0	00h	No
85h	R	A/D Converter LSbs Reg 1		RD2.3	RD2.2	RD2.1	RD2.0	RD1.3	RD1.2	RD1.1	RD1.0	N/A	No
86h	R	A/D Converter LSbs Reg 2		V12.3	V12.2	V12.1	V12.0	AM.3	AM.2	AM.1	AM.0	N/A	No
87h	R	A/D Converter LSbs Reg 3		V50.3	V50.2	V50.1	V50.0	V25.3	V25.2	V25.1	V25.0	N/A	No
88h	R	A/D Converter LSbs Reg 4		VCC.3	VCC.2	VCC.1	VCC.0	VCP.3	VCP.2	VCP.1	VCP.0	N/A	No
89h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No
8Ah	R	SMSC Test Register		RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh	No
8Bh	R/W	SMSC Test Register		RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh	Yes
8Ch	R	SMSC Test Register		RES	RES	RES	TST4	TST3	TST2	TST1	TST0	N/A	No
8Dh	R/W	SMSC Test Register		RES	RES	RES	TST4	TST3	TST2	TST1	TST0	N/A	Yes
8Eh	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No
8Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
90h	R/W	FANTACH1 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No
91h	R/W	FANTACH2 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No
92h	R/W	FANTACH3 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No
93h	R/W	FANTACH4 Option		RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h	No
94h	R/W	PWM1 Option		RES Note 27.6	RES Note 27.6	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch	No
95h	R/W	PWM2 Option		RES Note 27.6	RES Note 27.6	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch	No
96h	R/W	PWM3 Option		RES Note 27.6	RES Note 27.6	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch	No
97h	R/W	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	5Ah	Yes
98h	R/W	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	F1h	Yes
99h	R	VTR Reading		7	6	5	4	3	2	1	0	N/A	No
9Ah	R	Vbat Reading		7	6	5	4	3	2	1	0	N/A	No
9Bh	R/W	VTR Low Limit		7	6	5	4	3	2	1	0	00h	No
9Ch	R/W	VTR High Limit		7	6	5	4	3	2	1	0	FFh	No
9Dh	R/W	VBAT Low Limit		7	6	5	4	3	2	1	0	00h	No
9Eh	R/W	VBAT High Limit		7	6	5	4	3	2	1	0	FFh	No
9Fh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
A0h	R/W	SLP_S3# INT Mask Register		VCC	12V	5V	VTR	VCCP	5VTR	VBAT	RES	00h	Yes
A1h	R/W	SMSC Reserved		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	Yes
A2h	R/W	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	N/A	Yes
A3h	R/W	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h	Yes
A4h	R	SMSC Test Register		TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A	No
A5h	R/W	PWMA Current Duty Cycle		7	6	5	4	3	2	1	0	FFh	Yes
A6h	R/W	PWMB Current Duty Cycle		7	6	5	4	3	2	1	0	FFh	Yes
A7h	R/W	PWM A Frequency		RES	RES	RES	RES	FRQ3	FRQ2	FRQ1	FRQ0	0Bh	Yes
A8h	R/W	PWM B Frequency		RES	RES	RES	RES	FRQ3	FRQ2	FRQ1	FRQ0	0Bh	Yes
A9h	R	FANTACHA Reading LSB		7	6	5	4	3	2	1	0	FEh Note 27.8	No
AAh	R	FANTACHA Reading MSB		15	14	13	12	11	10	9	8	FFh Note 27.8	No
ABh	R	FANTACHB Reading LSB		7	6	5	4	3	2	1	0	FEh Note 27.8	No
ACH	R	FANTACHB Reading MSB		15	14	13	12	11	10	9	8	FFh Note 27.8	No
ADh	R/W	FANTACHA Minimum LSB		7	6	5	4	3	2	1	0	FFh	No
A Eh	R/W	FANTACHA Minimum MSB		15	14	13	12	11	10	9	8	FFh	No
AFh	R/W	FANTACHB Minimum LSB		7	6	5	4	3	2	1	0	FFh	No
B0h	R/W	FANTACHB Minimum MSB		15	14	13	12	11	10	9	8	FFh	No
B1h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
B2h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No

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Reg Addr	Read/ Write	Reg Name		Bit 7 MSb	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSb	Default Value	Lock
B3h	R/W	SMSC Test Register		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
B4h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
B5h	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
B6h	R/W	TPC TachA Option Register		RES	RES	tpc/clk Periods	Depreci- ation Disable	Sam- pling Disable	Pulse Duration	1	0	28h	No
B7h	R/W	TPC TachB Option Register		RES	RES	tpc/clk Periods	Depreci- ation Disable	Sam- pling Disable	Pulse Duration	1	0	28h	No
B8h	R/W	Max RPM for TACHA		7	6	5	4	3	2	1	0	0Eh	No
B9h	R/W	Max RPM for TACHB		7	6	5	4	3	2	1	0	0Eh	No
BAh	R	SMSC Test Register		7	6	5	4	3	2	1	0	0Fh	No
BBh	R	SMSC Test Register		7	6	5	4	3	2	1	0	0Fh	No
BCh-FEh	R	Reserved		RES	RES	RES	RES	RES	RES	RES	RES	00h	No
FFh	R	SMSC Test Register		TST7	TST 6	TST 5	TST 4	TST3	TST2	TST1	TST0	N/A	No

Note: SMSC Test Registers may be read/write registers. Writing these registers can cause unwanted results.

Note 27.1 The PWMx Current Duty Cycle Registers are only writable when the associated fan is in manual mode. In this case, the register is writable when the start bit is set, but not when the lock bit is set.

Note 27.2 The Lock and Start bits in the Ready/Lock/Start register are locked by the Lock Bit. The OVRID bit and the Vbat bit are always writable, both when the start bit is set and when the lock bit is set.

Note 27.3 The Interrupt status registers are cleared on a read if no events are active

Note 27.4 The INTEN bit in register 7Ch is always writable when the lock bit is set.

Note 27.5 In Shutdown Mode (LPMD=1 & START=0) all the H/W Monitoring registers/bits are not accessible except for the following: Bits[2:0] in the Special Function Register (SFTR) at offset 7Ch and Bits[7:0] in the Configuration register at offset 7Fh.

Note 27.6 These Reserved bits are read/write bits. Writing these bits to a '1' has no effect on the hardware.

Note 27.7 SMSC bits may be read/write bits. Writing these bits to a value other than the default value may cause unwanted results

Note 27.8 This register/bit is reset to its default value on a VCC POR.

Note 27.9 The START bit may be reset to its default value on a VCC POR or a VTR POR depending on the setting of Bit[5] START_Default located in the same register.

Note 27.10 The READY bit indicates that the device is operational. The device is operational immediately after power has been applied to the device, therefore software will always see this bit as a '1'.

Note 27.11 Version / Stepping number can range from 89h to 8Fh. The initial Version / Stepping number is 89h. Contact SMSC for latest Version / Stepping number.

Note 27.12 All three Zone x Low Temp Limit (67h, 68h and 69h) must be written to a value that is not 80h in order for autofan to operate.

27.2 Detailed Register Description

Note: Reserved registers are read-only registers that return a value of 00h, unless otherwise specified. Writes to reserved registers are ignored.

27.2.1 Register 00h-0Fh: Reserved

27.2.2 Register 10h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
10h	R/W	SMSC TEST	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

Setting the Lock bit has no effect on this register.

This register must not be written. Writing this register may produce unexpected results.

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27.2.3 Registers 11h-1Fh: Reserved**27.2.4 Registers 20-24h, 99-9Ah: Voltage Reading**

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
20h	R	5VTR Reading	7	6	5	4	3	2	1	0	N/A
21h	R	Vccp Reading	7	6	5	4	3	2	1	0	N/A
22h	R	VCC Reading	7	6	5	4	3	2	1	0	N/A
23h	R	+5V Reading	7	6	5	4	3	2	1	0	N/A
24h	R	+12V Reading	7	6	5	4	3	2	1	0	N/A
99h	R	VTR Reading	7	6	5	4	3	2	1	0	N/A
9Ah	R	Vbat Reading	7	6	5	4	3	2	1	0	N/A

The Voltage Reading registers reflect the current voltage of the voltage monitoring inputs. Voltages are presented in the registers at $\frac{3}{4}$ full scale for the nominal voltage, meaning that at nominal voltage, each register will read C0h, except for the Vbat input. Vbat is nominally a 3.0V input that is implemented on a +3.3V (nominal) analog input. Therefore, the nominal reading for Vbat is AEh.

Note: Vbat will only be monitored when the Vbat Monitoring Enable bit is set to '1'. Updating the Vbat register automatically clears the Vbat Monitoring Enable bit.

Table 27.2 Voltage vs. Register Reading

INPUT	NOMINAL VOLTAGE	REGISTER READING AT NOMINAL VOLTAGE	MAXIMUM VOLTAGE	REGISTER READING AT MAXIMUM VOLTAGE	MINIMUM VOLTAGE	REGISTER READING AT MINIMUM VOLTAGE
VTR	3.3V	C0h	4.38V	FFh	0V	00h
Vbat (Note 27.13)	3.0V	AEh	4.38V	FFh	0V	00h
5VTR	5.0V	C0h	6.64V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

Note 27.13 Vbat is a nominal 3.0V input source that has been implemented on a 3.3V analog voltage monitoring input.

The Voltage Reading registers will be updated automatically by the device with a minimum frequency of 4Hz if the average bits located in the Special Function register at offset 7Ch are set to 001. See [Table 25.2, "Conversion Cycle Timing," on page 193](#) for a complete list of the conversion times for the different programmable averaging options.

These registers are read only – a write to these registers has no effect.

27.2.5 Registers 25-27h: Temperature Reading

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
25h	R	Remote Diode 1 Temp Reading	7	6	5	4	3	2	1	0	N/A
26h	R	Internal Temp Reading	7	6	5	4	3	2	1	0	N/A
27h	R	Remote Diode 2 Temp Reading	7	6	5	4	3	2	1	0	N/A

The Temperature Reading registers reflect the current temperatures of the internal and remote diodes. Remote Diode 1 Temp Reading register reports the temperature measured by the Remote1- and Remote1+ pins, Remote Diode 2 Temp Reading register reports the temperature measured by the Remote2- and Remote2+ pins, and the Internal Temp Reading register reports the temperature measured by the internal (ambient) temperature sensor. Current temperatures are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in [Table 27.3](#). The Temperature Reading register will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly (this corresponds to the diode fault interrupt status bits). The Temperature Reading registers will be updated automatically by the SCH5017 Chip with a minimum frequency of 4Hz.

Note: These registers are read only – a write to these registers has no effect.

Each of the temperature reading registers are mapped to a zone. Each PWM may be programmed to operate in the auto fan control operating mode by associating a PWM with one or more zones. The following is a list of the zone associations.

- Zone 1 is controlled by Remote Diode 1 Temp Reading
- Zone 2 is controlled by Internal Temp Reading (Ambient Temperature Sensor) or Remote Diode 2 (see Bit[1] Zone 2 Select in the [Register 7Fh: Configuration Register on page 256](#))
- Zone 3 is controlled by Remote Diode 2 Temp Reading

Table 27.3 Temperature vs. Register Reading

Temperature	Reading (Dec)	Reading (Hex)
-127°C	-127	81h
.	.	.
.	.	.
-50°C	-50	CEh
.	.	.
.	.	.
0°C	0	00h
.	.	.
.	.	.
50°C	50	32h
.	.	.
.	.	.
127°C	127	7Fh
(SENSOR ERROR)		80h

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27.2.6 Registers 28-2Fh: Fan Tachometer Reading

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
28h	R	FANTACH1 Reading LSB	7	6	5	4	3	2	1	0	FFh
29h	R	FANTACH1 Reading MSB	15	14	13	12	11	10	9	8	FFh
2Ah	R	FANTACH2 Reading LSB	7	6	5	4	3	2	1	0	FFh
2Bh	R	FANTACH2 Reading MSB	15	14	13	12	11	10	9	8	FFh
2Ch	R	FANTACH3 Reading LSB	7	6	5	4	3	2	1	0	FFh
2Dh	R	FANTACH3 Reading MSB	15	14	13	12	11	10	9	8	FFh
2Eh	R	FANTACH4 Reading LSB	7	6	5	4	3	2	1	0	FFh
2Fh	R	FANTACH4 Reading MSB	15	14	13	12	11	10	9	8	FFh

Note: These registers are reset to their default value on a VCC POR.

The Fan Tachometer Reading registers contain the number of 11.111 μ s periods (90KHz) between the programmed number of edges. Five edges returns the number of clocks between full fan revolutions if the fans produce two tachometer pulses per full revolution. These registers are updated at least once every second.

This value is represented for each fan in a 16 bit, unsigned number.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, including when the start bit=0.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

These registers are read only – a write to these registers has no effect.

27.2.7 Registers 30-32h: Current PWM Duty

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
30h	R/W (See Note)	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
31h	R/W (See Note)	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A
32h	R/W (See Note)	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	N/A

Note: These registers are only writable when the associated fan is in manual mode. These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Current PWM Duty registers store the duty cycle that the chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh. After the **Ready/Lock/Start** Register Start bit is set, this register and the PWM signals are updated based on the algorithm described in the Auto Fan Control Operating Mode section and the Ramp Rate Control logic, unless the associated fan is in manual mode – see below.

Note: When the device is configured for Manual Mode, the Ramp Rate Control logic should be disabled.

When read, the Current PWM Duty registers return the current PWM duty cycle for the respective PWM signal.

These registers are read only – a write to these registers has no effect.

Note: If the current PWM duty cycle registers are written while the part is not in manual mode or when the start bit is zero, the data will be stored in internal registers that will only be active and observable when the start bit is set and the fan is configured for manual mode. While the part is not in manual mode and the start bit is zero, the current PWM duty cycle registers will read back FFh.

Manual Mode (Test Mode)

In manual mode, when the start bit is set to 1 and the lock bit is 0, the current duty cycle registers are writeable to control the PWMs.

Note: When the lock bit is set to 1, the current duty cycle registers are Read-Only.

The PWM duty cycle is represented as follows:

Table 27.4 PWM Duty vs Register Reading

CURRENT DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

During spin-up, the PWM duty cycle is reported as 0%.

Notes:

- The PWMx Current Duty Cycle always reflects the current duty cycle on the associated PWM pin.
- The PWMx Current Duty Cycle register is implemented as two separate registers: a read-only and a write-only. When a value is written to this register in manual mode there will be a delay before the programmed value can be read back by software. The hardware updates the read-only PWMx Current Duty Cycle register on the beginning of a PWM cycle. If Ramp Rate Control is disabled, the delay to read back the programmed value will be from 0 seconds to 1/(PWM frequency) seconds. Typically, the delay will be 1/(2*PWM frequency) seconds.

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27.2.8 Register 33h-3Dh: Reserved**27.2.9 Register 3Eh: Company ID**

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	5Ch

The Company ID register contains the company identification number. This number is a method for uniquely identifying the part manufacturer.

This register is read only – a write to this register has no effect.

27.2.10 Register 3Fh: Version / Stepping

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
3Fh	R	Version / Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	89h Note 27.14

Note 27.14 Version / Stepping number can range from 89h to 8Fh. The initial Version / Stepping number is 89h. Contact SMSC for latest Version / Stepping number.

The four least significant bits of the Version / Stepping register [3:0] contain the current stepping of the SCH5017 silicon. The four most significant bits [7:4] reflect the version number.

The register is used by application software to identify which device has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-arounds for bugs found in a specific silicon stepping. This register is read only – a write to this register has no effect.

27.2.11 Register 40h: Ready/Lock/Start Monitoring

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
40h	R/W	Ready/Lock/Start	RES	RES	START Default	Vbat Mon	OVRID	READY	LOCK Note 27.17	START Note 27.16	00h

Setting the Lock bit makes the Lock and Start bits read-only.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	START (Note 27.18)	R/W	0 Note 27.16	When software writes a 1 to this bit, the SCH5017 enables monitoring and PWM output control functions based on the limit and parameter registers. Before this bit is set, the part does not update register values. Whenever this bit is set to 0, the monitoring and PWM output control functions are based on the default limits and parameters, regardless of the current values in the limit and parameter registers. The SCH5017 preserves the values currently stored in the limit and parameter registers when this bit is set or cleared. This bit becomes read only when the Lock bit is set. When this bit is 0, all fans are on full 100% duty cycle (256/256). When this bit is 0, the part is not monitoring. It is expected that all limit and parameter registers will be set by BIOS or application software prior to setting this bit because these registers cannot be written once the start bit is set.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
1	LOCK	R/W	0 Note 27.17	Setting this bit to 1 locks specified limit and parameter registers. Once this bit is set, limit and parameter registers become read only and will remain locked until the device is powered off. This register bit becomes read only once it is set.
2	READY	R	0	The SCH5017 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are functioning (all bias conditions for the A/Ds have stabilized and the A/Ds are in operational mode). (Always reads back '1'.)
3	OVRID	R/W	0	If this bit is set to 1, all PWM outputs go to 100% duty cycle regardless of whether or not the lock bit is set.
4	Vbat Monitoring Enable	R/W (Note 27.16)	0	The Vbat Monitoring Enable bit determines if Vbat will be monitored on the next available monitoring cycle. This is a read/write bit. Writing this bit to a '1' will enable the Vbat input to be monitored on the next available monitoring cycle. Writing this bit to a '0' has no effect. This bit is cleared on an HVTR POR or when the Vbat register is updated. Software can poll this bit for a '0' after setting it to a '1' to determine when the Vbat register has been updated. 0 = Vbat input is not being monitored (default) 1 = Vbat input is being monitored The lock bit has no effect on this register bit.
5	START Default	R/W	0	This bit controls which Power On Reset is used to set Bit[1] START of this register to its default value. 0 = Reset START bit on VTR POR 1 = Reset START bit on VCC POR
6-7	Reserved	R	0	Reserved

Note 27.15 This bit is set by software and cleared by hardware. Writing a '0' to this register has no effect.

Note 27.16 The START bit is Reset on a VTR POR by default. Setting Bit[5] START_DEFAULT in this register to '1' will cause the START bit to be reset to its default value on a VCC POR.

Note 27.17 The LOCK bit is cleared on a VCC POR.

Note 27.18 There is a start-up time of up to 247ms (default - see [Table 25.2, "Conversion Cycle Timing," on page 193](#)) for monitoring after the start bit is set to '1', during which time the reading registers are not valid. Software can poll the TRDY bit located in the Configuration Register (7Fh) to determine when the voltage and temperature readings are valid. The following summarizes the operation of the part based on the Start bit:

1. If Start bit = '0' then:
 - a. Fans are set to Full On.
 - b. No voltage, temperature, or fan tach monitoring is performed. The values in the reading registers will be N/A (Not Applicable), which means these values will not be considered valid readings until the Start bit = '1'. The exception to this is the Tachometer reading registers, which always give the actual reading on the TACH pins.
 - c. No Status bits are set.
2. If Start bit = '1'
 - a. All fan control and monitoring will be based on the current values in the registers. There is no need to preserve the default values after software has programmed these registers because no monitoring or auto fan control will be done when Start bit = '0'.
 - b. Status bits may be set.

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- c. The limit and parameter registers are read-only when the start bit is 1. Only the Current PWM Duty Cycle and Ready/Lock /Start registers are writable when the associated fan is in manual mode. The INTEN bit in register 7Ch is also writable when the start bit is set.

Note: Once programmed, the register values will be saved when start bit is reset to '0'.

27.2.12 Register 41h: Interrupt Status Register 1

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
41h	R-C (See Note 27.19)	Interrupt Status 1	INT23	D2	AMB	D1	5V	VCC	Vccp	5VTR	00h Note 27.20
Note 27.19 This register is cleared on a read if no events are active. Note 27.20 This register is reset to its default value on a VCC POR.											

This register is read only – a write to this register has no effect.

Note: The individual enable bits for D2, AMB, and D1 are located in the Interrupt Enable 3 (Temp) register at offset 82h. The individual enable bits for 5V, VCC, Vccp, and 5VTR are located in the Interrupt Enable 1 register at offset 7Eh.

The Interrupt Status Register 1 bits are automatically set by the device whenever the 5VTR, Vccp, VCC, or 5V input voltages violate the limits set in the corresponding voltage limit registers or when the measured temperature on Remote Diode 1, Remote Diode 2, or the Ambient Temperature violates the limits set in the corresponding temperature limit registers.

This register holds a bit set until the event is read by software or until the individual enable bit is cleared (see Note below). The contents of this register are cleared (set to 0) automatically by the SCH5017 after it is read by software, if the voltage or temperature no longer violates the limits set in the limit and parameter registers. Once set, the Interrupt Status Register 1 bits remain set until a read event occurs or until the individual enable bits is cleared, even if the voltage or temperature no longer violate the limits set in the limit registers. Note that clearing the group Temp, Fan, or Volt enable bits or the global INTEN enable bit has no effect on the status bits. See [Registers 44-4Dh, 9B-9Eh: Voltage Limit Registers on page 244](#) and [Registers 4E-53h: Temperature Limit Registers on page 245](#).

This register contains a bit that indicates that a bit is set in the other interrupt status registers. If bit 7 is set, then a status bit is set in either the Interrupt Status Register 2 Register or the Interrupt Status Register 3 Register. Therefore, S/W can poll this register, and only if bit 7 is set does the other registers need to be read. This bit is cleared (set to 0) automatically by the device if there are no bits set in either the Interrupt Status Register 2 or the Interrupt Status Register 3.

This register is read only – a write to this register has no effect.

Note:

Clearing the individual enable bits. There are two cases and in both cases it is not possible to change the individual interrupt enable while the start bit is set.

1. The interrupt status bit is not set when you clear the individual interrupt enable. Here the interrupt status bit will not get set when you set the start bit. Regardless of whether the limits are violated during a measurement.
2. An interrupt status bit had been set from a previous condition. So you clear the start bit and then clear the individual interrupt enable. The associated interrupts status bit will not be cleared immediately, but will be cleared when the start bit is set when the associated reading register is updated.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	5VTR_Error	R	0	The SCH5017 automatically sets this bit to 1 when the 5VTR input voltage is less than or equal to the limit set in the 5VTR Low Limit register or greater than the limit set in the 5VTR High Limit register.
1	Vccp_Error	R	0	The SCH5017 automatically sets this bit to 1 when the Vccp input voltage is less than or equal to the limit set in the Vccp Low Limit register or greater than the limit set in the Vccp High Limit register.
2	VCC_Error	R	0	The SCH5017 automatically sets this bit to 1 when the VCC input voltage is less than or equal to the limit set in the VCC Low Limit register or greater than the limit set in the VCC High Limit register.
3	5V_Error	R	0	The SCH5017 automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Remote Diode 1 Limit Error	R	0	The SCH5017 automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ is less than or equal to the limit set in the Remote Diode 1 Low Temp register or greater than the limit set in Remote Diode 1 High Temp register.
5	Internal Sensor Limit Error	R	0	The SCH5017 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal Low Temp register or greater than the limit set in the Internal High Temp register.
6	Remote Diode 2 Limit Error	R	0	The SCH5017 automatically sets this bit to 1 when the temperature input measured by the Remote2- and Remote2+ is less than or equal to the limit set in the Remote Diode 2 Low Temp register or greater than the limit set in the Remote Diode 1 High Temp register.
7	INT23 Event Active	R	0	The device automatically sets this bit to 1 when a status bit is set in the Interrupt Status Register 2 or Interrupt Status Register 3.

27.2.13 Register 42h: Interrupt Status Register 2

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
42h	R-C (See Note 27.21)	Interrupt Status Register 2	ERR2	ERR1	FANTAC H4	FANTA CH3	FANTAC H2	FANTA CH1	RES	12V	00h Note 27.22
Note 27.21 This register is cleared on a read if no events are active.											
Note 27.22 This register is reset to its default value on a VCC POR.											

This register is read only – a write to this register has no effect.

The Interrupt Status Register 2 bits is automatically set by the device whenever a remote temperature sensor error occurs, a tach reading value is above the minimum value set in the tachometer minimum registers, or whenever the 12V input voltage violates the limits set in the limit and parameter registers. The Interrupt Status Register 2 register holds a set bit until the event is read by software or until the individual interrupt enable bit is cleared.

This register holds a bit set until the event is read by software or until the individual enable bit is cleared (see Note below). The contents of this register are cleared (set to 0) automatically by the SCH5017 after it is read by software, if the voltage no longer violate the limits set in the limit and parameter registers, if the temperature sensor error no longer exists, or if the tach reading register is no longer above the minimum. Once set, the Interrupt Status Register 2 bits remain set until a read event occurs or until the individual interrupt enable bit is cleared, even if the voltage, Tach, or diode event no longer exists.

The remote diode fault bits do not clear on a read while the fault condition exists. If the start bit is set when a fault condition occurs, 80h will be loaded into the associated temperature reading register, which will cause the associated diode limit error bit to be set (Remote Diode 1 Limit Error or Remote

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Diode 2 Limit Error) in addition to the diode fault bit. Disabling the enable bit for the diode will clear both the fault bit and the error bit for that diode (see Note below).

This register is read only – a write to this register has no effect.

Note:

Clearing the individual enable bits. There are two cases and in both cases it is not possible to change the individual interrupt enable while the start bit is set.

1. The interrupt status bit is not set when you clear the individual interrupt enable. Here the interrupt status bit will not get set when you set the start bit. Regardless of whether the limits are violated during a measurement.
2. An interrupt status bit had been set from a previous condition. So you clear the start bit and then clear the individual interrupt enable. The associated interrupts status bit will not be cleared immediately, but will be cleared when the start bit is set when the associated reading register is updated.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	+12v_Error	R	0	The SCH5017 automatically sets this bit to 1 when the 12V input voltage is less than or equal to the limit set in the 12V Low Limit register or greater than the limit set in the 12V High Limit register.
1	Reserved	R	0	Reserved
2	FANTACH1 Slow/Stalled	R	0	The SCH5017 automatically sets this bit to 1 when the FANTACH1 input reading is above the value set in the Tach1 Minimum MSB and LSB registers.
3	FANTACH2 Slow/Stalled	R	0	The SCH5017 automatically sets this bit to 1 when the FANTACH2 input reading is above the value set in the Tach2 Minimum MSB and LSB registers.
4	FANTACH3 Slow/Stalled	R	0	The SCH5017 automatically sets this bit to 1 when the FANTACH3 input reading is above the value set in the Tach3 Minimum MSB and LSB registers.
5	FANTACH4 Slow/Stalled	R	0	The SCH5017 automatically sets this bit to 1 when the FANTACH4 input reading is above the value set in the Tach4 Minimum MSB and LSB registers.
6	Remote Diode 1 Fault	R	0	The SCH5017 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote1+ or Remote1- thermal diode input pins as defined in the section Diode Fault on page 198 . Note: If the START bit is set and a fault condition exists, the Remote Diode 1 reading register will be forced to 80h.
7	Remote Diode 2 Fault	R	0	The SCH5017 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote2+ or Remote2- thermal diode input pins as defined in the section Diode Fault on page 198 . Note: If the START bit is set and a fault condition exists, the Remote Diode 2 reading register will be forced to 80h.

27.2.14 Register 43h: VID

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
43h	R	VID	RES	RES	VID5	VID4	VID3	VID2	VID1	VID0	N/A

The VID register contains the values of SCH5017 VID0-VID5 input pins. This register indicates the status of the VID lines that interconnect the processor to the Voltage Regulator Module (VRM). Software uses the information in this register to determine the voltage that the processor is designed to operate at. With this information, software can then dynamically determine the correct values to place in the Vccp Low Limit and Vccp High Limit registers.

Note: The VID5 bit returns 0 when the VID5/FANTACH3 pin is configured for the alternate function FANTACH3

This register is read only – a write to this register has no effect.

27.2.15 Registers 44-4Dh, 9B-9Eh: Voltage Limit Registers

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
44h	R/W	5VTR Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	5VTR High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	Vccp Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	Vccp High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	VCC Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	VCC High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh
9Bh	R/W	VTR Low Limit	7	6	5	4	3	2	1	0	00h
9Ch	R/W	VTR High Limit	7	6	5	4	3	2	1	0	FFh
9Dh	R/W	Vbat Low Limit	7	6	5	4	3	2	1	0	00h
9Eh	R/W	Vbat High Limit	7	6	5	4	3	2	1	0	FFh

Setting the Lock bit has no effect on these registers.

If a voltage input either exceeds the value set in the voltage high limit register or falls below or equals the value set in the voltage low limit register, the corresponding bit will be set automatically by the SCH5017 in the interrupt status registers (41-42h, 83h). Voltages are presented in the registers at $\frac{1}{4}$ full scale for the nominal voltage, meaning that at nominal voltage, each register will read C0h, except for the Vbat input. Vbat is nominally a 3.0V input that is implemented on a +3.3V (nominal) analog input. Therefore, the nominal reading for Vbat is AEh.

Note: Vbat will only be monitored when the Vbat Monitoring Enable bit is set to '1'. Updating the Vbat reading register automatically clears the Vbat Monitoring Enable bit.

Table 27.5 Voltage Limits vs. Register Setting

INPUT	NOMINAL VOLTAGE	REGISTER READING AT NOMINAL VOLTAGE	MAXIMUM VOLTAGE	REGISTER READING AT MAXIMUM VOLTAGE	MINIMUM VOLTAGE	REGISTER READING AT MINIMUM VOLTAGE
VTR	3.3V	C0h	4.38V	FFh	0V	00h
Vbat (Note)	3.0V	AEh	4.38V	FFh	0V	00h
5VTR	5.0V	C0h	6.64V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

Note: Vbat is a nominal 3.0V input source that has been implemented on a 3.3V analog voltage monitoring input.

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27.2.16 Registers 4E-53h: Temperature Limit Registers

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
4Eh	R/W	Remote Diode 1 Low Temp	7	6	5	4	3	2	1	0	81h
4Fh	R/W	Remote Diode 1 High Temp	7	6	5	4	3	2	1	0	7Fh
50h	R/W	Internal Low Temp	7	6	5	4	3	2	1	0	81h
51h	R/W	Internal High Temp	7	6	5	4	3	2	1	0	7Fh
52h	R/W	Remote Diode 2 Low Temp	7	6	5	4	3	2	1	0	81h
53h	R/W	Remote Diode 2 High Temp	7	6	5	4	3	2	1	0	7Fh

Setting the Lock bit has no effect on these registers.

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or is less than or equal to the value set in the low limit register, the corresponding bit will be set automatically by the SCH5017 in the Interrupt Status Register 1 (41h). For example, if the temperature reading from the Remote1- and Remote1+ inputs exceeds the Remote Diode 1 High Temp register limit setting, Bit[4] D1 of the Interrupt Status Register 1 will be set. The temperature limits in these registers are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in [Table 27.6](#).

Table 27.6 Temperature Limits vs. Register Settings

TEMPERATURE	LIMIT (DEC)	LIMIT (HEX)
-127°C	-127	81h
.	.	.
.	.	.
-50°C	-50	CEh
.	.	.
.	.	.
0°C	0	00h
.	.	.
.	.	.
50°C	50	32h
.	.	.
.	.	.
127°C	127	7Fh

27.2.17 Registers 54h-5Bh: Fan Tachometer Low Limit

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
54h	R/W	FANTACH1 Minimum LSB	7	6	5	4	3	2	1	0	FFh
55h	R/W	FANTACH1 Minimum MSB	15	14	13	12	11	10	9	8	FFh
56h	R/W	FANTACH2 Minimum LSB	7	6	5	4	3	2	1	0	FFh
57h	R/W	FANTACH2 Minimum MSB	15	14	13	12	11	10	9	8	FFh
58h	R/W	FANTACH3 Minimum LSB	7	6	5	4	3	2	1	0	FFh
59h	R/W	FANTACH3 Minimum MSB	15	14	13	12	11	10	9	8	FFh
5Ah	R/W	FANTACH4 Minimum LSB	7	6	5	4	3	2	1	0	FFh
5Bh	R/W	FANTACH4 Minimum MSB	15	14	13	12	11	10	9	8	FFh

Setting the Lock bit has no effect on these registers.

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. An interrupt status event will be generated when the tachometer reading is greater than the minimum tachometer limit.

The fan tachometer will not cause a bit to be set in the interrupt status register if the current value in the associated Current PWM Duty registers is 00h or if the PWM is disabled via the PWM Configuration Register.

Interrupts will never be generated for a fan if its tachometer minimum is set to FFFFh.

27.2.18 Registers 5C-5Eh: PWM Configuration

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
5Ch	R/W	PWM 1 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h
5Dh	R/W	PWM 2 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h
5Eh	R/W	PWM 3 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Bits [7:5] Zone/Mode

Bits [7:5] of the PWM Configuration registers associate each PWM with a temperature sensor.

- When in Auto Fan Mode, the PWM will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If 'Hottest' option is selected (101 or 110), the PWM will be controlled by the hottest of zones 2 and 3, or of zones 1, 2, and 3. If one of these options is selected, the PWM is controlled by the limits and parameters for the zone that requires the highest PWM duty cycle, as computed by the auto fan algorithm.
- When in manual control mode, the PWMx Current Duty Cycle Registers (30h-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. See PWMx Current Duty Cycle Registers description.
- When the fan is disabled (100) the corresponding PWM output is driven low (or high, if inverted).
- When the fan is Full On (011) the corresponding PWM output is driven high (or low, if inverted).

Datasheet**Note:**

- Zone 1 is controlled by Remote Diode 1 Temp Reading register
- Zone 2 is controlled by Internal Temp Reading Register or Remote Diode 2 (see Bit[1] Zone 2 Select in the [Register 7Fh: Configuration Register on page 256.](#))
- Zone 3 is controlled by Remote Diode 2 Temp Reading register

Table 27.7 Fan Zone Setting

ZON[7:5]	PWM CONFIGURATION
000	Fan on zone 1 auto
001	Fan on zone 2 auto
010	Fan on zone 3 auto
011	Fan always on full
100	Fan disabled
101	Fan controlled by hottest of zones 2,3
110	Fan controlled by hottest of zones 1,2,3
111	Fan manually controlled

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 1, 100% duty cycle will yield an output that is low for 255 clocks and high for 1 clock. If set to 0, 100% duty cycle will yield an output that is high for 255 clocks and low for 1 clock.

Bit [3] Reserved**Bits [2:0] Spin Up**

Bits [2:0] specify the 'spin up' time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in the table below before scaling to a lower speed. Note: during spin-up, the PWM pin is forced high for the duration of the spin-up time (i.e., 100% duty cycle = 256/256)

Note: To reduce the spin-up time, this device has implemented a feature referred to as Spin Up Reduction. Spin Up Reduction uses feedback from the tachometers to determine when each fan has started spinning properly. Spin up for a PWM will end when the tachometer reading register is below the minimum limit, or the spin-up time expires, whichever comes first. All tachs associated with a PWM must be below min. for spin-up to end prematurely. This feature can be disabled by clearing bit 4 (SUREN) of the Configuration register (7Fh). If disabled, the all fans go on full for the duration of their associated spin up time. Note that the Tachx minimum registers must be programmed to a value less than FFFFh in order for the spin-up reduction to work properly.

Table 27.8 Fan Spin-Up Register

SPIN[2:0]	SPIN UP TIME
000	0 sec
001	100ms
010	250ms (default)
011	400ms
100	700ms
101	1000ms
110	2000ms
111	4000ms

27.2.19 Registers 5F-61h, A7-A8h: Zone Temperature Range, PWM Frequency

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
5Fh	R/W	Zone 1 Range / Fan 1 Frequency	RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh
60h	R/W	Zone 2 Range / Fan 2 Frequency	RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh
61h	R/W	Zone 3 Range / Fan 3 Frequency	RAN3	RAN2	RAN1	RAN0	FRQ3	FRQ2	FRQ1	FRQ0	CBh
A7h	R/W	Fan 4 Frequency	RES	RES	RES	RES	FRQ3	FRQ2	FRQ1	FRQ0	0Bh
A8h	R/W	Fan 5 Frequency	RES	RES	RES	RES	FRQ3	FRQ2	FRQ1	FRQ0	0Bh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan Mode, when the temperature for a zone is above the Low Temperature Limit (registers 67-69h) and below the Absolute Temperature Limit (registers 6A-6Ch) the speed of a fan assigned to that zone is determined as follows by the auto fan control logic.

When the temperature reaches the temperature value programmed in the Zone x Low Temp Limit register, the PWM output assigned to that zone is at PWMx Minimum Duty Cycle. Between Zone x Low Temp Limit and (Zone x Low Temp Limit + Zone x Range), the PWM duty cycle increases linearly according to the temperature as shown in the figure below.

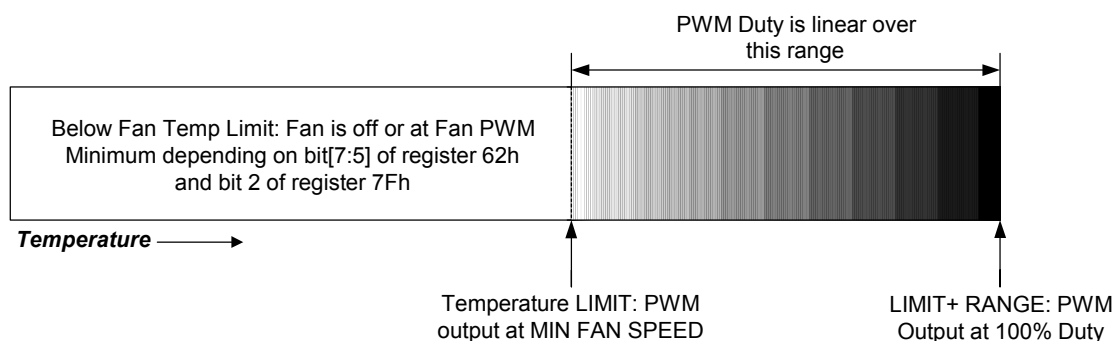


Figure 27.1 Fan Activity Above Fan Temp Limit

Example for PWM1 assigned to Zone 1:

- Zone 1 Low Temp Limit (Register 67h) is set to 50°C (32h).
- Zone 1 Range (Register 5Fh) is set to 8°C (7h)
- PWM1 Minimum Duty Cycle (Register 64h) is set to 50% (80h)

In this case, the PWM1 duty cycle will be 50% at 50°C.

Since (Zone 1 Low Temp Limit) + (Zone 1 Range) = 50°C + 8°C = 58°C, the fan controlled by PWM1 will run at 100% duty cycle when the temperature of the Zone 1 sensor is at 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (Zone 1 Low Temp Limit) + (Zone 1 Range), the duty cycle must be 100%.

The PWM frequency bits [3:0] determine the PWM frequency for the fan. If the high frequency option is selected the associated FANTACH inputs must be configured for Mode 1.

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27.2.19.1 PWM Frequency Selection (Default =1011 bits=25kHz)**Table 27.9 PWM Frequency Selection**

FREQUENCY SELECT BITS[3:0]	FREQUENCY 14.318MHZ CLOCK SOURCE
0000	11.0 Hz
0001	14.6 Hz
0010	21.9 Hz
0011	29.3 Hz
0100	35.2 Hz
0101	44.0 Hz
0110	58.6 Hz
0111	87.7 Hz
1000	15kHz
1001	20kHz
1010	30kHz
1011	25kHz (default)
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

27.2.19.2 Range Selection (Default =1100=32°C)**Table 27.10 Register Setting vs. Temperature Range**

RAN[3:0]	RANGE (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32
1101	40
1110	53.33
1111	80

Note: The range numbers will be used to calculate the slope of the PWM ramp up. For the fractional entries, the PWM will go on full when the temp reaches the next integer value e.g., for 3.33, PWM will be full on at (min. temp + 4).

27.2.20 Register 62h, 63h: PWM Ramp Rate Control

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
62h	R/W	PWM 1 Ramp Rate Control	RES1	RES1	RES1	RES	RR1E	RR1-2	RR1-1	RR1-0	E0h
63h	R/W	PWM 2, PWM 3 Ramp Rate Control	RR2E	RR2-2	RR2-1	RR2-0	RR3E	RR3-2	RR3-1	RR3-0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Description of RES1 Bits: These bits are reserved, reads return 1, writes are ignored.

Description of Ramp Rate Control bits:

If the Remote1 or Remote2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the part. The auto fan control logic calculates the PWM duty cycle for all temperature readings. If Ramp Rate Control is disabled, the PWM output will jump or oscillate between different PWM duty cycles causing the fan to suddenly change speeds, which creates unwanted fan noise. If enabled, the PWM Ramp Rate Control logic will prevent the PWM output from jumping, instead the PWM will ramp up/down towards the new duty cycle at a pre-determined ramp rate.

Ramp Rate Control

The Ramp Rate Control logic limits the amount of change to the PWM duty cycle over a period of time. This period of time is programmable via the Ramp Rate Control bits. For a detailed description of the Ramp Rate Control bits see [Table 27.11](#). For a description of the Ramp Rate Control logic see [Ramp Rate Control Logic on page 216](#).

Notes:

- RR1E, RR2E, and RR3E enable PWM Ramp Rate Control for PWM 1, 2, and 3 respectively.
- RR1-2, RR1-1, and RR1-0 control ramp rate time for PWM 1
- RR2-2, RR2-1, and RR2-0 control ramp rate time for PWM 2
- RR3-2, RR3-1, and RR3-0 control ramp rate time for PWM 3

Table 27.11 Ramp Rate Control Bits

RRX-[2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
000	35	52.53	206 msec	4.85
001	17.6	26.52	104 msec	9.62
010	11.8	17.595	69 msec	14.49
011	7.0	10.455	41 msec	24.39
100	4.4	6.63	26 msec	38.46
101	3.0	4.59	18 msec	55.56
110	1.6	2.55	10 msec	100

Table 27.11 Ramp Rate Control Bits (continued)

RRX-[2:0]	PWM RAMP TIME (SEC) (TIME FROM 33% DUTY CYCLE TO 100% DUTY CYCLE)	PWM RAMP TIME (SEC) (TIME FROM 0% DUTY CYCLE TO 100% DUTY CYCLE)	TIME PER PWM STEP (PWM STEP SIZE = 1/255)	PWM RAMP RATE (HZ)
111	0.8	1.275	5 msec	200

Note: This assumes the Ramp Rate Enable bit (RRxE) is set.

27.2.21 Registers 64-66h: Minimum PWM Duty Cycle

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
64h	R/W	PWM1 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h
65h	R/W	PWM2 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h
66h	R/W	PWM3 Minimum Duty Cycle	7	6	5	4	3	2	1	0	80h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These registers specify the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting in Auto Fan Control Mode.

Table 27.12 PWM Duty vs. Register Setting

MINIMUM PWM DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
.	.	.
.	.	.
.	.	.
25%	64	40h
.	.	.
.	.	.
.	.	.
50%	128	80h
.	.	.
.	.	.
.	.	.
100%	255	FFh

27.2.22 Registers 67-69h: Zone Low Temperature Limit

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
67h	R/W	Zone 1 Low Temp Limit	7	6	5	4	3	2	1	0	80h
68h	R/W	Zone 2 Low Temp Limit	7	6	5	4	3	2	1	0	80h
69h	R/W	Zone 3 Low Temp Limit	7	6	5	4	3	2	1	0	80h

APPLICATION NOTE: All three Zone x Low Temp Limit (67h, 68h and 69h) must be written to a value that is not 80h in order for autofan to operate.

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the auto fan algorithm based on the setting in the Zone x Range / PWMx Frequency register. Default = 90°C=5Ah

Table 27.13 Temperature Limit vs. Register Setting

LIMIT	LIMIT (DEC)	LIMIT (HEX)
-127°C	-127	81h
.	.	.
.	.	.
-50°C	-50	CEh
.	.	.
.	.	.
0°C	0	00h
.	.	.
.	.	.
50°C	50	32h
.	.	.
.	.	.
127°C	127	7Fh

27.2.23 Registers 6A-6Ch: Absolute Temperature Limit

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan mode, if any zone associated with a PWM output exceeds the temperature set in the Absolute limit register, all PWM outputs will increase their duty cycle to 100% except those that are disabled via the PWM Configuration registers. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event.

If an absolute limit register set to 80h (-128°C), the safety feature is disabled for the associated zone. That is, if 80h is written into the Zone x Temp Absolute Limit Register, then regardless of the reading register for the zone, the fans will not turn on-full based on the absolute temp condition.

Default =100°C=64h.

When any fan is in auto fan mode, then if the temperature in any zone exceeds absolute limit, all fans go to full, including any in manual mode, except those that are disabled. Therefore, even if a zone is not associated with a fan, if that zone exceeds absolute, then all fans go to full. In this case, the absolute limit can be chosen to be 7Fh for those zones that are not associated with a fan, so that the fans won't turn on unless the temperature hits 127 degrees.

Table 27.14 Absolute Limit vs. Register Setting

ABSOLUTE LIMIT	ABS LIMIT (DEC)	ABS LIMIT (HEX)
-127°C	-127	81h
.	.	.
.	.	.
-50°C	-50	CEh
.	.	.
.	.	.
0°C	0	00h
.	.	.
.	.	.
50°C	50	32h
.	.	.
.	.	.
127°C	127	7Fh

27.2.24 Registers 6D-6Eh: SMSC Test Registers

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Dh	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	44h
6Eh	R/W	SMSC Test Register	TST3	TST2	TST1	TST0	RES	RES	RES	RES	40h

This is a read/write register. Writing this register may produce unwanted results.

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

27.2.25 Register 6F: XOR Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
6Fh	R/W	XOR Test Register	RES	RES	RES	RES	RES	RES	RES	XEN	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

The part incorporates an XOR tree test mode. When the test mode is enabled by setting the 'XEN' bit high via SMBus, the part enters XOR test mode.

The following signals are included in the XOR test tree:

- VID0, VID1, VID2, VID3, VID4, VID5/FANTACH3
- FANTACH1, FANTACH2, FANTACH4
- PWM2, PWM3

Since the test mode is XOR tree, the order of the signals in the tree is not important. SDA and SCL are not included in the test tree.

27.2.26 Registers 70h-78h: SMSC Test Registers

SMSC Test registers are read/write registers. Writing to these registers may cause unwanted results.

27.2.27 Register 79h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
79h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is a read/write register. Writing this register may produce unwanted results.

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

27.2.28 Register 7Ah: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Ah	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is a read/write register. Writing this register may produce unwanted results.

27.2.29 Register 7Bh: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Bh	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is a read/write register. Writing this register may produce unwanted results.

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

27.2.30 Register 7Ch: Special Function Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Ch	R/W	Special Function	AVG2	AVG1	AVG0	SMSC	ZN1_SEL	INTEN	MONMD	LPMD	40h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register contains the following bits:

Bit[0] Low-Power Mode Select

0= Sleep Mode (default)

1= Shutdown Mode

Bit[1] Monitoring Mode Select

0= Continuous Monitor Mode (default)

1= Cycle Monitor Mode

Datasheet**Bit[2] nHWM_INT Enable**

0=Disables nHWM_INT pin output function (default)

1=Enables nHWM_INT pin output function

Bit[3] Zone 1 Select

This bit controls the temperature sensor for Zone 1 as it pertains to the auto fan control. This bit has no effect on the Remote Diode 1 or Remote Diode 2 sensor status events.

0= Zone 1 is controlled by Remote Diode 1 (default)

1= Zone 1 is controlled by Remote Diode 2

Bit [4] SMSC Reserved

This is a read/write bit. Reading this bit has no effect. Writing this bit to '1' may cause unwanted results.

Bits [7:5] AVG[2:0]

The AVG[2:0] bits determine the amount of averaging for each of the six measurements that are performed by the hardware monitor before the reading registers are updated. The AVG[2:0] bits are priority encoded where the most significant bit has highest priority. For example, when the AVG2 bit is asserted, 32 averages will be performed for each measurement before the reading registers are updated regardless of the state of the AVG[1:0] bits.

SFTR[7:5]			AVERAGES PER READING			
AVG2	AVG1	AVG0	REM DIODE 1	REM DIODE 2	INTERNAL DIODE	All Voltage Readings (+5VTR, +5V, +12V, Vccp, VTR, Vbat, and VCC)
0	0	0	128	128	8	8
0	0	1	16	16	1	1
0	1	X	16	16	16	16
1	X	X	32	32	32	32

Note: The default for the AVG[2:0] bits is '010'b.

27.2.31 Register 7Dh: Reserved**27.2.32 Register 7Eh: Interrupt Enable 1 Register**

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Eh	R/W	Interrupt Enable 1 (Voltages)	VCC	12V	5V	VTR	VCCP	5VTR	VBAT	VOLT	ECh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register is used to enable individual voltage error events to set the corresponding status bits in the interrupt status registers. This register also contains the group voltage enable bit (Bit[0] VOLT), which is used to enable voltage events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] Group interrupt Voltage Enable (VOLT)

0=Out-of-limit voltages do not affect the state of the nHWM_INT pin (default)

1=Enable out-of-limit voltages to make the nHWM_INT pin active low

Bit[1] VBAT Error Enable

Bit[2] 5VTR Error Enable

Bit[3] Vccp Error Enable

Bit[4] VTR Error Enable

Bit[5] 5V Error Enable

Bit[6] 12V Error Enable

Bit[7] VCC Error Enable

The individual voltage error event bits are defined as follows:

0=disable

1=enable.

See [Figure 25.1 Interrupt Control on page 197](#).

27.2.33 Register 7Fh: Configuration Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
7Fh	R/W	Configuration	INIT	SMSC	SMSC	SUREN	TRDY Note 27.23	VID5 / FANTACH3	ZN2 Sel	SMSC	10h

Note 27.23 This bit is reset on a VCC POR

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register contains the following bits:

Bit[0] SMSC Reserved

This is an SMSC Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[1] Zone 2 Select

This bit controls the temperature sensor for Zone 2 as it pertains to the auto fan control. This bit has no effect on the Ambient Temperature sensor status events.

0= Zone 2 is controlled by Ambient Temperature Sensor (default)

1= Zone 2 is controlled by Remote Diode 2

Bit[2] VID5/FANTACH3

This bit is the alternate function select bit for the VID5/FANTACH3 input pin.

0=VID5 (default)

1=FANTACH3

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Bit[3] TRDY: Temperature Reading Ready. This bit indicates that the temperature reading registers have valid values. This bit is used after writing the start bit to '1'. 0= not valid, 1=valid.

Bit[4] SUREN: Spin-up reduction enable. This bit enables the reduction of the spin-up time based on feedback from all fan tachometers associated with each PWM. 0=disable, 1=enable (default)

Bit[5] SMSC Reserved

This is an SMSC Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[6] SMSC Reserved

This is an SMSC Reserved bit. Writing this bit to a value different than the default value may cause unwanted results.

Bit[7] Initialization

Setting the INIT bit to '1' performs a soft reset. This bit is self-clearing. Soft Reset sets all the registers except the Reading Registers to their default values.

27.2.34 Register 80h: Interrupt Enable 2 Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
80h	R/W	Interrupt Enable 2 (Fan Tachs)	RES	FAN-TACH B	FAN-TACH A	FANTA CH4	FANTA CH3	FANTA CH2	FANTA CH1	FAN-TACH	7Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual fan tach error events to set the corresponding status bits in the interrupt status registers. This register also contains the group fan tach enable bit (Bit[0] TACH), which is used to enable fan tach events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

This register contains the following bits:

Bit[0] FANTACH (Group TACH Enable)

0=Out-of-limit tachometer readings do not affect the state of the nHWM_INT pin (default)

1=Enable out-of-limit tachometer readings to make the nHWM_INT pin active low

Bit[1] Fantach 1 Event Enable

Bit[2] Fantach 2 Event Enable

Bit[3] Fantach 3 Event Enable

Bit[4] Fantach 4 Event Enable

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual fan tach error event bits are defined as follows:

0=disable

1=enable.

See [Figure 25.1 Interrupt Control on page 197](#).

27.2.35 Register 81h: TACH_PWM Association Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
81h	R/W	TACH_PWM Association	T4H	T4L	T3H	T3L	T2H	T2L	T1H	T1L	A4h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to associate a PWM with a tachometer input. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers.

The fan tachometer will not cause a bit to be set in the interrupt status register:

- if the current value in Current PWM Duty registers is 00h or
- if the fan is disabled via the Fan Configuration Register.

Note: A bit will never be set in the interrupt status for a fan if its tachometer minimum is set to FFFFh.

See bit definition below.

Bits[1:0] Tach1. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[3:2] Tach2. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[5:4] Tach3. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[7:6] Tach4. These bits determine the PWM associated with this Tach. See bit combinations below.

BITS[1:0], BITS[3:2], BITS[5:4], BITS[7:6]	PWM ASSOCIATED WITH TACHX
00	PWM1
01	PWM2
10	PWM3
11	Reserved

Notes:

- Any PWM that has no TACH inputs associated with it must be configured to operate in Mode 1.
- All TACH inputs must be associated with a PWM output. If the tach is not being driven by the associated PWM output it should be configured to operate in Mode 1 and the associated TACH interrupt must be disabled.

27.2.36 Register 82h: Interrupt Enable 3 Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
82h	R/W	Interrupt Enable 3 (Temp)	RES	RES	RES	RES	D2EN	D1EN	AMB	TEMP	0Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable individual thermal error events to set the corresponding status bits in the interrupt status registers. This register also contains the group thermal enable bit (Bit[0] TEMP), which is used to enable thermal events to force the interrupt pin (nHWM_INT) low if interrupts are enabled (see Bit[2] INTEN of the Special Function register at offset 7Ch).

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This register contains the following bits:

Bit[0] TEMP. Group temperature enable bit.

0=Out-of-limit temperature readings do not affect the state of the nHWM_INT pin (default)

1=Enable out-of-limit temperature readings to make the nHWM_INT pin active low

Bit[1] Ambient Temperature Status Enable bit.

Bit[2] Remote Diode 1 Temperature Status Enable bit.

Bit[3] Remote Diode 2 Temperature Status Enable bit

Bit[4] Reserved

Bit[5] Reserved

Bit[6] Reserved

Bit[7] Reserved

The individual thermal error event bits are defined as follows:

0=disable

1=enable.

See [Figure 25.1 Interrupt Control on page 197](#).

27.2.37 Register 83h: Interrupt Status Register 3

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
83h	R-C ¹	Interrupt Status 3	FANTACHB	FANTACHA	RES	RES	RES	RES	Vbat	VTR	00h

Note: This register is cleared on a read if no events are active

The Interrupt Status Register 3 bits[1:0] are automatically set by the device whenever a voltage event occurs on the VTR or Vbat inputs. A voltage event occurs when any of these inputs violate the limits set in the corresponding limit registers.

The Interrupt Status Register 3 bits [7:6] are automatically set by the device whenever a tachometer event occurs on the FANTACHA or FANTACHB inputs. A tachometer event occurs when any of these inputs violate the limits set in the corresponding limit registers

This register holds a set bit until the event is read by software or until the individual enable bit is cleared. The contents of this register are cleared (set to 0) automatically by the device after it is read by software, if the voltage or tachometer reading no longer violate the limits set in the limit and parameter registers. Once set, the Interrupt Status Register 3 bits remain set until a read event occurs or until the individual enable bits is cleared, even if the voltage or tachometer reading no longer violate the limits set in the limit registers. Note that clearing the group Temp, Fan, or Volt enable bits or the global INTEN enable bit has no effect on the status bits.

Note: The individual enable bits for VTR and Vbat are located in the Interrupt Enable 1 register at offset 7Eh. The individual enable bits for the FANTACH status bits are located in the Interrupt Enable 2 register at offset 80h.

This register is read only – a write to this register has no effect.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	VTR_Error	R	0	The device automatically sets this bit to 1 when the VTR input voltage is less than or equal to the limit set in the VTR Low Limit register or greater than the limit set in the VTR High Limit register.
1	Vbat_Error	R	0	The device automatically sets this bit to 1 when the Vbat input voltage is less than or equal to the limit set in the Vbat Low Limit register or greater than the limit set in the Vbat High Limit register.
2-5	Reserved	R	0	Reserved
6	FANTACHA	R	0	The SCH5017 automatically sets this bit to 1 when the FANTACHA input reading is above the value set in the TachA Minimum MSB and LSB registers.
7	FANTACHB	R	0	The SCH5017 automatically sets this bit to 1 when the FANTACHB input reading is above the value set in the TachB Minimum MSB and LSB registers.

27.2.38 Registers 84h-88h: A/D Converter LSbs Registers

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
84h	R	A/D Converter LSbs Reg 5	VTR.3	VTR.2	VTR.1	VTR.0	VB.T.3	VB.T.2	VB.T.1	VB.T.0	N/A
85h	R	A/D Converter LSbs Reg 1	RD2.3	RD2.2	RD2.1	RD2.0	RD1.3	RD1.2	RD1.1	RD1.0	N/A
86h	R	A/D Converter LSbs Reg 2	V12.3	V12.2	V12.1	V12.0	AM.3	AM.2	AM.1	AM.0	N/A
87h	R	A/D Converter LSbs Reg 3	V50.3	V50.2	V50.1	V50.0	V25.3	V25.2	V25.1	V25.0	N/A
88h	R	A/D Converter LSbs Reg 4	VCC.3	VCC.2	VCC.1	VCC.0	VCP.3	VCP.2	VCP.1	VCP.0	N/A

There is a 10-bit Analog to Digital Converter (ADC) located in the hardware monitoring block that converts the measured voltages into 10-bit reading values. Depending on the averaging scheme enabled (i.e., 16x averaging, 32x averaging, etc.), the hardware monitor may take multiple readings and average them to create 12-bit reading values. The 8 MSb's of the reading values are placed in the Reading Registers. When the upper 8-bits located in the reading registers are read the 4 LSb's are latched into their respective bits in the A/D Converter LSbs Register. This give 12-bits of resolution with a minimum value of $1/16^{\text{th}}$ per unit measured. (i.e., Temperature Range: $-127.9375\text{ }^{\circ}\text{C} < \text{Temp} < 127.9375\text{ }^{\circ}\text{C}$ and Voltage Range: $0 < \text{Voltage} < 256.9375$). See the DC Characteristics for the accuracy of the reading values.

The eight most significant bits of the 12-bit averaged readings are stored in Reading registers and compared with Limit registers. The Interrupt Status Register bits are asserted if the corresponding measured value(s) on the inputs violate their programmed limits.

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27.2.39 Register 89h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
89h	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

27.2.40 Registers 8Ah: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ah	R	SMSC Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

27.2.41 Registers 8Bh: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Bh	R/W	SMSC Test Register	RES	TST6	TST5	TST4	TST3	TST2	TST1	TST0	4Dh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

27.2.42 Registers 8Ch: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Ch	R	SMSC Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	N/A

27.2.43 Registers 8Dh: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Dh	R/W	SMSC Test Register	RES	RES	RES	TST4	TST3	TST2	TST1	TST0	N/A

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

27.2.44 Registers 8Eh: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
8Eh	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an SMSC Test register.

27.2.45 Register 8F: Reserved

27.2.46 Registers 90h-93h: FANTACHX Option Registers

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
90h	R/W	FANTACH1 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
91h	R/W	FANTACH2 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
92h	R/W	FANTACH3 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h
93h	R/W	FANTACH4 Option	RES	RES	RES	3EDG	MODE	EDG1	EDG0	SLOW	04h

Bit[0] SLOW

0= Force tach reading register to FFFFh if number of tach edges detected is greater than 0, but less than programmed number of edges. (default)

1=Force tach reading register to FFFEh if number of tach edges detected is greater than 0, but less than programmed number of edges.

Bit[2:1] The number of edges for tach1 reading:

00=2 edges

01=3 edges

10=5 edges (default)

11=9 edges

Bit[3] Tachometer Reading Mode

0=mode 1 – standard (default)

1=mode 2 – enhanced.

Note: Unused FANTACH inputs must be configured for Mode 1.

Note: Tach inputs associated with PWM outputs that are configured for high frequency mode must be configured for Mode 1.

Bit[4] 3 Edge Detection (Mode 2 only)

0=Don't ignore first 3 edges (default)

1=Ignore first 3 tachometer edges after guard time

Note: This bit has been added to support a small sampling of fans that emit irregular tach pulses when the PWM transitions 'ON'. Typically, the guard time is sufficient for most fans.

Bit[7:5] Reserved

27.2.47 Registers 94h-96h: PWMx Option Registers

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
94h	R/W	PWM1 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch

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95h	R/W	PWM2 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch
96h	R/W	PWM3 Option	RES	RES	OPP	GRD1	GRD0	SZEN	UPDT1	UPDT0	0Ch

Bits[1:0] Tachs reading registers associated with PWMx are updated: (Mode 2 only)

00=once a second (default)

01=twice a second

1x=every 300msec

Bit[2] Snap to Zero (SZEN)

This bit determines if the PWM output ramps down to OFF or if it is immediately set to zero.

0=Step Down the PWMx output to Off at the programmed Ramp Rate

1=Transition PWMx to Off immediately when the calculated duty cycle is 00h (default)

Bit[4:3] Guard time (Mode 2 only)

00=63 clocks (90kHz clocks ~ 700usec)

01=32 clocks (90kHz clocks ~ 356usec) (default)

10=16 clocks (90kHz clocks ~ 178usec)

11=8 clocks (90kHz clocks ~ 89usec)

Bit[5] Opportunistic Mode Enable

0= Opportunistic Mode Disabled. Update Tach Reading once per PWMx Update Period (see Bits[1:0] in this register)

1=Opportunistic Mode is Enabled. The tachometer reading register is updated any time a valid tachometer reading can be made. If a valid reading is detected prior to the Update cycle, then the Update counter is reset.

Bit[7:6] Reserved

27.2.48 Register 97h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
97h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	5Ah

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This is an SMSC Test Register. Writing to this register may cause unwanted results.

27.2.49 Register 98h:SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
98h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	F1h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This is an SMSC Test Register. Writing to this register may cause unwanted results.

27.2.50 Registers 99h-9Ah: Voltage Reading Registers

See [Section 27.2.4, "Registers 20-24h, 99-9Ah: Voltage Reading," on page 235.](#)

27.2.51 Registers 9B-9EH: Voltage Limit Registers

See [Section 27.2.15, "Registers 44-4Dh, 9B-9Eh: Voltage Limit Registers," on page 244.](#)

27.2.52 Register 9Fh: Reserved

27.2.53 Register A0h: SLP_S3# INT Mask Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A0h	R/W	SLP_S3# INT Mask Register	VCC	12V	5V	VTR	VCCP	5VTR	VBAT	RES	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to mask the individual voltage events from being set in the Interrupt Status Registers when the system enters the Sleep S3 state (SLP_S3# pin is low AND the SLP_S5# pin is high). Each voltage input has a corresponding status and enable bit.

- The 5V, VCC, Vccp, and 5VTR status bits are located in Interrupt Status Register 1 (41h)
- The 12V status bit is located in the Interrupt Status Register 2 (42h)
- The Vbat and VTR status bits are located in Interrupt Status Register 3 (83h).
- All the individual voltage enable bits and the group voltage enable bit are located in the Interrupt enable 1 (Voltages) register (7Eh).

To enable a voltage event onto the nHWM_INT pin, software must set the individual enable bit, the group (VOLT) enable bit, and the pin enable (INTEN) bit.

For voltage inputs that are 'OFF' in the sleep S3 state, the BIOS can configure the corresponding Mask bit to block interrupts from that voltage source when the system is in a S3 sleep state. The hardware will prevent the individual masked interrupt status bits from being set if the Mask bit is enabled and the SLP_S3# pin is asserted low and the SLP_S5# pin is high.

This register contains the following bits:

Bit[0] Reserved

Bit[1] Vbat Event Mask Enable

Bit[2] 5VTR Event Mask Enable

Bit[3] Vccp Event Mask Enable

Bit[4] VTR Event Mask Enable

Bit[5] 5V Event Mask Enable

Bit[6] 12V Event Mask Enable

Bit[7] VCC Event Mask Enable

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These bits are defined as follows:

0=Interrupt Status bit is not masked when SLP_S3# is asserted low and SLP_S5# pin is high

1=Interrupt Status bit is masked when SLP_S3# is asserted low and SLP_S5# pin is high

See [Figure 25.1 Interrupt Control on page 197](#) to see how the SLP_S3# Mask bits effect the corresponding status bits, thereby preventing an interrupt event on the nHWM_INT pin.

27.2.54 Register A1h: SMSC Reserved

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A1h	R/W	SMSC Reserved	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is an SMSC Reserved register. Writing this register to a value other than the default value may cause unwanted results.

27.2.55 Register A2h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A2h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This is an SMSC Test Register. Writing to this register may cause unwanted results.

27.2.56 Register A3h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A3h	R/W	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	00h

This is an SMSC Test Register. Writing to this register may cause unwanted results.

27.2.57 Register A4h: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A4h	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an SMSC Test register.

27.2.58 Registers A5h - A6h: PWM[A,B] Current Duty Cycle

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
------------------	------------	---------------	-------------	-------	-------	-------	-------	-------	-------	-------------	---------------

A5h	R/W	PWMA Current Duty Cycle	7	6	5	4	3	2	1	0	FFh
A6h	R/W	PWMB Current Duty Cycle	7	6	5	4	3	2	1	0	FFh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

These registers are used by software to set the PWM duty cycle for PWMA and PWMB. The Current PWM Duty registers store the duty cycle that the chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh.

The PWM duty cycle is represented as follows:

Table 27.15 PWM Duty vs Register Reading

CURRENT DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

Note: The PWMx Current Duty Cycle always reflects the current duty cycle on the associated PWM pin.

27.2.59 Registers A7h - A8h: PWMx Frequency

These registers are used to set the PWM frequency for PWMA and PWMB. For a complete description see [Section 27.2.19, "Registers 5F-61h, A7-A8h: Zone Temperature Range, PWM Frequency," on page 248.](#)

27.2.60 Registers A9h - ACh: Fan Tachometer Reading

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
A9h	R	FANTACHA Reading LSB	7	6	5	4	3	2	1	0	FEh
AAh	R	FANTACHA Reading MSB	15	14	13	12	11	10	9	8	FFh
ABh	R	FANTACHB Reading LSB	7	6	5	4	3	2	1	0	FEh
ACh	R	FANTACHB Reading MSB	15	14	13	12	11	10	9	8	FFh

Note: These registers are reset to their default value on a VCC POR.

The Fan Tachometer Reading registers can be configured to report the tach reading as the number of tach pulses per update time (TPC Mode) or in the legacy mode, which reports the number of 11.111μs periods (90KHz) between full revolutions.

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These FANTACH Reading registers default to reporting the fantach reading in the legacy mode. Bit[5] of [Registers B6h - B7h: TPC Tachx Option Register on page 268](#) is used to select the tachometer reading mode.

When the FANTACH reading registers are configured for TPC mode, the fantach reading registers return the number of tach pulses detected over the programmed update time. The update rate is programmable in Bits[1:0] [Registers B6h - B7h: TPC Tachx Option Register on page 268](#). The following equation shows how to convert the TPC reading value to an RPM value.

$$RPMs = TachReading \times Multiplier$$

The following table shows how to choose the Multiplier to convert the TPC reading to Rotations per Minute (RPM).

Table 27.16 TPC TACH Reading Converted to RPMs

TACH UPDATE RATE (SEC)	MULTIPLIER TO CONVERT TPC READING TO RPM VALUE
0.5	60
1.0	30
2.0	15

If the tach reading mode is programmed to return the tach reading in the number of clock pulses per rotation, the tachometer logic converts the TPC reading into this representation. In this mode the Fan Tachometer Reading registers contain the number of 11.111μs periods (90KHz) between full fan revolutions. Fans produce two tachometer pulses per full revolution. These registers are updated at the programmed update rate.

This reading value is represented for each fan in a 16 bit, unsigned number in either mode.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional. The START bit has no effect on these tachometer inputs.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

In legacy mode, FFFh indicates that the fan is slow or not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow). This is the maximum tachometer count value in legacy mode. In TPC mode, 0000h indicates the slow or stalled fan condition.

These registers are read only – a write to these registers has no effect.

27.2.61 Registers ADh - B0h: Fan Tachometer Low Limit (MSB, LSB)

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
ADh	R/W	FANTACHA Minimum LSB	7	6	5	4	3	2	1	0	FFh
A Eh	R/W	FANTACHA Minimum MSB	15	14	13	12	11	10	9	8	FFh
AFh	R/W	FANTACHB Minimum LSB	7	6	5	4	3	2	1	0	FFh
B0h	R/W	FANTACHB Minimum MSB	15	14	13	12	11	10	9	8	FFh

Setting the Lock bit has no effect on these registers.

The Fan Tachometer Low Limit registers contain a value that indicates the minimum allowable speed the fan is allowed to spin before an interrupt is generated. Fans spinning at a rate less than the minimum limit are considered slow or stalled.

If the FANTACH Reading registers are configured for legacy mode (clocks/rotation) than an interrupt will be generated when the tachometer reading is greater than the programmed minimum tachometer limit. If the FANTACH Reading registers are configured for TPC Mode (tach pulses/update time) than an interrupt will be generated when the tachometer reading is less than the programmed minimum tachometer limit. See [Registers A9h - ACh: Fan Tachometer Reading on page 266](#).

The fan tachometer will cause a bit to be set in the interrupt status register even if the current value in the associated Current PWM Duty registers is 00h. Therefore, software should disable interrupts before turning the associated PWM to the OFF state if the PWM is being used to control the fan.

Interrupts will never be generated for a fan:

- In legacy mode, if its tachometer minimum is set to FFFFh.
- In TPC mode, if its tachometer minimum is set to 0000h.

27.2.62 Registers B1h - B2h: Reserved

27.2.63 Register B3h: SMSC Reserved

27.2.64 Registers B6h - B7h: TPC Tachx Option Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B6h	R/W	TPC TachA Option Register	RES	RES	tpc/clk Periods	Sampling Rate	Sampling Disable	Pulse Duration	UPDT1	UPDT0	28h
B7h	R/W	TPC TachB Option Register	RES	RES	tpc/clk Periods	Sampling Rate	Sampling Disable	Pulse Duration	UPDT1	UPDT0	28h

Bit[7]: Reserved

Bit[6]: Reserved

Bit[5]: TACH Value

This bit determines if the tach value returned is in units of tach pulses per Update Rate (TPC) or in legacy mode that returns the number of 90kHz clocks per revolution (1 revolution = 2 tach pulses).

0= Tach Reading value in Tach Pulses per Update Rate (TPC), where the sample period is determined by Bits[1:0]

1= Tach Reading value in number of 90kHz clk periods per revolution (default)

APPLICATION NOTE: Tach interrupts should be disabled prior to changing the Tach Value bit.

Bit[4]: Dynamic Sampling Rate Disable

The device has the ability to automatically adjust the sampling rate of the tach monitor based on the expected rate of the tach input signal or it may be set to always sample at the maximum sampling rate.

0=Dynamic Sampling

1=Fixed Sampling (default). Sampling rate will be set to the maximum sampling rate as determined by [Table 27.18, "Program Value for TACH Max RPM and Max Sampling Rates," on page 269](#).

Bit[3]: Sampling Disable

0=Uses Sampling Pulses to monitor tach input (This is used for fans directly controlled by PWM output where the tach signal is not valid during the off periods of the PWM pulse.) (default)

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1=Always monitors tach input. (This requires tach signal always valid. Typically used with four wire fan solutions)

Bit[2]: Sampling Pulse Duration.

This clock determines the duration of the sampling pulse.

0=1 90kHz clock

1=2 90kHz clocks (default)

Bit[1:0]: Tach Update Rate

These bits determine how often the Tach register is updated.

Table 27.17 Tach Update Rate Select

UPDT[1:0]	TACH UPDATE RATE (SEC)
00	0.5 (default)
01	1.0
10	2.0
11	Reserved

27.2.65 Registers B8h - B9h: Max RPM for TACHs A,B

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
B8h	R/W	Max RPM for TACHA	7	6	5	4	3	2	1	0	0Eh
B9h	R/W	Max RPM for TACHA	7	6	5	4	3	2	1	0	0Eh

The tach monitoring logic for TACHA and TACHB adjusts the sampling rate based on the expected frequency of the tach input. Software should program the register value that corresponds to the maximum attainable RPM value into this register. The following table shows the programmable values for each RPM value and the corresponding maximum sampling frequency. For example, if TACHA will reach a maximum RPM value of 4800 RPM when the fan is set to a 100% duty cycle, this register should be programmed to 11h.

Table 27.18 Program Value for TACH Max RPM and Max Sampling Rates

RPM MAX	PROGRAMMED REGISTER VALUE (HEX)	MAX SAMPLING FREQUENCY
5501-6000	0E (default)	401.8
5001-5500	0F	375
4501-5000	11	330.9
4001-4500	12	312.5
3501-4000	15	267.9
3000-3500	18	234.4
2501-3000	1C	200.9
2001-2500	21	170.5

Table 27.18 Program Value for TACH Max RPM and Max Sampling Rates

RPM MAX	PROGRAMMED REGISTER VALUE (HEX)	MAX SAMPLING FREQUENCY
1501-2000	2A	133.9
1001-1500	38	100.4
≤1000	54	67

Note: If the maximum RPM value is unknown this register should be programmed for the maximum RPM value of 6000RPMs (default).

27.2.66 Register BAh - BBh: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
BAh	R	SMSC Reserved	7	6	5	4	3	2	1	0	0Fh
BBh	R	SMSC Reserved	7	6	5	4	3	2	1	0	0Fh

27.2.67 Registers BCh-FEh: Reserved

27.2.68 Register FFh: SMSC Test Register

Register Address	Read/Write	Register Name	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value
98h	R	SMSC Test Register	TST7	TST6	TST5	TST4	TST3	TST2	TST1	TST0	N/A

This register is an SMSC Test register.

Chapter 28 Runtime Registers

28.1 Runtime Register Summary

The following registers are runtime registers in the SCH5017. They are located at the address programmed in the Base I/O Address in Logical Device A (also referred to as the Runtime Register) at the offset shown. These registers are powered by VTR.

Table 28.1 Runtime Register Summary

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	VBAT POR	REGISTER
00	R/WC	-	-	0x00	-	-	PME_S3_STS
01	R/WC	-	-	0x00	-	-	PME_S5_STS
02	R/W	-	-	0x00	-	-	PME_S3_EN
03	R/W	-	-	-	-	0x01	PME_S5_EN
04	R/WC	-	-	0x00	-	-	PMES3_STS1
05	R/WC	-	-	0x00	-	-	PMES3_STS3
06	R/WC	-	-	0x00	-	-	PMES3_STS5 (Note 28.1)
07	R/WC	-	-	Note 28.2	-	-	PMES3_STS6
08	R/W	-	-	0x00 ¹	-	-	PMES3_EN1
09	R/W	-	-	0x00	-	-	PMES3_EN3
0A	R/W	-	-	0x00	-	-	PMES3_EN5
0B	R/W	-	-	0x00	-	-	PMES3_EN6
0C	R/WC	-	-	0x00	-	-	PMES5_STS1
0D	R/WC	-	-	0x00	-	-	PMES5_STS3
0E	R/WC	-	-	0x00	-	-	PMES5_STS5
0F	R/WC	-	-	Note 28.2	-	-	PMES5_STS6
10	R/W	-	-	-	-	0x00	PMES5_EN1
11	R/W	-	-	-	-	0x00	PMES5_EN3
12	R/W	-	-	-	-	0x00	PMES5_EN5
13	R/W	-	-	-	-	0xF2	PMES5_EN6
14	Note 28.9	-	-	Note 28.2	-	-	SMI_STS1
15	Note 28.9	-	-	0x00	-	-	SMI_STS2
16	R/WC	-	-	0x00	-	-	SMI_STS3
17	R/WC	-	-	0x00	-	-	SMI_STS4

Table 28.1 Runtime Register Summary (continued)

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	VBAT POR	REGISTER
18	R/W	-	-	0x00	-	-	SMI_EN1
19	R/W	-	-	0x00	-	-	SMI_EN2
1A	R/W	-	-	0x00	-	-	SMI_EN3
1B	R/W	-	-	0x00	-	-	SMI_EN4
1C	R/W	-	-	0x00	-	-	MSC_STS
1D	R	-	-	-	-	-	Reserved – reads return 0
1E	R/W	0x03	0x03	0x03	-	-	Force Disk Change
1F	R	-	-	-	-	-	Floppy Data Rate Select Shadow
20	R	-	-	-	-	-	UART1 FIFO Control Shadow
21	R	-	-	-	-	-	UART2 FIFO Control Shadow
22	R	-	-	-	-	-	Reserved – reads return 0
23	R/W	-	-	0x84	-	-	GP10
24	R/W	-	-	0x04	-	-	GP11
25	R/W	-	-	0x04	-	-	GP12
26	R/W	-	-	0x04	-	-	GP13
27	R/W	-	-	0x84	-	-	GP14
28	R	-	-	-	-	-	Reserved
29	R	-	-	-	-	-	Reserved
2A	R	-	-	-	-	-	Reserved
2B	R	-	-	-	-	-	Reserved – reads return 0
2C	R/W	-	-	0x8C	-	-	GP21
2D	R/W	-	-	0x8C	-	-	GP22
2E	R	-	-	-	-	-	Reserved – reads return 0
2F	R	-	-	-	-	-	Reserved – reads return 0
30	R	-	-	-	-	-	Reserved
31	R	-	-	-	-	-	Reserved

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Table 28.1 Runtime Register Summary (continued)

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	VBAT POR	REGISTER
32	R/W	-	-	0x01	-	-	GP27
33	R	-	-	-	-	-	Reserved
34	R	-	-	-	-	-	Reserved
35	R/W	-	-	0x84	-	-	GP32
36	R/W	-	-	0x84	-	-	GP33
37	R	-	-	-	-	-	Reserved
38	R	-	-	-	-	-	Reserved
39	R/W	-	-	0x01	-	-	GP36
3A	R/W	-	-	0x01	-	-	GP37
3B	R/W	-	-	0x01	-	-	GP40
3C	R	-	-	-	-	-	Reserved – reads return 0
3D	R/W	-	-	0x01	-	-	GP42
3E	R	-	-	0x84	-	-	GP43
3F	R/W	-	-	0x01	-	-	GP50
40	R/W	-	-	0x01	-	-	GP51
41	R/W	-	-	0x01	-	-	GP52
42	R/W	-	-	0x01	-	-	GP53
43	R/W	-	-	0x01	-	-	GP54
44	R/W	-	-	0x01	-	-	GP55
45	R/W	-	-	0x01	-	-	GP56
46	R/W	-	-	0x01	-	-	GP57
47	R/W	-	-	0x01	-	-	GP60
48	R/W	-	-	0x01	-	-	GP61
49	Note 28.4	0xxxx000b Note 28.5	-	0xxxx000b Note 28.5	-	x0000000b Note 28.5	PWR_REC
4A	R	-	-	-	-	0x00	SLP_S3_Shift
4B	R/W	-	-	0x1F	-	-	GP1
4C	R/W	-	-	0x00	-	-	GP2
4D	R/W	-	-	0x00	-	-	GP3
4E	R/W	-	-	0x00	-	-	GP4
4F	R/W	-	-	0x00	-	-	GP5
50	R/W	-	-	0x00	-	-	GP6

Table 28.1 Runtime Register Summary (continued)

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	VBAT POR	REGISTER
51	R	-	-	-	-	-	Reserved – reads return 0
52	R/W Note 28.3	-	-	Note 28.2	-	Note 28.2	INTRD
53	R/W	-	-	-	-	0x00	SLP_S3_Pre_ State
54	R	-	-	-	-	-	Reserved – reads return 0
55	R	-	-	-	-	-	Reserved – reads return 0
56	R	-	-	-	-	-	Reserved – reads return 0
57	R	-	-	-	-	-	Reserved – reads return 0
58	R	-	-	-	-	-	Reserved – reads return 0
59	R	-	-	-	-	-	Reserved – reads return 0
5A	R	-	-	-	-	-	TEST
5B	Note 28.10	-	-	-	-	0x0C	DBLCLICK
5C	Note 28.10	Note 28.2	Note 28.2	Note 28.2	-	-	Mouse_Specifi c_Wake
5D	R/W	-	-	0x00	-	-	LED1
5E	R/W	-	-	0x00	-	-	LED2
5F	Note 28.6	-	-	-	-	0xE0	Keyboard Scan Code – Make Byte 1
60	Note 28.6	-	-	-	-	0x37	Keyboard Scan Code – Make Byte 2
61	Note 28.6	-	-	-	-	0xE0	Keyboard Scan Code – Break Byte 1
62	Note 28.6	-	-	-	-	0xF0	Keyboard Scan Code – Break Byte 2
63	Note 28.6	-	-	-	-	0x37	Keyboard Scan Code – Break Byte 3
64	Note 28.6	Note 28.2	Note 28.2	Note 28.2	-	Note 28.2	Keyboard PWRBTN/SPE KEY
65	R/W	0x00	0x00	0x00	-	-	WDT_TIME_O UT

Table 28.1 Runtime Register Summary (continued)

REGISTER OFFSET (HEX)	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	VBAT POR	REGISTER
66	R/W	0x00	0x00	0x00	-	-	WDT_VAL
67	R/W	0x00	0x00	0x00	-	-	WDT_CFG
68	R/W Note 28.8	0x00 Note 28.7	0x00	0x00	-	-	WDT_CTRL
69	R/W	-	-	0x00	-	-	SPKR
6A	R/W	-	-	Note 28.2	-	Note 28.2	SMB_ISO
6B	R	-	-	-	-	-	Reserved – reads return 0
6C	R	-	-	-	-	-	Reserved – reads return 0
6D	R/W	-	-	-	-	0x00	TEST
6E-7F	R	-	-	-	-	-	Reserved – reads return 0

Note 28.1 Bit 3 of the PME_STS5 register may be set on a VCC POR. If GP53 are configured as input, then their corresponding PME and SMI status bits will be set on a VCC POR.

Note 28.2 See the register description for the default value.

Note 28.3 Bit[0] cannot be written to '1'. Bit[1] and Bit[7] are read-only.

Note 28.4 This register is a read/write register when bit[7]=0, except bit[4]. Bit[4] is a read-only bit. This register is a read-only register when bit[7]=1.

Note 28.5 This is a binary number. The x's denote a bit that is not affected by the reset condition.

Note 28.6 This register is read/write when Bit [7] Keyboard PWRBTN/SPEKEY Lock of the Keyboard PWRBTN/SPEKEY register at offset 64h is set to '0' and Read-Only when Bit [7] is set to '1'.

Note 28.7 Bit 0 is not cleared by PCI RESET.

Note 28.8 This register contains some bits that are read or write only.

Note 28.9 See the register description for the bit-wise access type.

Note 28.10 This register is read/write when Bit [7] in the [Mouse_Specific_Wake](#) Register is set to '0' and Read-Only when Bit [7] is set to '1'.

28.2 Runtime Register Description

The following registers are located at an offset from (PME_BLK) the address programmed into the base I/O address register for Logical Device A.

Table 28.2 Detailed Runtime Register Description

NAME	REG OFFSET (HEX)	DESCRIPTION
PME_S3_STS Default = 0x00 on VTR POR	00 (R/WC)	PME S3 Pin Status Register Bit[0] PME_S3_Status = 0 (default) = 1 Autonomously Set when a wakeup event occurs that normally asserts the nIO_PME_S3 signal. This bit is set independent of the state of the PME_S3_EN bit Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to PME_Status will clear it and cause the device to stop asserting nIO_PME_S3, in enabled. Writing a "0" to PME_Status has no effect.
PME_S5_STS Default = 0x00 on VTR POR	01 (R/WC)	PME S5 Pin Status Register Bit[0] PME_S5_Status = 0 (default) = 1 Autonomously Set when a wakeup event occurs that normally asserts the nIO_PME_S5 signal. This bit is set independent of the state of the PME_S5_EN bit Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to PME_Status will clear it and cause the device to stop asserting nIO_PME_S5, in enabled. Writing a "0" to PME_Status has no effect.
PME_S3_EN Default = 0x00 on VTR POR	02 (R/W)	PME S3 Pin Enable Register Bit[0] PME_S3_En = 0 nIO_PME_S3 signal assertion is disabled (default) = 1 Enables this device to assert nIO_PME_S3 signal Bit[7:1] Reserved PME_S3_En is not affected by Vcc POR, SOFT RESET or PCI RESET
PME_S5_EN Default = 0x01 on Vbat POR	03 (R/W)	PME S5 Pin Enable Register Bit[0] PME_S5_En = 0 nIO_PME_S5 signal assertion is disabled (default) = 1 Enables this device to assert nIO_PME_S5 signal Bit[7:1] Reserved PME_S5_En is not affected by VTR POR, Vcc POR, SOFT RESET or PCI RESET
PMES3_STS1 Default = 0x00 on VTR POR	04 (R/WC)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_S3_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S3 pin. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] Reserved Bit[6] IRINT. This bit is set by a transition on the IR pin (IRRXX) Bit[7] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
PMES3_STS3 Default = 0x00 on VTR POR	05 (R/WC)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_S3_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S3 pin. Bit[0] WDT Bit[1] GP21 Bit[2] GP22 Bit[3] DEVINT_STS (status of group SMI signal for PME) Bit[4] GP27 Bit[5] GP32 Bit[6] GP33 Bit[7] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.
PMES3_STS5 Default = 0x00 on VTR POR (Note 28.16)	06 (R/WC)	PME Wake Status Register 5 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_S3_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S3 pin. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.
PMES3_STS6 Default = 0x00, 0x01, 0x02 or 0x03 on VTR POR The default will be 0x02 if there is a INTRUSION event under VBAT power only, 0x01 if there is a LOW_BAT event under VBAT power only, 0x03 if both events occur or a VBAT POR occurs, 0x00 if neither event occurs. Bit[0] will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only.	07 (R/WC)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_S3_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S3 pin. Bit[0] LOW_BAT, Cleared by a write of '1'. When the battery is removed and replaced or the if the battery voltage drops below 1.2V under battery power, then the LOW_BAT PME status bit is set on VTR POR. When the battery voltage drops below 2.4 volts under VTR power (VCC=0) or under battery power only, the LOW_BAT PME status bit is set on VCC POR. The corresponding enable bit must be set to generate a PME. The low battery event is not a PME wakeup event. Bit[1] INTRUSION_STS The INTRUSION bit will default to '1' on a VTR POR if an intrusion event occurs under battery power only or if a VBAT POR occurs. Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_STS (Wake on specific mouse click) Bit[5] SPEKEY_STS (Wake on specific key) Bit[6] PB_STS Bit[7] PFR_STS Power Failure Recovery Status The PME Status register is not affected by VCC POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Status Register has no effect.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
PMES3_EN1 Default = 0x00 on VTR POR	08 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME_S3 wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_S3_EN bit is "1", the source will assert the nIO_PME_S3 signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME_S3 signal. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] Reserved Bit[6] IRINT Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PMES3_EN3 Default = 0x00 on VTR POR	09 (R/W)	PME Wake Status Register 3 This register is used to enable individual PME wake sources onto the nIO_PME_S3 wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_S3_EN bit is "1", the source will assert the nIO_PME_S3 signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME_S3 signal. Bit[0] WDT Bit[1] GP21 Bit[2] GP22 Bit[3] DEVINT_EN (Enable bit for group SMI signal for PME) Bit[4] GP27 Bit[5] GP32 Bit[6] GP33 Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PMES3_EN5 Default = 0x00 on VTR POR	0A (R/W)	PME Wake Enable Register 5 This register is used to enable individual PME wake sources onto the nIO_PME_S3 wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_S3_EN bit is "1", the source will assert the nIO_PME_S3 signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME_S3 signal. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
PMES3_EN6 Default = 0x00 on VTR POR	0B (R/W)	PME Enable Register 6 This register is used to enable individual PME sources onto the nIO_PME_S3 signal. When the PME Enable register bit for a PME source is active ("1"), if the source asserts a PME event and the PME_S3_EN bit is "1", the source will assert the nIO_PME_S3 signal. When the PME Enable register bit for a PME source is inactive ("0"), the PME Status register will indicate the state of the PME source but will not assert the nIO_PME_S3 signal. Bit[0] LOW_BAT Bit[1] INTRUSION Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_EN (Wake on specific mouse click) Bit[5] SPEKEY_EN (Wake on specific key) Bit[6] PB_EN Bit[7] PFR_EN Power Failure Recovery enable The PME Enable register 6 is not affected by VCC POR, SOFT RESET or PCI RESET.
PMES5_STS1 Default = 0x00 on VTR POR	0C (R/WC)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_S5_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S5 pin. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] Reserved Bit[6] IRINT. This bit is set by a transition on the IR pin (IRRX) Bit[7] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.
PMES5_STS3 Default = 0x00 on VTR POR	0D (R/WC)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_S5_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S5 pin. Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] Reserved Bit[4] GP27 Bit[5] GP32 Bit[6] GP33 Bit[7] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
PMES5_STS5 Default = 0x00 on VTR POR (Note 28.16)	0E (R/WC)	PME Wake Status Register 5 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_S5_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S5 pin. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.
PMES5_STS6 Default = 0x00 or 0x02 on VTR POR The default will be 0x02 if there is a INTRUSION event under VBAT power only, 0x00 if no INTRUSION event occurs.	0F (R/WC)	This register indicates the state of the individual PME sources, independent of the individual source enables or the PME_S5_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". If enabled, any set bit in this register asserts the nIO_PME_S5 pin. Bit[0] Reserved Bit[1] INTRUSION_STS The INTRUSION bit will default to '1' on a VTR POR if an intrusion event occurs under battery power only or if a VBAT POR occurs. Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_STS (Wake on specific mouse click) Bit[5] SPEKEY_STS (Wake on specific key) Bit[6] PB_STS Bit[7] PFR_STS Power Failure Recovery Status The PME Status register is not affected by VCC POR, SOFT RESET or PCI RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Status Register has no effect.
PMES5_EN1 Default = 0x00 on Vbat POR	10 (R/W)	PME Wake Enable Register 1 This register is used to enable individual PME wake sources onto the nIO_PME_S5 wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_S5_EN bit is "1", the source will assert the nIO_PME_S5 signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME_S5 signal. Bit[0] HW_Monitor Bit[1] RI2 Bit[2] RI1 Bit[3] KBD Bit[4] MOUSE Bit[5] Reserved Bit[6] IRINT Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
PMES5_EN3 Default = 0x00 on Vbat POR	11 (R/W)	PME Wake Status Register 3 This register is used to enable individual PME wake sources onto the nIO_PME_S5 wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_S5_EN bit is "1", the source will assert the nIO_PME_S5 signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME_S5 signal. Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] Reserved Bit[4] GP27 Bit[5] GP32 Bit[6] GP33 Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PMES5_EN5 Default = 0x00 on Vbat POR	12 (R/W)	PME Wake Enable Register 5 This register is used to enable individual PME wake sources onto the nIO_PME_S5 wake bus. When the PME Wake Enable register bit for a wake source is active ("1"), if the source asserts a wake event so that the associated status bit is "1" and the PME_S5_EN bit is "1", the source will assert the nIO_PME_S5 signal. When the PME Wake Enable register bit for a wake source is inactive ("0"), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME_S5 signal. Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PMES5_EN6 Default = 0xF2 on Vbat POR	13 (R/W)	PME Enable Register 6 This register is used to enable individual PME sources onto the nIO_PME_S5 signal. When the PME Enable register bit for a PME source is active ("1"), if the source asserts a PME event and the PME_S5_EN bit is "1", the source will assert the nIO_PME_S5 signal. When the PME Enable register bit for a PME source is inactive ("0"), the PME Status register will indicate the state of the PME source but will not assert the nIO_PME_S5 signal. Bit[0] Reserved Bit[1] INTRUSION Bit[2] GP60 Bit[3] GP61 Bit[4] SPEMSE_EN (Wake on specific mouse click) Bit[5] SPEKEY_EN (Wake on specific key) Bit[6] PB_EN Bit[7] PFR_EN Power Failure Recovery enable The PME Enable register 6 is not affected by VCC POR, SOFT RESET or PCI RESET.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
SMI_STS1 Default = 0x02, 0x42, 0x03 or 0x43 On VTR POR. The default will be 0x42 if there is a INTRUSION event under VBAT power only, 0x03 if there is a LOW_BAT event under VBAT power only, 0x43 if both events occur or a VBAT POR occurs, or 0x02 if neither event occurs. Bit 0 will be set to '1' on a VCC POR if the battery voltage drops below 2.4V under VTR power (VCC=0) or under battery power only. Bit 1 is set to '1' on VCC POR, VTR POR, PCI Reset and soft reset.	14 Bits[0, 6] are R/WC. Bits[1:4,7] are RO.	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source except as shown. Bit[0] LOW_BAT. Cleared by a write of '1'. When the battery is removed and replaced or if the battery voltage drops below 1.2V (nominal) under battery power only (VBAT POR), then the LOW_BAT SMI status bit is set on VTR POR. When the battery voltage drops below 2.4 volts (nominal) under VTR power (VCC=0) or under battery power only, the LOW_BAT SMI status bit is set on VCC POR. Bit[1] PINT. The parallel port interrupt defaults to '1' when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[2] U2INT Bit[3] U1INT Bit[4] FINT Bit[5] Reserved Bit[6] INTRUSION. Cleared by a write of '1'. The INTRUSION bit will default to '1' on a VTR POR if an intrusion event occurs under battery power only or if a VBAT POR occurs. (A VBAT POR occurs when the battery is removed and replaced or if the battery voltage drops below 1.2V under battery power only.) Bit[7] WDT
SMI_STS2 Default = 0x00 on VTR POR	15 (R/W) Bits[0,1] are RO Bits[2] is Read-Clear.	SMI Status Register 2 This register is used to read the status of the SMI inputs. Bit[0] MINT. Cleared at source. Bit[1] KINT. Cleared at source. Bit[2] IRINT. This bit is set by a transition on the IR pin (IRRXX). Cleared by a read of this register. Bit[3] Reserved Bit[4] SPEMSE_STS (Wake on specific mouse click) - Cleared by writing a '1' Bit[7:5] Reserved
SMI_STS3 Default = 0x00 on VTR POR	16 (R/WC)	SMI Status Register 3 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] GP54 Bit[4] GP55 Bit[5] GP56 Bit[6] GP57 Bit[7] GP60
SMI_STS4 Default = 0x00 on VTR POR (See Note 28.16)	17 (R/WC)	SMI Status Register 4 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of '1'. Bit[0] Reserved Bit[1] Reserved Bit[2] GP32 Bit[3] GP33 Bit[4] Reserved Bit[5] GP42 Bit[6] Reserved Bit[7] GP61

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Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
SMI_EN1 Default = 0x00 On VTR POR	18 (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the group nIO_SMI output. 1=Enable 0=Disable Bit[0] EN_LOW_BAT Bit[1] EN_PINT Bit[2] EN_U2INT Bit[3] EN_U1INT Bit[4] EN_FINT Bit[5] Reserved Bit[6] EN_INTRUSION Bit[7] EN_WDT
SMI_EN2 Default = 0x00 on VTR POR	19 (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the group nSMI output, and the group nSMI output onto the nIO_SMI GPI/O pin, the serial IRQ stream or into the PME Logic. Unless otherwise noted, 1=Enable 0=Disable Bit[0] EN_MINT Bit[1] EN_KINT Bit[2] EN_IRINT Bit[3] Reserved Bit[4] EN_SPEMS Bit[5] EN_SMI_PME (Enable group SMI into PME logic) Bit[6] EN_SMI_S (Enable group SMI onto serial IRQ) Bit[7] EN_SMI (Enable group SMI onto nIO_SMI pin)
SMI_EN3 Default = 0x00 on VTR POR	1A (R/W)	SMI Enable Register 3 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] GP54 Bit[4] GP55 Bit[5] GP56 Bit[6] GP57 Bit[7] GP60
SMI_EN4 Default = 0x00 on VTR POR	1B (R/W)	SMI Enable Register 4 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] Reserved Bit[1] Reserved Bit[2] GP32 Bit[3] GP33 Bit[4] Reserved Bit[5] GP42 Bit[6] Reserved Bit[7] GP61

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
MSC_STS Default = 0x00 on VTR POR	1C (R/W)	Miscellaneous Status Register Bits[5:0] can be cleared by writing a 1 to their position (writing a 0 has no effect). Bit[0] Either Edge Triggered Interrupt Input 0 Status. This bit is set when an edge occurs on the GP21 pin. Bit[1] Either Edge Triggered Interrupt Input 1 Status. This bit is set when an edge occurs on the GP22 pin. Bit[2] Reserved Bit[3] Reserved Bit[4] Either Edge Triggered Interrupt Input 4 Status. This bit is set when an edge occurs on the GP60 pin. Bit[5] Either Edge Triggered Interrupt Input 5 Status. This bit is set when an edge occurs on the GP61 pin. Bit[7:6] Reserved. This bit always returns zero.
N/A	1D (R)	Bits[7:0] Reserved – reads return 0
Force Disk Change Default = 0x03 on VCC POR, PCI Reset and VTR POR	1E (R/W)	Force Disk Change Bit[0] Force Disk Change for FDC0 0=Inactive 1=Active Bit[1] Force Disk Change for FDC1 0=Inactive 1=Active Force Change 0 and 1 can be written to 1 but are not clearable by software. Force Change 0 is cleared on nSTEP and nDS0 Force Change 1 is cleared on nSTEP and nDS1 DSKCHG (FDC DIR Register, Bit 7) = (nDS0 AND Force Change 0) OR (nDS1 AND Force Change 1) OR nDSKCHG Setting either of the Force Disk Change bits active '1' forces the FDD nDSKCHG input active when the appropriate drive has been selected. Bit[7:2] Reserved
Floppy Data Rate Select Shadow	1F (R)	Floppy Data Rate Select Shadow Bit[0] Data Rate Select 0 Bit[1] Data Rate Select 1 Bit[2] PRECOMP 0 Bit[3] PRECOMP 1 Bit[4] PRECOMP 2 Bit[5] Reserved Bit[6] Power Down Bit[7] Soft Reset
UART1 FIFO Control Shadow	20 (R)	UART FIFO Control Shadow 1 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
UART2 FIFO Control Shadow	21 (R)	UART FIFO Control Shadow 2 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
N/A	22 (R)	Bits[7:0] Reserved – reads return 0
GP10 Default = 0x84 on VTR POR	23 (R/W)	General Purpose I/O bit 1.0 Bit[0] Reserved Bit[1] Reserved Bit[2] Alternate Function Select 1= nIDE_RSTDRV 0=GPO Bits[6:3] Reserved Bit[7] Output Type Select read only returns 1= Open Drain Note: The pin can only be an Open Drain output.
GP11 Default = 0x04 on VTR POR	24 (R/W)	General Purpose I/O bit 1.1 Bit[0] Reserved Bit[1] Reserved Bit[2] Alternate Function Select 1= nPCIRST_OUT1 0= GPO Bits[6:3] Reserved Bit[7] Reserved Note: The pin can only be an push-pull output.
GP12 Default = 0x04 on VTR POR	25 (R/W)	General Purpose I/O bit 1.2 Bit[0] Reserved Bit[1] Reserved Bit[2] Alternate Function Select 1= nPCIRST_OUT2 0= GPO Bits[6:3] Reserved Bit[7] Reserved Note: The pin can only be an push-pull output.
GP13 Default = 0x04 on VTR POR	26 (R/W)	General Purpose I/O bit 1.3 Bit[0] Reserved Bit[1] Reserved Bit[2] Alternate Function Select 1= nPCIRST_OUT3 0= GPO Bits[6:3] Reserved Bit[7] Reserved Note: The pin can only be an push-pull output.
GP14 Default = 0x84 on VTR POR	27 (R/W)	General Purpose I/O bit 1.1 Bit[0] Reserved Bit[1] Reserved Bit[2] Alternate Function Select 1= nPCIRST_OUT4 0= GPO Bits[6:3] Reserved Bit[7] Output Type Select read only returns 1= Open Drain Note: The pin can only be an Open Drain output.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
N/A	28-2B (R)	Bits[7:0] Reserved – reads return 0
GP21 Default =0x8C on VTR POR	2C (R/W)	General Purpose I/O bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KDAT (Default) 10=Either Edge Triggered Interrupt Input 0 (Note 28.13) 01=Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull (Default) APPLICATION NOTE: When Bits[3:2] are programmed to '11' to select the KDAT function, bit[0] should always be programmed to '0'. The KDAT function will not operate properly when bit[0] is set.
GP22 Default =0x8C on VTR POR	2D (R/W)	General Purpose I/O bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11= KCLK (Default) 10= Either Edge Triggered Interrupt Input 1 (Note 28.13) 01= Reserved 00=Basic GPIO function Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull APPLICATION NOTE: When Bits[3:2] are programmed to '11' to select the KCLK function, bit[0] should always be programmed to '0'. The KCLK function will not operate properly when bit[0] is set.
N/A	2E-31 (R)	Bits[7:0] Reserved – reads return 0
GP27 Default = 0x01 on VTR POR	32 (R/W)	General Purpose I/O bit 2.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=8042 P17 function (Note 28.12) 01=nIO_SMI (Note 28.15) 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
GP32 Default = 0x84 on VTR POR	35 (R/W)	General Purpose I/O bit 3.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=MDAT (Default) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull APPLICATION NOTE: When Bit[2] are programmed to '1' to select the MDAT function, bit[0] should always be programmed to '0'. The MDAT function will not operate properly when bit[0] is set.
GP33 Default = 0x84 on VTR POR	36 (R/W)	General Purpose I/O bit 3.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=MCLK (Default) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull APPLICATION NOTE: When Bit[2] are programmed to '1' to select the MCLK function, bit[0] should always be programmed to '0'. The MCLK function will not operate properly when bit[0] is set.
GP36 Default = 0x01 on VTR POR	39 (R/W)	General Purpose I/O bit 3.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1= nKBDRST 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP37 Default = 0x01 on VTR POR	3A (R/W)	General Purpose I/O bit 3.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=A20M 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP40 Default =0x01 on VTR POR	3B (R/W)	General Purpose I/O bit 4.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=DRVDE0 (Note 28.14) 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
N/A	3C (R)	Bits[7:0] Reserved – reads return 0
GP42 Default =0x01 on VTR POR	3D (R/W)	General Purpose I/O bit 4.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_PME_S3 Note: configuring this pin function as output with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP43 Default =0x84 on VTR POR	3E (R/W)	General Purpose I/O bit 4.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nIO_PME_S5 (Default) Note: Configuring this pin function as output with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. 0=Basic GPIO function Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain (Default) 0=Push Pull
GP50 Default = 0x01 on VTR POR	3F (R/W)	General Purpose I/O bit 5.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nRI2 (Note 28.11) 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP51 Default = 0x01 on VTR POR	40 (R/W)	General Purpose I/O bit 5.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=nDCD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP52 Default = 0x01 on VTR POR	41 (R/W)	General Purpose I/O bit 5.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=RXD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

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Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
GP53 Default = 0x01 on VTR POR	42 (R/W)	General Purpose I/O bit 5.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Alternate Function Select 1=TXD2 0=GPIO Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP54 Default = 0x01 on VTR POR	43 (R/W)	General Purpose I/O bit 5.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=FANTACHB 01=nDSR2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP55 Default = 0x01 on VTR POR	44 (R/W)	General Purpose I/O bit 5.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=PWMB 01=nRTS2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP56 Default = 0x01 on VTR POR	45 (R/W)	General Purpose I/O bit 5.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=FANTACHA 01=nCTS2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP57 Default = 0x01 on VTR POR	46 (R/W)	General Purpose I/O bit 5.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=PWMA 01=nDTR2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
GP60 Default = 0x01 on VTR POR	47 (R/W)	General Purpose I/O bit 6.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=WDT 10=Either Edge Triggered Interrupt Input 4 (Note 28.13) 01=LED1 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP61 Default = 0x01 on VTR POR	48 (R/W)	General Purpose I/O bit 6.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[3:2] Alternate Function Select 11=Reserved 10=Either Edge Triggered Interrupt Input 5 (Note 28.13) 01=LED2 00=GPIO Bits[6:4] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
PWR_REC Power Recovery Register Default = 0xxxx000b on VTR POR Default =x0000000b on a Vbat POR Default = 0xxxx000b on a VCC POR and PCI Reset Note: x indicates that the bit is not effected by this reset condition.	49 R/W when bit[7] =0 (default), except for bit[4] Bit[4] is a Read-Only bit. Read-Only when bit[7]=1	A/C Power Control/Recovery Register Bit[0:2] Reserved Bit[3] SLP_S3# sampling enable 0=Sampling is disabled (Mode 1) 1=Sampling is enabled (Mode 2) When sampling is enabled the SLP_S3# pin is sampled every 0.5 seconds and stored in an 8-bit shift register for up to a maximum of 4 seconds. Bit[4] Previous State Bit (This read-only bit is powered by Vbat) Note: (THIS BIT IS NOT RESET ON A VTR POR) This bit contains the state of the SLP_S3# pin when VTR power is removed from the device. 0=off (SLP_S3# signal was low) 1=on (SLP_S3# signal was high) Bit[6:5] APF (After Power Failure) (These bits are powered by Vbat) Note: (THIS BIT IS NOT RESET ON A VTR POR) When VTR transitions from the OFF state to the ON state, the power recovery logic will look at the APF bits to determine if the power supply should be off or on. If the logic determines that the Power Supply should be place in the ON state it will assert the active low nIO_PME_S5 pin. The auto recovery logic does not directly control the n3V_GATE pin. The n3V_GATE pin is controlled by the nFPRST, PWRGD_PS, SLP_S3# and SLP_S5# pins. 00=Power Supply Off 01=Power Supply On 10=Power Supply set to Previous State 11=Power Supply Off Bit[7] Register Recovery R/W Control This bit is used to control write access to the Power Recovery Register at offset 49h. 0=Read/Write 1=Read-Only

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Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
SLP_S3_Shift default = 0x00 on a Vbat POR default = value latched on Power Failure on a VTR POR	4A (R)	SPL_S3# Shift Register This 8-bit register is used to read the SLP_S3# sample values loaded in the shift register in A/C Power Recovery Control - Mode 2. Bit[0] = SLP_S3# sampled 0 - 0.5sec before power failure Bit[1] = SLP_S3# sampled 0.5 - 1.0sec before power failure Bit[2] = SLP_S3# sampled 1.0 - 1.5sec before power failure Bit[3] = SLP_S3# sampled 1.5 - 2.0sec before power failure Bit[4] = SLP_S3# sampled 2.0 - 2.5sec before power failure Bit[5] = SLP_S3# sampled 2.5 - 3.0sec before power failure Bit[6] = SLP_S3# sampled 3.0 - 3.5sec before power failure Bit[7] = SLP_S3# sampled 3.5 - 4.0sec before power failure Bit definition 0=off (SLP_S3# signal was low) 1=on (SLP_S3# signal was high) Note: This register is powered by Vbat
GP1 Default = 0x1F on VTR POR	4B (R/W)	General Purpose I/O Data Register 1 Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved
GP2 Default = 0x00 on VTR POR	4C (R/W)	General Purpose I/O Data Register 2 Bit[0] Reserved Bit[1] GP21 Bit[2] GP22 Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] GP27
GP3 Default = 0x00 on VTR POR	4D (R/W)	General Purpose I/O Data Register 3 Bit[0] Reserved Bit[1] Reserved Bit[2] GP32 Bit[3] GP33 Bit[4] Reserved Bit[5] Reserved Bit[6] GP36 Bit[7] GP37
GP4 Default = 0x00 on VTR POR	4E (R/W)	General Purpose I/O Data Register 4 Bit[0] GP40 Bit[1] Reserved Bit[2] GP42 Bit[3] GP43 Bit[7:4] Reserved
GP5 Default = 0x00 on VTR POR	4F (R/W)	General Purpose I/O Data Register 5 Bit[0] GP50 Bit[1] GP51 Bit[2] GP52 Bit[3] GP53 Bit[4] GP54 Bit[5] GP55 Bit[6] GP56 Bit[7] GP57

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
GP6 Default = 0x00 on VTR POR	50 (R/W)	General Purpose I/O Data Register 6 Bit[0] GP60 Bit[1] GP61 Bit[7:2] Reserved
N/A	51 (R)	Bits[7:0] Reserved – reads return 0
INTRD Default = 0x01 (nINTRD_IN low) or 0x03 (nINTRD_IN high) On VBAT POR Default = 0x00 or 0x01 (nINTRD_IN low), or 0x02 or 0x03 (nINTRD_IN high) on VTR POR. The default will be 0x01 if an intrusion event occurred under battery power only, or if a VBAT POR occurred with nINTRD_IN low; 0x03 with nINTRD_IN high.	52 (R/W) Bit[0] Cannot Be Written to '1' Bit[1] – Read Only Bit[7] – Read Only	Intruder Detection Register Bit[0] INTRUSION; cannot be written to '1' When the INTRUDER# input goes high-to-low or low-to-high, this bit will be set. Software must write a '0' to clear this bit. Writes of '1' to this bit are ignored. Bit[1] INTRD_STS – Read Only This bit indicates the current state (inverted) of the nINTRD_IN pin. 0 = nINTRD_IN is high 1 = nINTRD_IN is low Bit[7:2] Read/Write (Note 28.17)
SLP_S3_Pre_State Default = 0x00 on Vbat POR	53 (R/W)	SLP_S3# Previous State Select Register Bits[7:3] Reserved – reads return 0 Bits[2:0] SLP_S3# Previous State Select The inverted TTL level of the SLP_S3# pin is sampled every 0.5 seconds and placed into an 8-bit shift register while VTR and VCC are on. The SLP_S3# Previous State Select bits determine which bit is used as the previous state bit following a power failure (VTR ≤ ~2.2V). 000 = SLP_S3# sampled 0 - 0.5sec before power failure 001 = SLP_S3# sampled 0.5 - 1.0sec before power failure 010 = SLP_S3# sampled 1.0 - 1.5sec before power failure 011 = SLP_S3# sampled 1.5 - 2.0sec before power failure 100 = SLP_S3# sampled 2.0 - 2.5sec before power failure 101 = SLP_S3# sampled 2.5 - 3.0sec before power failure 110 = SLP_S3# sampled 3.0 - 3.5sec before power failure 111 = SLP_S3# sampled 3.5 - 4.0sec before power failure
N/A	54 -59 (R)	Bits[7:0] Reserved – reads return 0
TEST Default = 0x00 on VBAT POR	5A (R)	Bits[0:1,5] SMSC Reserved bit. Must be written as a '0'. Bits[2:4,6:7] Reserved Read only.

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Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
DBLCLICK Default = 0x0C on VBAT POR	5B R/W when Mouse_Specific_Wake register- Bit [7] is '0' Read Only when Mouse_Specific_Wake register- Bit [7] is '1'	Double Click for Specific Wake on Mouse Select Register The DBLCLICK contains a numeric value that determines the time interval used to check for a double mouse click. DBLCLICK is the time interval between mouse clicks. For example, if DBLCLICK is set to 0.5 seconds, you have one half second to click twice for a double-click. Bit[0:5] This field contains a six bit weighted sum value from 0 to 0x3Fh which provides a double click interval between 0.0859375 and 5.5 seconds. Each incremental digit has a weight of 0.0859375 seconds.
Mouse_Specific_Wake Default = 00h on VBAT POR Default = 0xxxxxxb on VTR POR, VCC POR, and PCI Reset Note: The 'x' indicates bit is not effected by reset	5C R/W when Bit [7] is '0' Read Only when Bit [7] is '1'	Specific Wake on Mouse Click Control Register Bit[0:1] SMSC Reserved bit. Must be written as a '0'. Bits[4:2] SPESME SELECT. These bits select which mouse event is/are routed to trigger a PME S3 or PME S5 wake event. 000 = Any button click or any movement (left/right/middle) 001 = One click of left button. 010 = One click of right button. 011 = Any one click of left/right/middle button. 100 = Reserved 101 = Two times click of left button. 110 = Two times click of right button. 111 = Reserved Bit[5] Reserved. Read only zero. Bit[6] KB_MSE_SWAP. This bit swaps the Keyboard and Mouse Port interfaces. 0 = The Keyboard and Mouse Ports are not swapped. 1 = The Keyboard and Mouse Ports are swapped. Bit [7] Mouse_Specific_Wake Lock (Note) (This bit is Reset on a VBAT POR, VTR POR, VCC POR, and PCI Reset) 0 = Mouse_Specific_Wake , and DBLCLICK Registers are Read/Write. 1 = Mouse_Specific_Wake and DBLCLICK Registers are Read Only.
LED1 Default = 0x00 on VTR POR	5D (R/W)	LED1 Bit[1:0] LED1 Control 00=off 01=blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
LED2 Default = 0x00 on VTR POR	5E (R/W)	LED2 Bit[1:0] LED2 Control 00=off 01=blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
Keyboard Scan Code – Make Byte 1 (MSB) Default = 0xE0 on Vbat POR	5F (R/W)	Keyboard Scan Code This register is used to decode the first byte received from keyboards that generate multi-byte make codes and for single byte make codes. Bit[0] LSB of Scan Code Bit[7] MSB of Scan Code Note: The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). Note: Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.
Keyboard Scan Code – Make Byte 2 (LSB) Default = 0x37 on Vbat POR	60 (R/W)	Keyboard Scan Code This register is used only for multi-byte make codes. It is used to decode the second byte received. Bit[0] LSB of Scan Code Bit[7] MSB of Scan Code Note: The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). Note: Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.
Keyboard Scan Code – Break Byte 1 (MSB) Default = 0xE0 on Vbat POR	61 (R/W)	Keyboard Scan Code This register is used to decode the first byte received from keyboards that generate multi-byte make codes and for single byte break codes. Bit[0] LSB of Scan Code Bit[7] MSB of Scan Code Note: The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). Note: Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.

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Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
Keyboard Scan Code – Break Byte 2 Default = 0xF0 on Vbat POR	62 (R/W)	Keyboard Scan Code This register is used to decode the second byte received in multi-byte break codes. Bit[0] LSB of Scan Code Bit[7] MSB of Scan Code Note: The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). Note: Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.
Keyboard Scan Code – Break Byte 3 (LSB) Default = 0x37 on Vbat POR	63 (R/W)	Keyboard Scan Code This register is used to decode the third byte received in scan 2 multi-byte break codes. Bit[0] LSB of Scan Code Bit[7] MSB of Scan Code Note: The keyboard scan code registers default to the ACPI scan 2 Power make/break codes. (i.e., make=E0_37, break=E0_F0_37). Note: Programming this register to 0x00 indicates that this register a don't care. Any valid scan code that is received will be a match.
Keyboard PWRBTN/SPEKEY Default = 6Ch on Vbat POR Default = 0xxxxxxx on VTR POR, VCC POR, and PCI Reset Note: The 'x' indicates bit is not effected by reset	64 R/W when Bit [7] is '0' Read Only when Bit [7] is '1'	Bit[0] SMSC Reserved bit. Must be written as a '0'. Bit[1] SMSC Reserved bit. Must be written as a '0'. Bits[3:2] SPEKEY ScanCode. This bit is used to configure the hardware to decode a particular type of scan code. 00 = Single Byte, Scan Code Set 1 (Ex. make=37h and break=B7h) 01 =Multi-Byte, Scan Code Set 1 (Ex. make = E0h, 37h and break = E0h, B7h) 10 = Single Byte, Scan Code Set 2 (Ex. make=37h and break=F0h 37h) 11 = Multi-Byte, Scan Code Set 2 (Ex. make = E0h, 37h and break = E0h F0h 37h) (Default) Bits[5:4] Keyboard Power Button Release These bits are used to determine the pulse width of the Power Button event from the keyboard (KB_PB_STS). The wake on specific key can be configured to generate a PME event and/or power button event. If it is used to generate a power button event, the following bits will determine when the KB_PB_STS event is de-asserted. 00=De-assert KB_PB_STS 0.5sec after it is asserted (default) 01=De-assert KB_PB_STS after any valid scan code NOT EQUAL to the programmed make code. 10=De-assert KB_PB_STS when scan code received is equal to programmed break code 11=Reserved Bit[6] SMSC Reserved bit. Must be written as a '1'.

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
Keyboard PWRBTN/SPEKEY (continued)		Bit [7] Keyboard PWRBTN/SPEKEY Lock (Note) (This bit is Reset on a Vbat POR, VTR POR, VCC POR, and PCI Reset) 0 = Keyboard PWRBTN/SPEKEY and Keyboard Scan Code Registers are Read/Write 1 = Keyboard PWRBTN/SPEKEY and Keyboard Scan Code Registers are Read Only Note: The following registers become Read-Only when Bit [7] is '1': Keyboard Scan Code – Make Byte 1 at offset 5Fh Keyboard Scan Code – Make Byte 2 at offset 60h Keyboard Scan Code – Break Byte 1 at offset 61h Keyboard Scan Code – Break Byte 2 at offset 62h Keyboard Scan Code – Break Byte 3 at offset 63h Keyboard PWRBTN/SPEKEY at offset 64h
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and PCI Reset	65 (R/W)	Watch-dog Timeout Bit[0] Reserved Bit[1] Reserved Bits[6:2] Reserved, = 00000 Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and PCI Reset	66 (R/W)	Watch-dog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) 0xFF Time-out = 255 minutes (seconds)
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and PCI Reset	67 (R/W)	Watch-dog timer Configuration Bit[0] Reserved Bit[1] Keyboard Enable =1 WDT is reset upon a Keyboard interrupt. =0 WDT is not affected by Keyboard interrupts. Bit[2] Mouse Enable =1 WDT is reset upon a Mouse interrupt. =0 WDT is not affected by Mouse interrupts. Bit[3] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 0011 = IRQ3 0010 = IRQ2 (Note) 0001 = IRQ1 0000 = Disable Note: IRQ2 is used for generating SMI events via the serial IRQ's stream. The WDT should not be configured for IRQ2 if the IRQ2 slot is enabled for generating an SMI event.

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Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
WDT_CTRL Default = 0x00 on VCC POR and VTR POR Default = 0000000xb on PCI Reset Note: Bit[0] is not cleared by PCI Reset	68 (R/W) Bit[2] is Write-Only	Watch-dog timer Control Bit[0] Watch-dog Status Bit, R/W =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] P20 Force Timeout Enable, R/W = 1 Allows rising edge of P20, from the Keyboard Controller, to force the WD timeout event. A WD timeout event may still be forced by setting the Force Timeout Bit, bit 2. Note: If the P20 signal is high when the enable bit is set a WD timeout event will be generated. = 0 P20 activity does not generate the WD timeout event. Note: The P20 signal will remain high for a minimum of 1us and can remain high indefinitely. Therefore, when P20 forced timeouts are enabled, a self-clearing edge-detect circuit is used to generate a signal which is OR'ed with the signal generated by the Force Timeout Bit. Bit[7:4] Reserved. Set to 0
SPKR Default = 0x00 on VTR POR	69 R/W	Speaker Output Register Bit[0] EVENT_STATUS = 0 (default) Trigger Event inactive = 1 Trigger Event active. Bit[1] OUTPUT_EN = 0 (default) SPEAKER output is disabled = 1 SPEAKER output is enabled. Bit[2] SW_EVENT = 0 (default) When cleared a Software generated SPEAKER output is disabled. = 1 (default) When set a Software generated SPEAKER output is enabled. Bit[3] HWM_EN :This bit is used to enable the HW Mon interrupt to generate a speaker tone event. = 1 When this be is a '1', asserting the HW Monitor interrupt will assert Bit[0] (the Tone status bit). = 0 When this be is a '0', the HW Monitor interrupt has no effect on Bit[0] (the Tone status bit). Bit[4] INTRD_EN :This bit is used to enable Intruder detect to generate a speaker tone event. = 1 When this be is a '1', asserting the bit[0] in the INTRD register will assert Bit[0] (the Tone status bit) in this register. = 0 When this be is a '0', Intruder detection has no effect on Bit[0] (the Tone status bit). Bit[5:7] Reserved

Table 28.2 Detailed Runtime Register Description (continued)

NAME	REG OFFSET (HEX)	DESCRIPTION
SMB_ISO Default = 00000011b on Vbat POR and VTR POR Default = 0000yyxxb on VTR POR Only (see Note below) x= bits[1:0] value determined by bits[3:2]. y= bits[3:2] reset to '0' on Vbat POR and are not effected by other resets Note: Following a battery insertion the first VTR POR defaults to 03h. Subsequent VTR POR cycles are determined by bits[3:2]	6A R/W	SMBus Isolation Register Bit[0] S1_SEL = 0 SCLK1/SDAT1 isolated from SCLK/SDAT. = 1 SCLK1/SDAT1 connected to SCLK/SDAT (default first time suspend well is powered following a Vbat POR). Bit[1] S2_SEL = 0 SCLK2/SDAT2 isolated from SCLK/SDAT. = 1 SCLK2/SDAT2 connected to SCLK/SDAT (default first time suspend well is powered following a Vbat POR). Bit[2] S1_DEF(default): This bit determines the operation of SCLK1/SDAT1 at VTR POR and the VTR POR value of bit 0. = 0 S1_SEL (Bit 0) is set to 1 on VTR POR (VBAT POR default). = 1 S1_SEL (Bit 0) is reset to 0 on VTR POR. Bit[3] S2_DEF(default): This bit determines the operation of SCLK2/SDAT2 at VTR POR and the VTR POR value of bit 1. = 0 S2_SEL (Bit 1) is set to 1 on VTR POR (VBAT POR default). = 1 S2_SEL (Bit 1) is reset to 0 on VTR POR. Bits[5:4] Reserved Bit[6] PWRGD_DELAY_LOCK 0 = no lock operation (Default) 1 = When set to one, Bit[2] and Bit[3] of this register become RO. They remain RO until a VTR POR. Bit[7] PWRGD_DELAY_SEL 0= select PWRGD_3V delay 1= select no delay for PWRGD_3V
TEST Default=0x00 on Vbat POR	6D (R/W)	Test Register. Test Registers are reserved for SMSC. Users should not write to this register, may produce undesired results.
N/A	6E-7F (R)	Bits[7:0] Reserved – reads return 0

Note: When selecting an alternate function for a GPIO pin, all bits in the GPIO register must be properly programmed, including in/out, polarity and output type.

APPLICATION NOTE:

Note 28.11 If this pin is used for Ring Indicator wakeup, either the nRI2 event can be enabled via bit 1 in the PME_EN1 register or the GP50 PME event can be enabled via bit 0 in the PME_EN5 register.

APPLICATION NOTE:

Note 28.12 In order to use the P17 functions, the corresponding GPIO must be programmed for output, non-invert, and push-pull output type.

Note 28.13 If the EETI function is selected for this GPIO then both a high-to-low and a low-to-high edge will set the PME, SMI and MSC status bits.

Note 28.14 If the FDC function is selected on this pin (DRV_DEN0) then bit 6 of the FDD Mode Register (Configuration Register 0xF0 in Logical Device 0) will override bit 7 in the GPIO Control Register. Bit 7 of the FDD Mode Register will also affect the pin if the FDC function is selected.



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Note 28.15 The nIO_SMI pin is inactive when the internal group SMI signal is inactive and when the SMI enable bit (EN_SMI, bit 7 of the SMI_EN2 register) is '0'. When the output buffer type is OD, nIO_SMI pin is floating when inactive; when the output buffer type is push-pull, the nIO_SMI pin is high when inactive.

Note 28.16 Bit3 of the PME_STS5 register may be set on a VCC POR. If GP53 is configured as input, then the corresponding PME status bits will be set on a VCC POR. These bits are R/W but have no effect on circuit operation.

Note 28.17 These bits are R/W but have no effect on circuit operation.



Chapter 29 Configuration

The Configuration of the SCH5017 is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The SCH5017 is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the SCH5017 allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder

After a PCI Reset or Vcc Power On Reset the SCH5017 is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the SCH5017 into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the SCH5017 is in Configuration Mode.

The SYSOPT pin is latched on the falling edge of the PCI_RESET# or on Vcc Power On Reset to determine the configuration register's base address. The SYSOPT pin is used to select the CONFIG PORT's I/O address at power-up. Once powered up the configuration port base address can be changed through configuration registers CR26 and CR27. **The SYSOPT pin is a hardware configuration pin which is shared with the nRTS1 signal on pin 87.**

Note: An external pull-down resistor is required for the base IO address to be 0x02E for configuration.
An external pull-up resistor is required to move the base IO address for configuration to 0x04E.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

PORT NAME	SYSOPT= 0 10K PULL-DOWN RESISTOR	SYSOPT= 1 10K PULL-UP RESISTOR	TYPE
CONFIG PORT	0x02E	0x04E	Write
INDEX PORT (Note 29.1)	0x02E	0x04E	Read/Write
DATA PORT	INDEX PORT + 1		Read/Write

Note 29.1 The configuration port base address can be relocated through CR26 and CR27.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode
2. Configure the Configuration Registers
3. Exit Configuration Mode.

Enter Configuration Mode

To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. The config key consists of 0x55 written to the CONFIG PORT. Once the configuration key is received correctly the chip enters into the Configuration State (The auto Config ports are enabled).

Configuration Mode

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In configuration mode, the INDEX PORT is located at the CONFIG PORT address and the DATA PORT is at INDEX PORT address + 1.

The desired configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note: If accessing the Global Configuration Registers, step (a) is not required.

Exit Configuration Mode

To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note: Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

Programming Example

The following is an example of a configuration program in Intel 8086 assembly language.

```

;-----
; ENTER CONFIGURATION MODE |
;-----\
MOV DX,02EH
MOV AX,055H
OUT DX,AL
;-----
; CONFIGURE REGISTER CRE0, |
; LOGICAL DEVICE 8         |
;-----\
MOV DX,02EH
MOV AL,07H
OUT DX,AL;Point to LD# Config Reg
MOV DX,02FH
MOV AL, 08H
OUT DX,AL;Point to Logical Device 8
;
MOV DX,02EH
MOV AL,E0H
OUT DX,AL; Point to CRE0
MOV DX,02fH
MOV AL,02H
OUT DX,AL; Update CRE0
;-----

```

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```

; EXIT CONFIGURATION MODE
;-----\
MOV DX, 02EH
MOV AX, 0AAH
OUT DX, AL

```

Notes:

- SOFT RESET: Bit 0 of Configuration Control register set to one.
- All host accesses are blocked for 500µs after Vcc POR (See [Power-Up Timing on page 330.](#))

Table 29.1 Configuration Register Summary

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x78	0x78	0x78	0x78	Device ID - hard wired
0x21	R	Current Revision				Device Rev - hard wired
0x22	R/W	0x00	0x00	0x00	0x00	Power Control
0x23	R/W (Note 29.4)	0x00	0x00	0x00	-	Reserved
0x24	R/W	0x44	0x44	0x44	-	OSC
0x26	R/W	Sysopt=0: 0x2E Sysopt=1: 0x4E	Sysopt=0: 0x2E Sysopt=1: 0x4E	-	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	Sysopt=0: 0x00 Sysopt=1: 0x00	Sysopt=0: 0x00 Sysopt=1: 0x00	-	-	Configuration Port Address Byte 1 (High Byte)
0x28	R	-	-	-	-	Reserved
0x2A	R/W	-	0x00	0x00	-	TEST 6
0x2B	R/W	-	0x00	0x00	-	TEST 4
0x2C	R/W	-	0x00	0x00	-	TEST 5
0x2D	R/W	-	0x00	0x00	-	TEST 1
0x2E	R/W	-	0x00	0x00	-	TEST 2
0x2F	R/W	-	0x00	0x00	-	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x03	0x03	0x03	0x03	Primary Base I/O Address High Byte

Table 29.1 Configuration Register Summary (continued)

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
0x61	R/W	0xF0	0xF0	0xF0	0xF0	Primary Base I/O Address Low Byte
0x70	R/W	0x06	0x06	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	0x02	0x02	DMA Channel Select
0xF0	R/W	0x0E	0x0E	0x0E	-	FDD Mode Register
0xF1	R/W	0x00	0x00	0x00	-	FDD Option Register
0xF2	R/W	0xFF	0xFF	0xFF	-	FDD Type Register
0xF4	R/W	0x00	0x00	0x00	-	FDD0
0xF5	R/W	0x00	0x00	0x00	-	FDD1
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (PARALLEL PORT)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	0x04	0x04	DMA Channel Select
0xF0	R/W	0x3C	0x3C	0x3C	-	Parallel Port Mode Register
0xF1	R/W	0x00	0x00	0x00	-	Parallel Port Mode Register 2
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (SERIAL PORT 1)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (SERIAL PORT 2)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte

Table 29.1 Configuration Register Summary (continued)

INDEX	TYPE	PCI RESET	VCC POR	VTR POR	SOFT RESET	CONFIGURATION REGISTER
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 2 Mode Register
0xF1	R/W	0x02	0x02	0x02	-	IR Options Register
0xF2	R/W	0x03	0x03	0x03	-	IR Half Duplex Timeout
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (KEYBOARD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select (Keyboard)
0x72	R/W	0x00	0x00	0x00	0x00	Secondary Interrupt Select (Mouse)
0xF0	R/W	0x00	0x00	0x00	-	KRESET and GateA20 Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE A CONFIGURATION REGISTERS (RUNTIME REGISTERS)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x62	R/W	0x00	0x00	0x00	0x00	Secondary Base I/O Address High Byte
0x63	R/W	0x00	0x00	0x00	0x00	Secondary Base I/O Address Low Byte
0XF0	R/W	-	-	0X00	-	CLOCKI32
0xF1	R (Note 29.2)	-	-	-	-	Reserved
0XF2	Note 2 9.3	0x04	0x04	0x04	-	Security Key Control Register
LOGICAL DEVICE B CONFIGURATION REGISTERS (RESERVED)						

Notes: Reserved registers are read-only, reads return 0.

Note 29.2 Bits[1:0] of this register are R/W bits that have no effect on the hardware.

Note 29.3 This register is Read/Write when bit[0]=0 and Read-Only when bit[0]=1.

Note 29.4 This is a read/write register. Writing to this register may cause unwanted results.

Chip-Level (Global) Control/Configuration Registers[0x00-0x2F]

The chip-level (global) registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the ADDRESS Port for register selection. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 29.2 Chip-Level (Global) Configuration Registers

REGISTER	ADDRESS	DESCRIPTION
CHIP (GLOBAL) CONTROL REGISTERS		
	0x00 - 0x01	Reserved - Writes are ignored, reads return 0.
Config Control Default = 0x00 on VCC POR, VTR POR and PCI RESET	0x02 W	The hardware automatically clears this bit after the write, there is no need for software to clear the bits. Bit 0 = 1: Soft Reset. Refer to the Table 29.1, "Configuration Register Summary," on page 303 for the soft reset value for each register.
	0x03 - 0x06	Reserved - Writes are ignored, reads return 0.
Logical Device # Default = 0x00 on VCC POR, VTR POR, SOFT RESET and PCI RESET	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.
CHIP-LEVEL, SMSC DEFINED		
Device ID - Hard wired Default = 0x78 on VCC POR, VTR POR, SOFT RESET and PCI RESET	0x20 R	A read only register which provides device identification.
Device Rev Hard wired = Current Revision	0x21 R	A read only register which provides device revision information. Bits[7:0] = current revision when read.
PowerControl Default = 0x00 on VCC POR, VTR POR, SOFT RESET and PCI RESET	0x22 R/W	Bit[0] FDC Power Bit[1] Reserved Bit[2] Reserved Bit[3] Parallel Port Power Bit[4] Serial Port 1 Power Bit[5] Serial Port 2 Power Bit[6] Reserved Bit[7] Reserved 0: Power Off or Disabled 1: Power On or Enabled

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Table 29.2 Chip-Level (Global) Configuration Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
Reserved Default = 0x00 on VCC POR, VTR POR and PCI RESET	0x23 R/W	Reserved. This is a read/write register. Writing to this register may cause unwanted results.
OSC Default = 0x44, on VCC POR, VTR POR and PCI RESET	0x24 R/W	Bit[0] Reserved Bit [1] PLL Control = 0 PLL is on (backward Compatible) = 1 PLL is off Bits[3:2] OSC = 01 Osc is on, BRG clock is on. = 10 Same as above (01) case. = 00 Osc is on, BRG Clock Enabled. = 11 Osc is off, BRG clock is disabled. Bit [5:4] Reserved, set to zero Bit [6] 16-Bit Address Qualification = 0 12-Bit Address Qualification = 1 16-Bit Address Qualification Note: For normal operation, bit 6 should be set. Bit[7] Reserved
Chip Level Vendor Defined	0x25	Reserved - Writes are ignored, reads return 0.
Configuration Address Byte 0 Default =0x2E (Sysopt=0) =0x4E (Sysopt=1) on VCC POR and PCI RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 (Note 29.5)
Configuration Address Byte 1 Default = 0x00 on VCC POR and PCI RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] (Note 29.5)
Default = 0x00 on VCC POR, SOFT RESET and PCI RESET	0x28	Bits[7:0] Reserved - Writes are ignored, reads return 0.
Chip Level Vendor Defined	0x29	Reserved - Writes are ignored, reads return 0.
TEST 6 Default = 0x00, on VCC POR and VTR POR	0x2A R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 4 Default = 0x00, on VCC POR and VTR POR	0x2B R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.

Table 29.2 Chip-Level (Global) Configuration Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
TEST 5 Default = 0x00, on VCC POR and VTR POR	0x2C R/W	Bit[7] Test Mode: Reserved for SMSC. Users should not write to this bit, may produce undesired results. Bit[6] 8042 Reset: 1 = put the 8042 into reset 0 = take the 8042 out of reset Bits[5:0] Test Mode: Reserved for SMSC. Users should not write to this bit, may produce undesired results.
TEST 1 Default = 0x00, on VCC POR and VTR POR	0x2D R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 2 Default = 0x00, on VCC POR and VTR POR	0x2E R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.
TEST 3 Default = 0x00, on VCC POR and VTR POR	0x2F R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.

Note 29.5 To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a PCI Reset or Vcc POR.

Note: The default configuration address is either 02Eh or 04Eh, as specified by the SYSOPT pin.

Logical Device Configuration/Control Registers [0x30-0xFF]

Used to access the registers that are assigned to each logical unit. This chip supports six logical units and has eight sets of logical device registers. The eight logical devices are Floppy, Parallel, Serial 1, Serial 2, Keyboard Controller, and Runtime Registers. A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device # Register (0x07).

The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT.

The Logical Device registers are accessible only when the device is in the Configuration State. The logical register addresses are shown in [Table 29.3](#).

Table 29.3 Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION
Activate (Note 29.6) Default = 0x00 on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x30)	Bits[7:1] Reserved, set to zero. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive

Table 29.3 Logical Device Registers (continued)

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION
Logical Device Control	(0x31-0x37)	Reserved – Writes are ignored, reads return 0.
Logical Device Control	(0x38-0x3F)	Vendor Defined - Reserved - Writes are ignored, reads return 0.
Memory Base Address	(0x40-0x5F)	Reserved – Writes are ignored, reads return 0.
I/O Base Address (Note 29.7) (see Table 29.4, “Base I/O Range for Logical Devices,” on page 310) Default = 0x00 on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x60-0x6F) 0x60,2,... = addr[15:8] 0x61,3,... = addr[7:0]	Registers 0x60 and 0x61 set the base address for the device. If more than one base address is required, the second base address is set by registers 0x62 and 0x63. Refer to Table 29.4 on page 310 for the number of base address registers used by each device. Unused registers will ignore writes and return zero when read.
Interrupt Select Defaults: 0x70 = 0x00 or 0x06 (Note 29.8) on VCC POR, VTR POR, PCI RESET and SOFT RESET 0x72 = 0x00, on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x70,0x72)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the keyboard controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.
DMA Channel Select Default = 0x02 or 0x04 (Note 29.9) on VCC POR, VTR POR, PCI RESET and SOFT RESET	(0x74,0x75)	Only 0x74 is implemented for FDC and Parallel port. 0x75 is not implemented and ignores writes and returns zero when read. Refer to DMA Channel Configuration.
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.
Logical Device Configuration	(0xE0-0xFE)	Reserved – Vendor Defined (see SMSC defined Logical Device Configuration Registers).
Reserved	0xFF	Reserved

Note 29.6 A logical device will be active and powered up according to the following equation unless otherwise specified:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).

The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.

Note 29.7 If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note 29.8 The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Note 29.9 The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02 and for logical device 3 and 5 is 0x04.

Table 29.4 Base I/O Range for Logical Devices

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE E.10)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TDR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
0x01	Reserved	n/a	n/a	n/a
0x02	Reserved	n/a	n/a	n/a
0x03	Parallel Port	0x60,0x61	[0x0100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
			(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3
0x04	Serial Port 1	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x05	Serial Port 2	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x06	Reserved	n/a	n/a	n/a
0x07	KYBD	n/a	Not Relocatable Fixed Base Address: 60,64	+0 : Data Register +4 : Command/Status Reg.
0x08	Reserved	n/a	n/a	n/a
0x09	Reserved	n/a	n/a	n/a

Table 29.4 Base I/O Range for Logical Devices (continued)

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE E.10)	FIXED BASE OFFSETS
0x0A	Runtime Register Block	0x60, 0x61	[0x0000:0x0F7F] on 128-byte boundaries	+00 : PME Status . . . +5F : Keyboard Scan Code (See Table 28.1 , "Runtime Register Summary," on page 271)
	Security Key Register	0x62, 0x63	[0x0000:0x0FDF] on 32-byte boundaries	+00 : Security Key Byte 0 . . . +1F: Security Key Byte 31
0x0B	Reserved	n/a	n/a	n/a
Config. Port	Config. Port	0x26, 0x27 (Note 29.11)	0x0100:0x0FFE On 2 byte boundaries	See description Configuration Register Summary and Description. Accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.

Note 29.10 This chip uses address bits [A11:A0] to decode the base address of each of its logical devices. This device performs 16 bit address qualification, therefore address bits [A15:A12] must be '0'.

Note 29.11 The Configuration Port is at either 0x02E or 0x04E (for SYSOPT=0 or SYSOPT=1) at power up and can be relocated via CR12 and CR13.

Table 29.5 Primary Interrupt Select Register

NAME	REG INDEX	DEFINITION
Primary Interrupt Select Default=0x00 or 0x06 (Note 29.12) on VCC POR, VTR POR, PCI RESET and SOFT RESET	0x70 (R/W)	Bits[3:0] selects which interrupt is used for the primary Interrupt. 0x00= no interrupt selected 0x01= IRQ1 0x02= IRQ2/nSMI 0x03= IRQ3 0x04= IRQ4 0x05= IRQ5 0x06= IRQ6 0x07= IRQ7 0x08= IRQ8 0x09= IRQ9 0x0A= IRQ10 0x0B= IRQ11 0x0C= IRQ12 0x0D= IRQ13 0x0E= IRQ14 0x0F= IRQ15 Notes: 1. All interrupts are edge high (except ECP/EPP) 2. nSMI is active low

Notes:

- An Interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND:
 - For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
 - For the PP logical device by setting IRQE, bit D4 of the Control Port and in addition
 - For the PP logical device in ECP mode by clearing serviceIntr, bit D2 of the ecr.
 - For the Serial Port logical device by setting any combination of bits D0-D3 in the IER and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
 - For the KYBD logical device (refer to [Chapter 12, "8042 Keyboard Controller Description," on page 127](#)).
- IRQs are disabled if not used/selected by any Logical Device. Refer to [Note 29.13 on page 312](#).
- nSMI must be disabled to use IRQ2.
- All IRQ's are available in Serial IRQ mode.

Note 29.12 The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Table 29.6 DMA Channel Select

NAME	REG INDEX	DEFINITION
DMA Channel Select Default=0x02 or 0x04 (See notes) on VCC POR, VTR POR, PCI RESET and SOFT RESET	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00= Reserved 0x01= DMA1 0x02= DMA2 0x03= DMA3 0x04-0x07= No DMA active

Notes:

- A DMA channel is activated by setting the DMA Channel Select register to [0x01-0x03] AND:
- For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
- For the PP logical device in ECP mode by setting dmaEn, bit D3 of the ecr.
- The DMA channel must be disabled if not used/selected by any Logical Device. Refer to Note A.
- The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02 and for logical device 3 and 5 is 0x04. The FDC must always be assigned to DMA Channel 2.

Note 29.13 Logical Device IRQ and DMA Operation. IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel must be disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (Active bit or address not valid).

FDC: For the following cases, the IRQ and DMA channel used by the FDC are disabled.

Digital Output Register (Base+2) bit D3 (DMAEN) set to "0".

The FDC is in power down (disabled).

Serial Ports:

Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupt is disabled.

Disabling DMA Enable bit, disables DMA for UART2. Refer to the IrCC specification.

Datasheet**Parallel Port:**

SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled.

ECP Mode:

- (DMA) dmaEn from ecr register. See table.
- IRQ - See table.

MODE (FROM ECR REGISTER)		IRQ CONTROLLED BY	DMA CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

Keyboard Controller: Refer to the [8042 Keyboard Controller Description on page 127](#) of this spec

SMSC Defined Logical Device Configuration Registers

The SMSC Specific Logical Device Configuration Registers reset to their default values only on PCI resets generated by Vcc or VTR POR (as shown) or the PCI_RESET# signal. These registers are not affected by soft resets.

Table 29.7 Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0X00]

NAME	REG INDEX	DEFINITION
FDD Mode Register Default = 0x0E on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bit[0] Floppy Mode = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[1] FDC DMA Mode = 0 Burst Mode is enabled = 1 Non-Burst Mode (default) Bit[3:2] Interface Mode = 11 AT Mode (default) = 10 (Reserved) = 01 PS/2 = 00 Model 30 Bit[4] Reserved (read/write bit) Bit[5] Reserved, set to zero Bit[6] FDC Output Type Control = 0 FDC outputs are OD12 open drain (default) = 1 FDC outputs are O12 push-pull Bit[7] FDC Output Control = 0 FDC outputs active (default) = 1 FDC outputs tri-stated

Table 29.7 Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0X00 (continued)]

NAME	REG INDEX	DEFINITION
FDD Option Register Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF1 R/W	Bit[0] Forced Write Protect = 0 Inactive (default) = 1 FDD nWRTPRT input is forced active when either of the drives has been selected. nWRTPRT (to the FDC Core) = WP (FDC SRA register, bit 1) = (nDS0 AND Forced Write Protect) OR (nDS1 AND Forced Write Protect) OR nWRTPRT (from the FDD Interface) OR Floppy Write Protect Notes: ■ The Floppy Write Protect bit is in the Device Disable register. ■ Boot floppy is always drive 0. Bit[1] Reserved Bits[3:2] Density Select = 00 Normal (default) = 01 Normal (reserved for users) = 10 1 (forced to logic "1") = 11 0 (forced to logic "0") Bit[7:4] Reserved. (read/write bits)
FDD Type Register Default = 0xFF on VCC POR, VTR POR and PCI RESET	0xF2 R/W	Bits[1:0] Floppy Drive A Type Bits[3:2] Floppy Drive B Type Bits[5:4] Reserved (could be used to store Floppy Drive C type) Bits[7:6] Reserved (could be used to store Floppy Drive D type) Note: The SCH5017 supports two floppy drives
	0xF3 R	Reserved, Read as 0 (read only)
FDD0 Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF4 R/W	Bits[1:0] Drive Type Select: DT1, DT0 Bits[2] Read as 0 (read only) Bits[4:3] Data Rate Table Select: DRT1, DRT0 Bits[5] Read as 0 (read only) Bits[6] Precompensation Disable PTS =0 Use Precompensation =1 No Precompensation Bits[7] Read as 0 (read only)
FDD1	0xF5 R/W	Refer to definition and default for 0xF4

Table 29.8 Parallel Port, Logical Device 3 [Logical Device Number = 0x03]

NAME	REG INDEX	DEFINITION
PP Mode Register Default = 0x3C on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bits[2:0] Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Bit[6:3] ECP FIFO Threshold 0111b (default) Bit[7] PP Interrupt Type Not valid when the parallel port is in the Printer Mode (100) or the Standard & Bi-directional Mode (000). = 1 Pulsed Low, released to high-Z. = 0 IRQ follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP. IRQ level type when the parallel port is in ECP, TEST, or Centronics FIFO Mode.
PP Mode Register 2 Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF1 R/W	Bits[3:0] Reserved. Set to zero Bit [4] TIMEOUT_SELECT = 0 TMOU (EPP Status Reg.) cleared on write of '1' to TMOU. = 1 TMOU cleared on trailing edge of read of EPP Status Reg. Bits[7:5] Reserved. Set to zero.

Table 29.9 Serial Port, Logical Device 4 [Logical Device Number = 0x04]

NAME	REG INDEX	DEFINITION
Serial Port 1 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit[6:2] Reserved, set to zero Bit[7]: Share IRQ =0 UARTS use different IRQs =1 UARTS share a common IRQ (Note 29.14)

Note 29.14 To properly share and IRQ:

1. Configure UART1 (or UART2) to use the desired IRQ.
2. Configure UART2 (or UART1) to use No IRQ selected.
3. Set the share IRQ bit.

Note: If both UARTs are configured to use different IRQs and the share IRQ bit is set, then both of the UART IRQs will assert when either UART generates an interrupt.

Table 29.10 Serial Port 2. Logical Device 5 [Logical Device Number = 0X05]

NAME	REG INDEX	DEFINITION
Serial Port 2 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed disabled (default) = 1 High Speed enabled Bit[4:2] Reserved, set to zero Bit[5] TXD2_MODE (See Note 29.15 .) =0 TXD2 pin reflects current configuration state =1 Override current pin configuration and force TXD2 pin tristate. Bits[7:6] Reserved. Set to zero.
IR Option Register Default = 0x02 on VCC POR, VTR POR and PCI RESET	0xF1 R/W	Bit[0] Receive Polarity = 0 Active High (Default) = 1 Active Low Bit[1] Transmit Polarity = 0 Active High = 1 Active Low (Default) Bit[2] Duplex Select = 0 Full Duplex (Default) = 1 Half Duplex Bits[5:3] IR Mode = 000 Standard COM Functionality (Default) = 001 IrDA = 010 ASK-IR = 011 Reserved = 1xx Reserved Bit[6] Reserved Set to 0. Bit[7] Reserved, write 0.
IR Half Duplex Timeout Default = 0x03 on VCC POR, VTR POR and PCI RESET	0xF2	Bits [7:0] These bits set the half duplex time-out for the IR port. This value is 0 to 10msec in 100usec increments. 0= blank during transmit/receive 1= blank during transmit/receive + 100usec

Note 29.15 The TXD2_MODE bit is a VTR powered bit that is reset on VTR POR only.

Table 29.11 KYBD. Logical Device 7 [Logical Device Number = 0X07]

NAME	REG INDEX	DEFINITION
KRST_GA20 Default = 0x00 on VCC POR, VTR POR and PCI RESET Bits[6:5] reset on VTR POR only	0xF0 R/W	KRESET and GateA20 Select Bit[7] Polarity Select for P12 = 0 P12 active low (default) = 1 P12 active high Bit[6] M_ISO. Enables/disables isolation of mouse signals into 8042. Does not affect MDAT signal to mouse wakeup (PME) logic. 1= block mouse clock and data signals into 8042 0= do not block mouse clock and data signals into 8042 Bit[5] K_ISO. Enables/disables isolation of keyboard signals into 8042. Does not affect KDAT signal to keyboard wakeup (PME) logic. 1= block keyboard clock and data signals into 8042 0= do not block keyboard clock and data signals into 8042 Bit[4] MLATCH = 0 MINT is the 8042 MINT ANDed with Latched MINT (default) = 1 MINT is the latched 8042 MINT Bit[3] KLATCH = 0 KINT is the 8042 KINT ANDed with Latched KINT (default) = 1 KINT is the latched 8042 KINT Bit[2] Port 92 Select = 0 Port 92 Disabled = 1 Port 92 Enabled Bit[1] Reserved (read/write bit) Bit[0] Reserved (read/write bit)

Table 29.12 PME. Logical Device A [Logical Device Number = 0X0A]

NAME	REG INDEX	DEFINITION
CLOCKI32 Default = 0x00 on VTR POR	0xF0 (R/W)	Bit[0] (CLK32_PRSN) 0 = 32kHz clock is connected to the CLKI32 pin (default) 1 = 32kHz clock is not connected to the CLKI32 pin (pin is grounded) Bit[1] SPEKEY_EN. This bit is used to turn the logic for the “wake on specific key” feature on and off. It will disable the 32kHz clock input to the logic when turned off. The logic will draw no power when disabled. 0 = “Wake on specific key” logic is on (default) 1 = “Wake on specific key” logic is off Bit[2] Reserved (read-only bit) Reads return 0. Writes have no effect. Bit[3] SPEMSE_EN This bit is used to turn the logic for the “wake on specific mouse click” feature on and off. It will disable the 32 Khz clock input to the logic when turned off. The logic will draw no power when disabled. 0 = “wake on specific mouse click” logic is on (default) 1 = “wake on specific mouse click” logic is off Bits[7:4] are reserved

Table 29.12 PME. Logical Device A [Logical Device Number = 0X0A] (continued)

NAME	REG INDEX	DEFINITION
Security Key Control (SKC) Register Default=0x04 on a VTR POR, VCC POR, PCI Reset	0xF2 R/W when bit[0]= 0 Read-Only when bit[0]=1	Bit[0] SKC Register Lock This bit blocks write access to the Security Key Control Register. 0 = Security Key Control Register is a Read/Write register (default) 1 = Security Key Control Register is a Read-Only register Bit[1] Read-Lock This bit prevents reads from the Security Key registers located at an offset from the Secondary Base I/O address in Logical Device A 0 = Permits read operations in the Security Key block (default) 1 = Prevents read operations in the Security Key block (Reads return 00h.) Bit[2] Write-Lock This bit prevents writes to the Security Key registers located at an offset from the Secondary Base I/O address in Logical Device A 0 = Permits write operations in the Security Key block 1 = Prevents write operations in the Security Key block (default) Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved

Note: The registers located in Logical Device A are runtime registers.

Chapter 30 Valid Power Modes

The following table shows the valid power states for each power supply to the device.

Table 30.1 Valid Power States

POWER SUPPLY	POWER STATE		
	S0-S2	S3	S4-S5
Vbat	On Off (Note 30.1)	On Off (Note 30.1)	On Off (Note 30.1)
VTR	On	On	On
VCC	On	Off	Off
HVTR	On (HVTR=VTR)	On (HVTR=VTR)	On (HVTR=VTR)

Note 30.1 Although this is not considered normal operating mode, Vbat = Off is a valid power state. When Vbat is off all battery backed system context will be lost.



Chapter 31 Operational Description

31.1 Maximum Guaranteed Ratings

Operating Temperature Range0°C to +70°C

Storage Temperature Range.....-55° to +150°C

Lead Temperature Range Refer to JEDEC Spec. J-STD-020b

Note: Stresses above those listed above and below could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

31.1.1 Super I/O section (pins 3 to 105)

Maximum V_{CC} +5.0V

Negative Voltage on any pin, with respect to Ground -0.3V

31.1.2 Hardware Monitoring Block (pins 1 to 2 and pins 106 to 128)

Maximum HVTR +5.0V

Positive Voltage on any pin, with respect to Ground (Except analog inputs) HVTR+0.3V

Negative Voltage on any pin, with respect to Ground (Except analog inputs)..... -0.3V

31.2 DC Electrical Characteristics

Table 31.1 Buffer Operational Ratings

SUPER I/O BLOCK (T _A = 0 ⁰ C – 70 ⁰ C, V _{CC} = +3.3 V ± 10%)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V _{ILI}			0.8	V	TTL Levels
High Input Level	V _{IHI}	2.0		5.5	V	
IS Type Input Buffer						
Low Input Level	V _{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V _{IHIS}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V _{HYS}		100		mV	

Table 31.1 Buffer Operational Ratings (continued)

SUPER I/O BLOCK ($T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{CC} = +3.3\text{ V} \pm 10\%$)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 6\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -3\text{mA}$
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 8\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -4\text{mA}$
OD4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 4\text{mA}$
High Output Level	V_{OH}			$V_{CC}+0.3$	V	Open Drain $V_C = 3.3\text{V}$
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 8\text{mA}$
High Output Level	V_{OH}			$V_{CC}+0.3$	V	Open Drain $V_{CC}=3.3\text{V}$
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 12\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -6\text{mA}$
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 12\text{mA}$
High Output Level	V_{OH}			$V_{CC}+0.3$	V	Open Drain $V_{CC}=3.3\text{V}$
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 14\text{mA}$
High Output Level	V_{OH}			$V_{CC}+0.3$	V	Open Drain $V_{CC}=3.3\text{V}$
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 14\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -14\text{mA}$

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Table 31.1 Buffer Operational Ratings (continued)

SUPER I/O BLOCK ($T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{CC} = +3.3\text{ V} \pm 10\%$)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO8 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 8\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -4\text{mA}$
IS/O8 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	Schmitt Trigger
High Input Level	V_{IHI}	2.2		5.5	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 8\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -4\text{mA}$
IO12 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 12\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -6\text{mA}$
IOP14 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 14\text{mA}$
High Output Level	V_{OH}	2.4			V	$I_{OH} = -14\text{mA}$
IOD16 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	$I_{OL} = 16\text{mA}$
High Output Level	V_{OH}			5.5	V	Open Drain
PCI Type Buffers (PCI_ICLK, PCI_I, PCI_O, PCI_IO)	3.3V PCI 2.1 Compatible.					

Table 31.1 Buffer Operational Ratings (continued)

SUPER I/O BLOCK ($T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{CC} = +3.3\text{ V} \pm 10\%$)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Leakage Current (ALL)						(Note 31.1)
Input High Current	$I_{LEAK_{IH}}$			10	μA	$V_{IN} = V_{CC}$
Input Low Current	$I_{LEAK_{IL}}$			-10	μA	$V_{IN} = 0\text{V}$
Backdrive Protect/ChiProtect (All signal pins excluding LAD[3:0], LDRQ#, LFRAME#)						
Input High Current	$I_{LEAK_{IH}}$			10	μA	$V_{CC} = 0\text{V}$ $V_{IN} = 5.5\text{V Max}$
Input Low Current	$I_{LEAK_{IL}}$			-10	μA	$V_{IN} = 0\text{V}$
5V Tolerant Pins (All signal pins excluding LAD[3:0], LDRQ#, LFRAME#) Inputs and Outputs in High Impedance State						
Input High Current	$I_{LEAK_{IH}}$			10	μA	$V_{CC} = 0\text{V}$ $V_{IN} = 5.5\text{V Max}$
Input Low Current	$I_{LEAK_{IL}}$			-10	μA	$V_{IN} = 0\text{V}$
LPC Bus Pins (LAD[3:0], LDRQ#, LFRAME#)						
Input High Current	$I_{LEAK_{IH}}$			10	μA	$V_{CC} = 0\text{V}$ and $V_{CC} = 3.3\text{V}$ $V_{IN} = 3.6\text{V Max}$
Input Low Current	$I_{LEAK_{IL}}$			-10	μA	$V_{IN} = 0\text{V}$
V_{CC} Supply Current Active	I_{CC}			15 (Note 31.2)	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V.
Trickle Supply Voltage	V_{TR}	2.97 (Note 31.3)	3.3	3.63	V	
V_{TR} Supply Current Active	I_{TR}	0.25 (Note 31.2, Note 31.4)		10 (Note 31.2, Note 31.4)	mA	All outputs, all inputs transitioning from/to 0V to/from 3.3V.
Battery Supply Voltage	V_{BAT}	2.2	3.0	3.6	V	
V_{BAT} Average Supply Current Active V_{BAT} Monitoring Active	$I_{BAT, AVG}$			1.5	μA	All outputs open, all inputs transitioning to/from 0V from/to 3.0V). See Section 25.4, "Monitoring Vbat," on page 194.
V_{BAT} Monitoring Disabled	$I_{BAT, AVG}$			1.0		

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Table 31.1 Buffer Operational Ratings (continued)

SUPER I/O BLOCK ($T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{CC} = +3.3\text{ V} \pm 10\%$)						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
V_{BAT} Peak Supply Current Active V_{BAT} Monitoring Active	I _{BAT, Peak}			10	μA	All outputs open, all inputs transitioning to/from 0V from/to 3.0V). See Section 25.4, "Monitoring Vbat," on page 194.

HARDWARE MONITORING BLOCK ($T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $HVTR = +3.3\text{ V} \pm 10\%$)						
Parameter	Symbol	Min	Typ	Max	Units	Comments
Temperature-to-Digital Converter Characteristics						
Internal Temperature Accuracy		-3 -2	±0.25	+3 +2	°C °C	0°C ≤ T _A ≤ 70°C 40°C ≤ T _A ≤ 70°C Resolution
External Diode Sensor Accuracy		-5 -3	±0.25	+5 +3	°C °C	-40°C ≤ T _S ≤ 125°C 40°C ≤ T _S ≤ 100°C Resolution
Analog-to-Digital Converter Characteristics						
Total Unadjusted Error	TUE			±2	%	Note 31.5
Differential Non-Linearity	DNL		±1		LSB	
Power Supply Sensitivity	PSS		±1		%/V	
Total Monitoring Cycle Time (Cycle Mode, Default Averaging)	t _{C(Cycle)}		1.25	1.4	sec	Note 31.6
Conversion Time (Continuous Mode, Default Averaging)	t _{C(Cts)}	225	247	275	msec	Note 31.7
Input Resistance			140	200	kΩ	
ADC Resolution						10 bits Note 31.10
Input Buffer (I) (FANTACH1-FANTACH4)						
Low Input Level	V _{ILI}			0.8	V	
High Input Level	V _{IHI}	2.0		V _{CC} +0.3	V	

HARDWARE MONITORING BLOCK ($T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $HVTR = +3.3\text{ V} \pm 10\%$)						
Parameter	Symbol	Min	Typ	Max	Units	Comments
I_{VID} Type Buffer (VID0-VID4)						(Note 31.11)
Low Input Level	V_{ILI}			0.4	V	
High Input Level	V_{IHI}	0.8		$V_{CC}+0.3$	V	
IOD Type Buffer (SCL, SDA, PWM1, PWM2, PWM3/ADDRESS ENABLE, nHWM_INT)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		$V_{CC}+0.3$	V	
Hysteresis	V_{HYS}		500		mV	
Low Output Level	V_{OL}			0.4	V	$I_{OL} = +4.0\text{ mA}$ (Note 31.9)
Leakage Current (ALL - Digital)						(Note 31.8)
Input High Current	$I_{LEAK_{IH}}$			10	μA	$V_{IN} = V_{CC}$
Input Low Current	$I_{LEAK_{IL}}$			-10	μA	$V_{IN} = 0\text{V}$
Digital Input Capacitance	C_{IN}			10	pF	
V_{CC} Supply Current						
Active Mode	I_{CC}			3	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V.
Sleep Mode	I_{CC}			500	μA	
Shutdown Mode	I_{CC}			3	μA	

Notes:

- Voltages are measured from the local ground potential, unless otherwise specified.
- Typicals are at $T_A=25^{\circ}\text{C}$ and represent most likely parametric norm.
- The maximum allowable power dissipation at any temperature is $PD = (T_{Jmax} - T_A) / QJA$.
- Timing specifications are tested at the TTL logic levels, $V_{IL}=0.4\text{V}$ for a falling edge and $V_{IH}=2.4\text{V}$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 31.1 All leakage currents are measured with all pins in high impedance.

Note 31.2 These values are estimated. They will be updated after Characterization. Contact SMSC for the latest values.

Note 31.3 The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

Note 31.4 Max I_{TRI} with $V_{CC} = 3.3\text{V}$ (nominal) is 10mA
Max I_{TRI} with $V_{CC} = 0\text{V}$ (nominal) is 250uA

Note 31.5 TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

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Note 31.6 Total Monitoring Cycle Time for cycle mode includes a one second delay plus all temperature conversions and all analog input voltage conversions.

Note 31.7 See [Table 25.2, "Conversion Cycle Timing," on page 193](#) for conversion cycle timing for all averaging options. Only the nominal default case is shown in this section.

Note 31.8 All leakage currents are measured with all pins in high impedance.

Note 31.9 The low output level for PWM pins is actually +8.0mA.

Note 31.10 The h/w monitor analog block implements a 10-bit ADC. The output of this ADC goes to an average block, which can be configured to accumulate the averaged value of the analog inputs. The amount of averaging is programmable. The output of the averaging block produce a 12-bit temperature or voltage reading value. The 8 MSbits go to the reading register and the 4 LSbits to the A/D LSb register.

Note 31.11 Other platform components may use VID inputs and may require tighter limits.

31.3 Capacitance Values for Pins

The input and output capacitance applies to both the Super I/O Block and the Hardware Monitoring Block digital pins.

Table 31.2 Capacitance $T_A = 25$; $f_c = 1\text{MHz}$; $V_{CC} = 3.3\text{V} \pm 10\%$

LIMITS						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Note: The input capacitance of a port is measured at the connector pins.



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Chapter 32 Timing Diagrams

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

NAME	CAPACITANCE TOTAL (PF)
SER_IRQ	50
LAD [3:0]	50
LDRQ#	50
nDIR	240
nSTEP	240
nDS0	240
PD[0:7]	240
nSTROBE	240
nALF	240
KDAT	240
KCLK	240
MDAT	240
MCLK	240
LED1	50
LED2	50
TXD1	50
TXD2	50

32.1 Power Up Timing

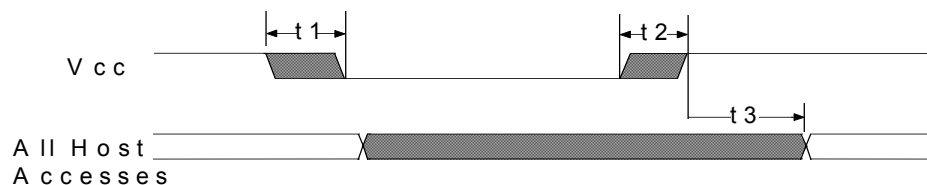


Figure 32.1 Power-Up Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 2.7V to 0V	300			μs
t2	Vcc Slew from 0V to 2.7V	100			μs
t3	All Host Accesses After Power-up (See Note 32.1)	125		500	μs

Note 32.1 Internal write-protection period after Vcc passes 2.7 volts on power-up

32.2 Input Clock Timing

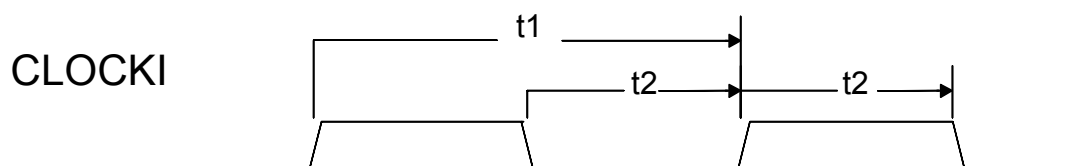


Figure 32.2 Input Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

32.3 LPC Interface Timing

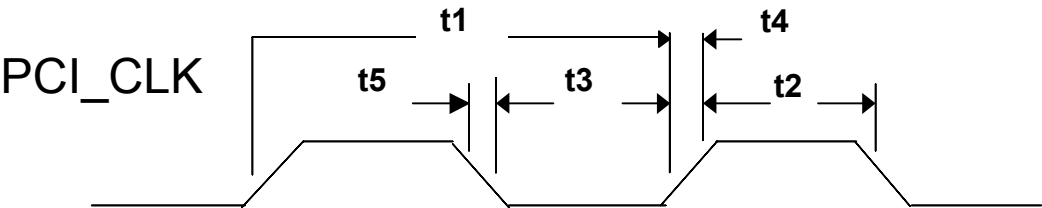


Figure 32.3 PCI Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

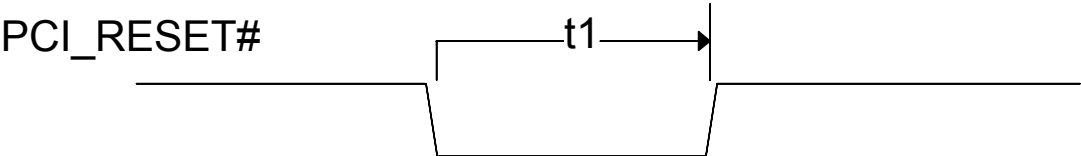
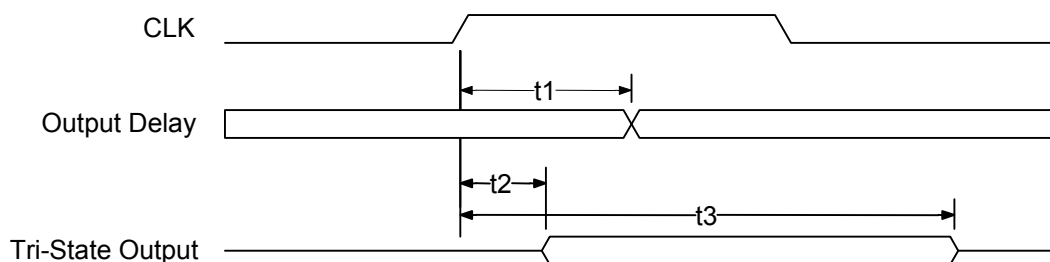
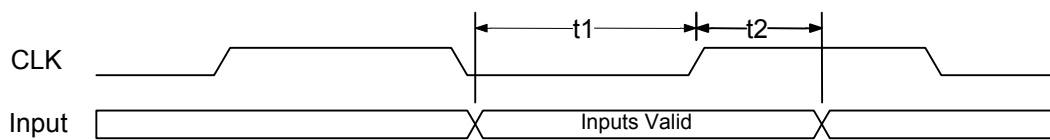


Figure 32.4 Reset Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PCI_RESET# width	1			ms

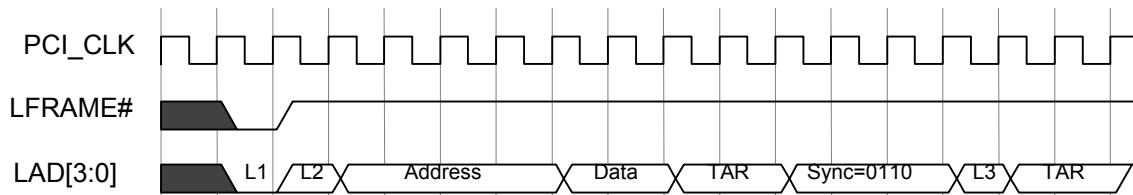
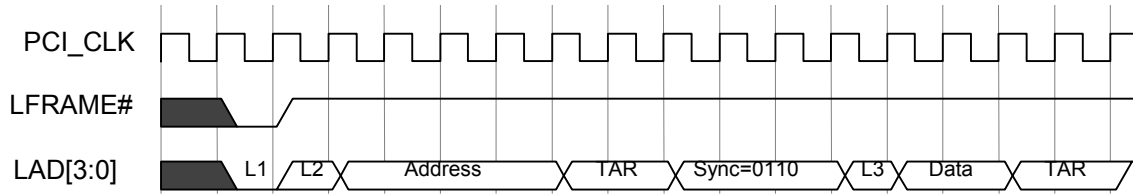

Figure 32.5 Output Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

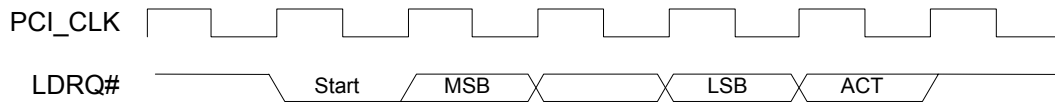
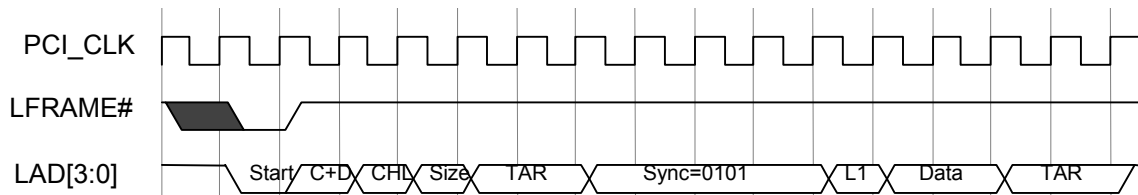

Figure 32.6 Input Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns

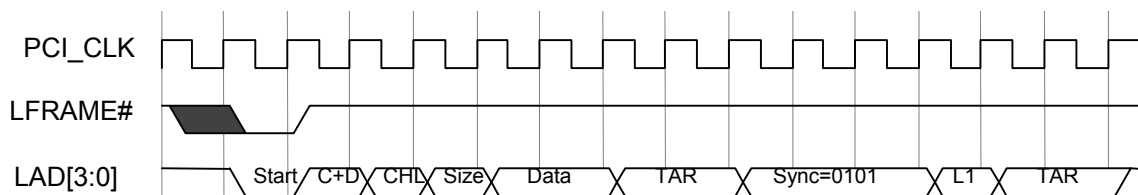
Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

**Figure 32.7 I/O Write**

Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

Figure 32.8 I/O Read**Figure 32.9 DMA Request Assertion through LDRQ#**

Note: L1=Sync of 0000

Figure 32.10 DMA Write (First Byte)

Note: L1=Sync of 0000

Figure 32.11 DMA Read (First Byte)

32.4 Floppy Disk Controller Timing

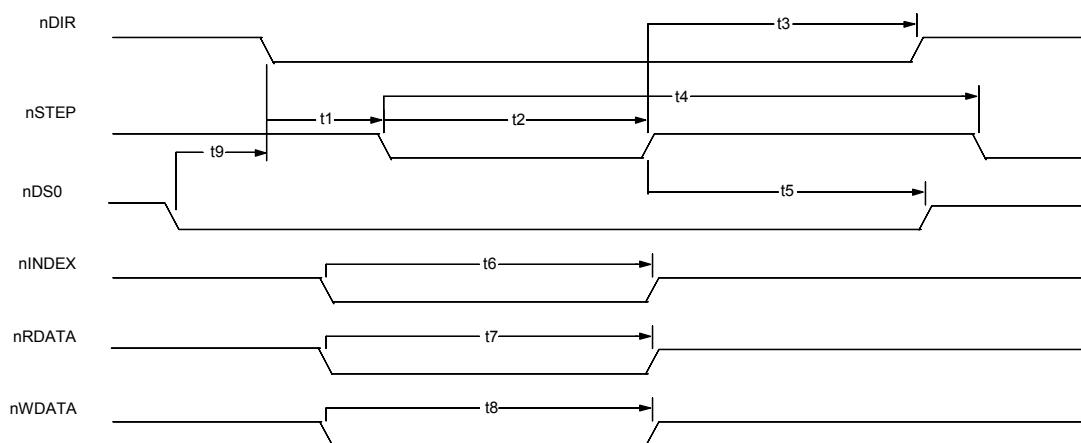


Figure 32.12 Floppy Disk Drive Timing (AT Mode Only)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0 Hold Time from nSTEP Low (Note 32.2)		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0 Setup Time nDIR Low (Note 32.2)	0			ns

*X specifies one MCLK period and Y specifies one WCLK period.

MCLK = 16 x Data Rate (at 500 kb/s MCLK = 8 MHz)

WCLK = 2 x Data Rate (at 500 kb/s WCLK = 1 MHz)

Note 32.2 The DS0 setup and hold times must be met by software.

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32.5 Parallel Port Timing

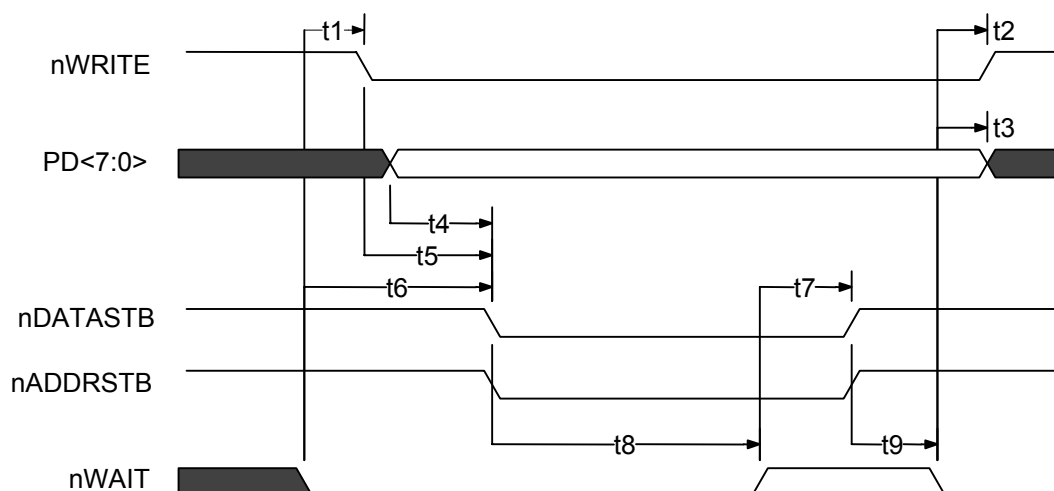
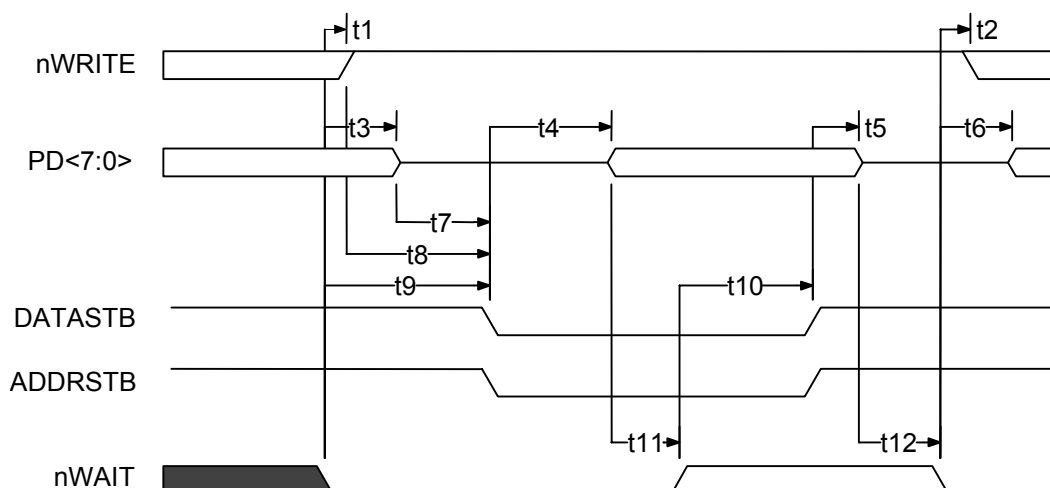


Figure 32.13 EPP 1.9 Data or Address Write Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Asserted (See Note 32.3)	60		185	ns
t2	nWAIT Asserted to nWRITE Change (See Note 32.3)	60		185	ns
t3	nWAIT Asserted to PDATA Invalid (See Note 32.3)	0			ns
t4	PDATA Valid to Command Asserted	10			ns
t5	nWRITE to Command Asserted	5		35	ns
t6	nWAIT Asserted to Command Asserted (See Note 32.3)	60		210	ns
t7	nWAIT Deasserted to Command Deasserted (See Note 32.3)	60		190	ns
t8	Command Asserted to nWAIT Deasserted	0		10	μs
t9	Command Deasserted to nWAIT Asserted	0			ns

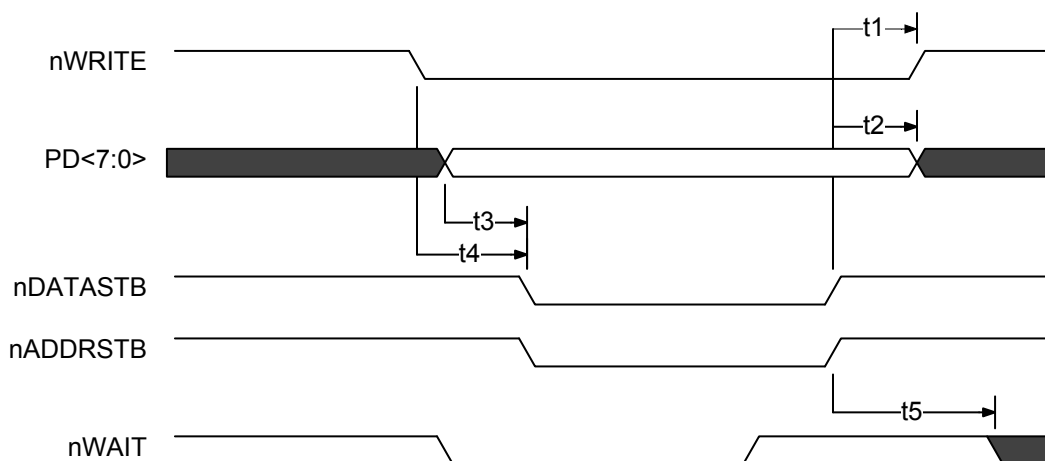
Note 32.3 nWAIT must be filtered to compensate for ringing on the parallel bus cable. nWAIT is considered to have settled after it does not transition for a minimum of 50 nsec


Figure 32.14 EPP 1.9 Data or Address Read Cycle

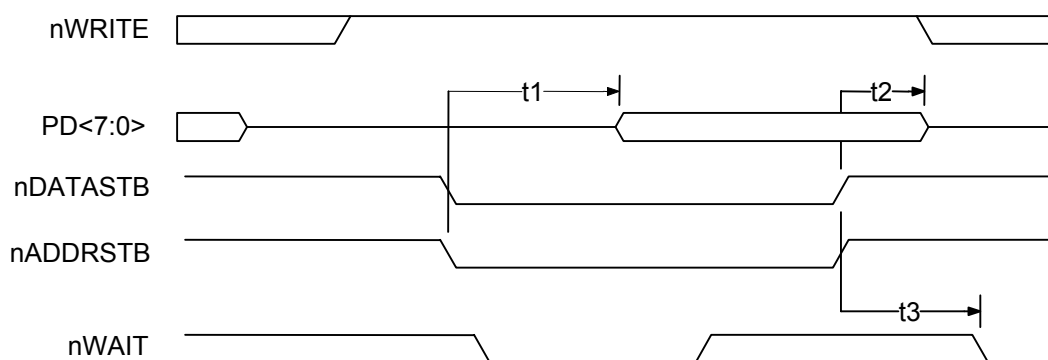
NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (Notes 1,2)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (Note 1)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			μs

Notes:

1. nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
2. When not executing a write cycle, EPP nWRITE is inactive high.

Datasheet**Figure 32.15 EPP 1.7 Data or Address Write Cycle**

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Deasserted to nWRITE Change	0		40	ns
t2	Command Deasserted to PDATA Invalid	50			ns
t3	PDATA Valid to Command Asserted	10		35	ns
t4	nWRITE to Command	5		35	ns
t5	Command Deasserted to nWAIT Deasserted	0			ns

**Figure 32.16 EPP 1.7 Data or Address Read Cycle**

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Asserted to PDATA Valid	0			ns
t2	Command Deasserted to PDATA Hi-Z	0			ns
t3	Command Deasserted to nWAIT Deasserted	0			ns

ECP PARALLEL PORT TIMING

Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500KBytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK and begins the next transfer based on Busy. Refer to [Figure 32.17 on page 339](#).

ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in [Figure 32.18 on page 340](#).

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has been accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready to accept a byte it sets HostAck (nALF) high to acknowledge the handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data, it sets HostAck (nALF) low, completing the transfer. This sequence is shown in [Figure 32.19 on page 341](#).

Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used in ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-drain), the drivers are dynamically changed from open-drain to push-pull. The timing for the dynamic driver change is specified in the *IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14*, July 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

Datasheet

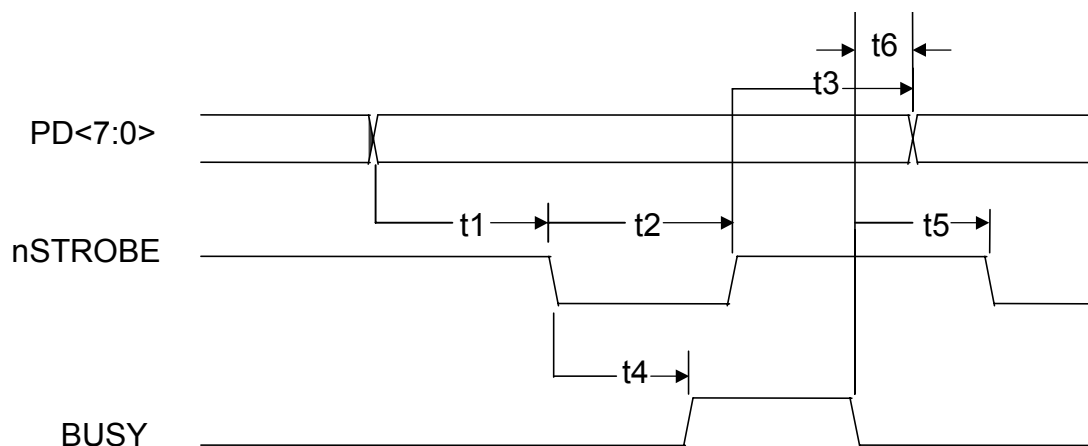
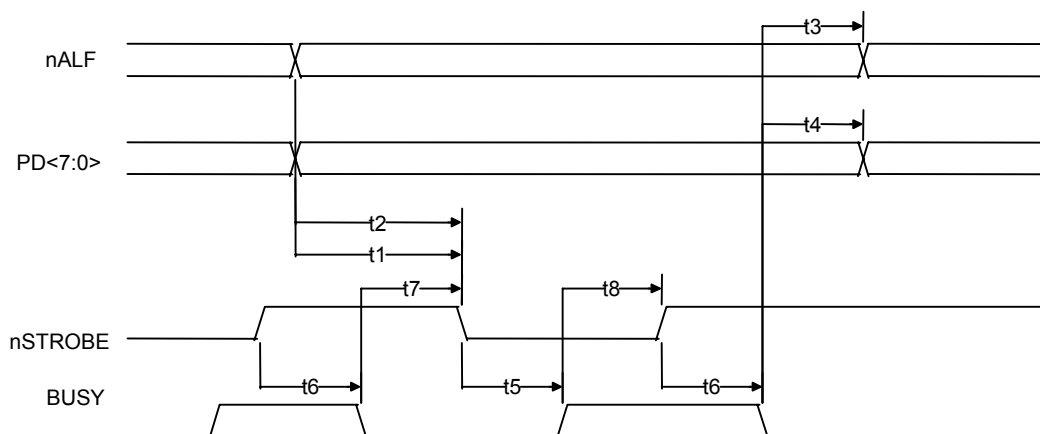


Figure 32.17 Parallel Port FIFO Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (See Note 32.4)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (See Note 32.4)	80			ns

Note 32.4 The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.


Figure 32.18 ECP Parallel Port Forward Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nALF Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nALF Changed (Notes 1,2)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (Notes 1,2)	80		180	ns
t5	nSTROBE Asserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (Notes 1,2)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (Note 2)	80		180	ns

Notes:

- Maximum value only applies if there is data in the FIFO waiting to be written out.
- BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

Datasheet

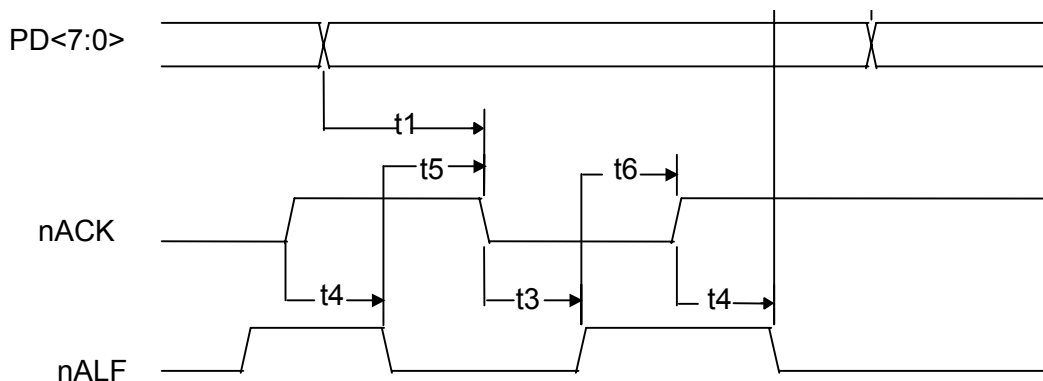
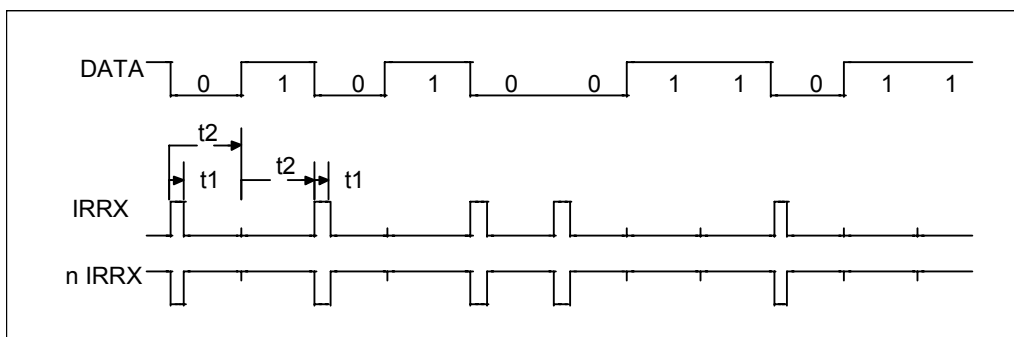


Figure 32.19 ECP Parallel Port Reverse Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nALF Deasserted to PDATA Changed	0			ns
t3	nACK Asserted to nALF Deasserted (Notes 1,2)	80		200	ns
t4	nACK Deasserted to nALF Asserted (Note 2)	80		200	ns
t5	nALF Asserted to nACK Asserted	0			ns
t6	nALF Deasserted to nACK Deasserted	0			ns
Notes: 1. Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nALF low. 2. nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.					

32.6 IR Timing

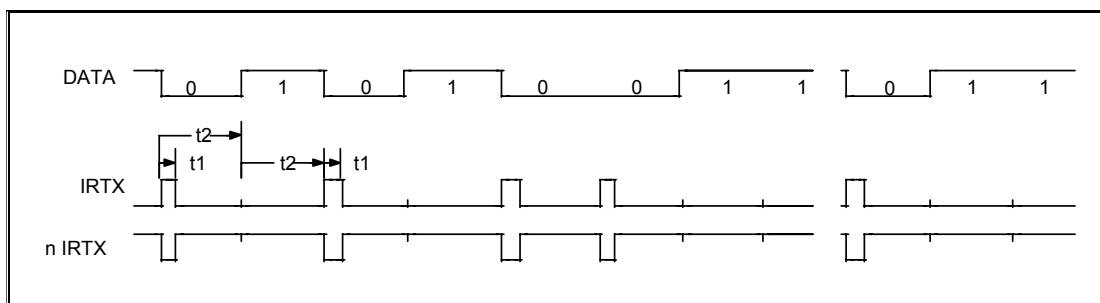


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	μs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	μs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	μs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	μs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	μs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	μs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	μs
t2	Bit Time at 115kbaud		8.68		μs
t2	Bit Time at 57.6kbaud		17.4		μs
t2	Bit Time at 38.4kbaud		26		μs
t2	Bit Time at 19.2kbaud		52		μs
t2	Bit Time at 9.6kbaud		104		μs
t2	Bit Time at 4.8kbaud		208		μs
t2	Bit Time at 2.4kbaud		416		μs

Notes:

1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41μs.
2. IRRX: L5, CRF1 Bit 0 = 1
nIRRX: L5, CRF1 Bit 0 = 0 (default)

Figure 32.20 IrDA Receive Timing

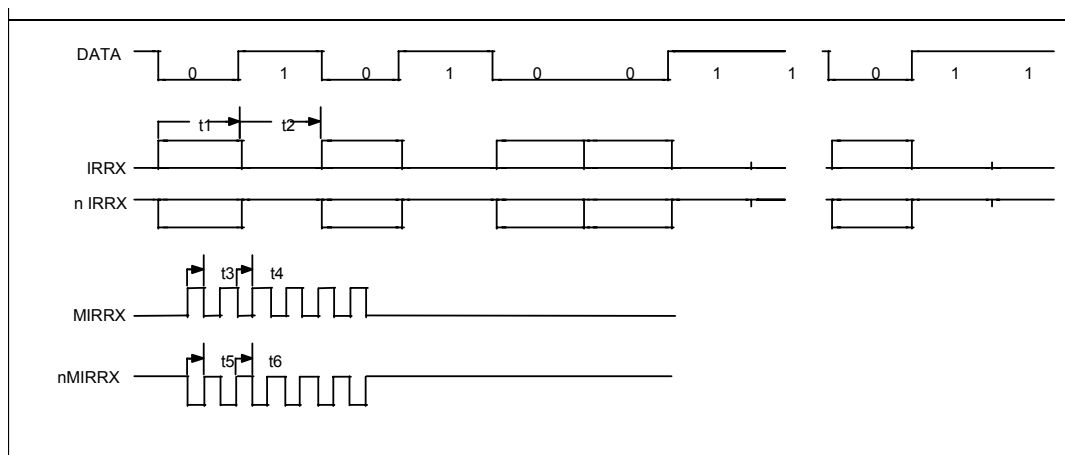
Datasheet

	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	μs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	μs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	μs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	μs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	μs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	μs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	μs
t2	Bit Time at 115kbaud		8.68		μs
t2	Bit Time at 57.6kbaud		17.4		μs
t2	Bit Time at 38.4kbaud		26		μs
t2	Bit Time at 19.2kbaud		52		μs
t2	Bit Time at 9.6kbaud		104		μs
t2	Bit Time at 4.8kbaud		208		μs
t2	Bit Time at 2.4kbaud		416		μs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
n IRTX: L5, CRF1 Bit 1 = 0

Figure 32.21 IrDA Transmit Timing

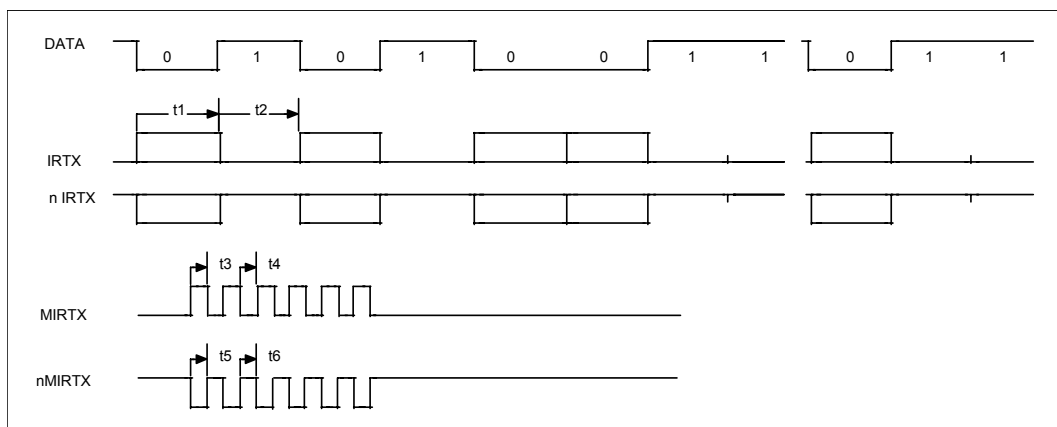


	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				μs
t2	Off Bit Time				μs
t3	Modulated Output "On"	0.8	1	1.2	μs
t4	Modulated Output "Off"	0.8	1	1.2	μs
t5	Modulated Output "On"	0.8	1	1.2	μs
t6	Modulated Output "Off"	0.8	1	1.2	μs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
nIRRX: L5, CRF1 Bit 0 = 0 (default)
MIRRX, nMIRRX are the modulated outputs

Figure 32.22 Amplitude Shift-Keyed IR Receive Timing

Datasheet

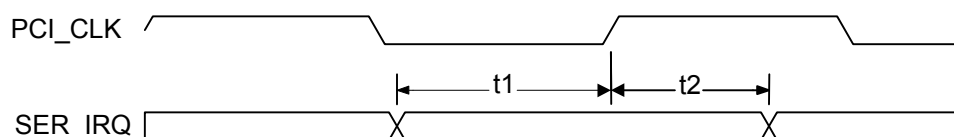
	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				μ s
t2	Off Bit Time				μ s
t3	Modulated Output "On"	0.8	1	1.2	μ s
t4	Modulated Output "Off"	0.8	1	1.2	μ s
t5	Modulated Output "On"	0.8	1	1.2	μ s
t6	Modulated Output "Off"	0.8	1	1.2	μ s

Notes:

1. IRTX: L5, CRF1 Bit 1 = 1 (default)

n IRTX: L5, CRF1 Bit 1 = 0

MIRTX, nMIRTX are the modulated outputs

Figure 32.23 Amplitude Shift-Keyed IR Transmit Timing**32.7 Serial IRQ Timing****Figure 32.24 Setup and Hold Time**

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

32.8 UART Interface Timing

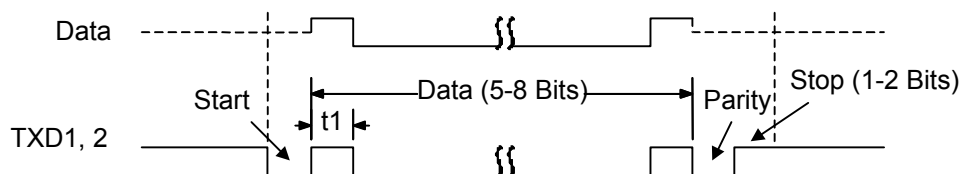


Figure 32.25 Serial Port Data

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR}^1		nsec

t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the "Baud Rate" table in the "Serial Port" section.

32.9 Keyboard/Mouse Interface Timing

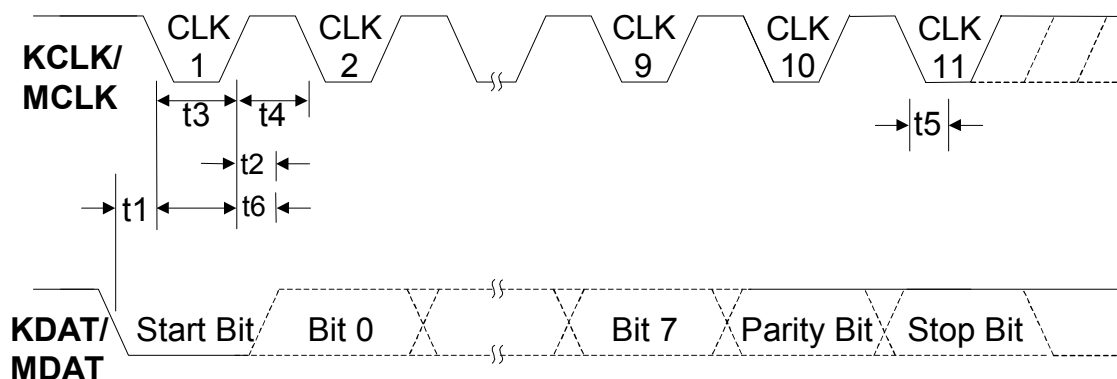


Figure 32.26 Keyboard/Mouse Receive/Send Data Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Time from DATA transition to falling edge of CLOCK (Receive)	5		25	μsec
t2	Time from rising edge of CLOCK to DATA transition (Receive)	5		T4-5	μsec
t3	Duration of CLOCK inactive (Receive/Send)	30		50	μsec
t4	Duration of CLOCK active (Receive/Send)	30		50	μsec
t5	Time to keyboard inhibit after clock 11 to ensure the keyboard does not start another transmission (Receive)	>0		50	μsec
t6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	μsec

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32.10 Resume Reset Signal Generation

nRSMRST signal is the reset output for the ICH resume well. This signal is used as a power on reset signal for the ICH.

SCH5017 detects when VTR voltage raises above **VTRIP**, provides a delay before generating the rising edge of nRSMRST. See definition of **VTRIP** on page 347.

This delay, tRESET_DELAY, (**t1** on page 347) is nominally 32ms, starts when VTR voltage rises above the **VTRIP** trip point. If the VTR voltage falls below **VTRIP** the during tRESET_DELAY then the following glitch protection behavior is implemented: When the VTR voltage rises above **VTRIP**, nRSMRST will remain asserted the full tRESET_DELAY after which nRSMRST is deasserted.

On the falling edge there is minimal delay, tRESET_FALL.

Timing and voltage parameters are shown in Figure 32.27 and Table 32.1.

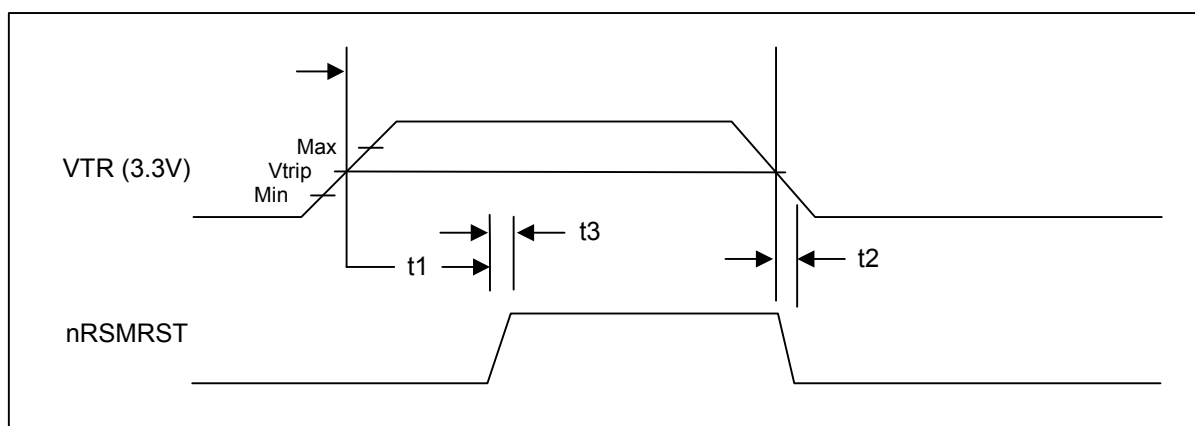


Figure 32.27 Resume Reset Sequence

Table 32.1 Resume Reset Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
t1	tRESET_DELAY: VTR active to nRSMRST inactive	10	32	100	msec	
t2	tRESET_FALL: VTR inactive to nRSMRST active (Glitch width allowance)			100	nsec	
t3	tRESET_RISE			100	nsec	
VTRIP	VTR low trip voltage	tbd	~2.2	tbd	V	

APPLICATION NOTE: The 5 Volt Standby power supply must power up before or simultaneous with VTR, and must power down simultaneous with or after VTR (from ICH2 data sheet.) SCH5017 does not have a 5 Volt Standby power supply input and does not respond to incorrect 5 Volt Standby power - VTR sequencing.

32.11 nLEDx Timing

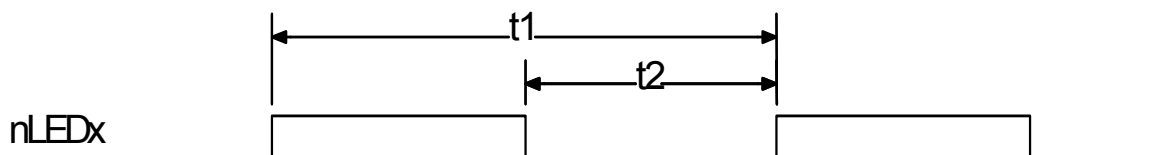


Figure 32.28 nLEDx Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period		1 or 2 ²	5.88 ¹	sec
t2	Blink ON Time	0	0.5 ²	1.52 ¹	sec

1. These Max values are due to internal Ring Oscillator. If 1Hz blink rate is selected for LED1 pin, the range will vary from 0.33Hz to 1.0Hz. If 0.5Hz blink rate is selected for LED1 pin, the range will vary from 0.17Hz to 0.5Hz.
2. The blink rate is programmed through Bits[1:0] in LEDx register. When Bits[1:0]=00, LED is OFF. Bits[1:0]=01 indicates LED blink at 1Hz rate with a 50% duty cycle (0.5 sec ON, 0.5 sec OFF). Bits[1:0]=10 indicates LED blink at ½ Hz rate with a 25% duty cycle (0.5 sec ON, 1.5 sec OFF). When Bits[1:0]=11, LED is ON.

32.12 PWM Outputs

The following section shows the timing for the PWM[1:3] outputs.



Figure 32.29 PWMx Output Timing

Table 32.2 Timing for PWM[1:3] Outputs

Name	Description	Min	Typ	Max	Units
t1	PWM Period (Note 1) - low frequency option - high frequency option	11.4 10.7		90.9 42.7	msec usec
t2	PWM High Time (Note 2)	0		99.6	%

Notes:
1. This value is programmable by the PWM frequency bits located in the FRFx registers.
2. The PWM High Time is based on a percentage of the total PWM period (min=0/256*T_{PWM}, max =255/256*T_{PWM}). During Spin-up the PWM High Time can reach a 100% or Full On. (T_{PWM} = t1).

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32.13 SMBus Interface

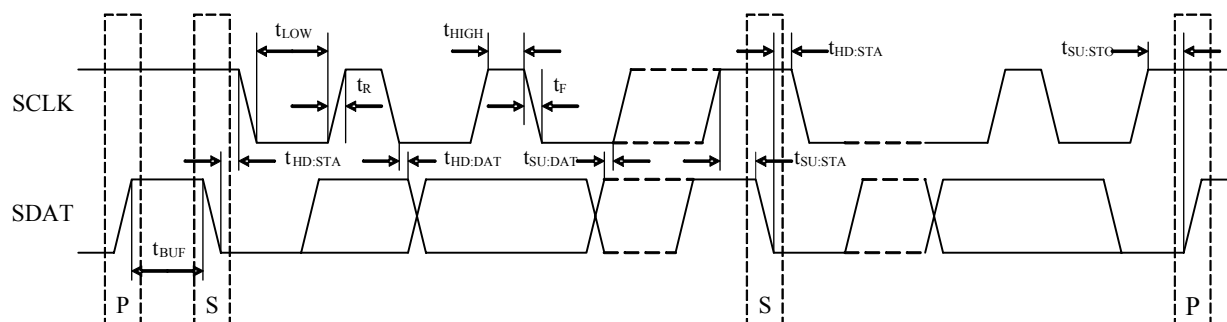


Figure 32.30 SMBus Timing

SYMBOL	PARAMETER	LIMITS		UNITS	COMMENTS
		MIN	MAX		
Fsmb	SMB Operating Frequency	10	400	kHz	Note 32.5
Tsp	Spike Suppression		50	ns	Note 32.6
Tbuf	Bus free time between Stop and Start Condition	1.3		μs	
Thd:sta	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		μs	
Tsu:sta	Repeated Start Condition setup time	0.6		μs	
Tsu:sto	Stop Condition setup time	0.6		μs	
Thd:dat	Data hold time	0.3	0.9	μs	
Tsu:dat	Data setup time	100		ns	Note 32.7
Tlow	Clock low period	1.3		μs	
Thigh	Clock high period	0.6		μs	
Tf	Clock/Data Fall Time	$20+0.1C_b$	300	ns	
Tr	Clock/Data Rise Time	$20+0.1C_b$	300	ns	
C_b	Capacitive load for each bus line		400	pF	

Note 32.5 The SMBus timing (e.g., max clock frequency of 400kHz) specified exceeds that specified in the System Management Bus Specification, Rev 1.1. This corresponds to the maximum clock frequency for fast mode devices on the I²C bus. See “The I²C Bus Specification,” version 2.0, Dec. 1998.

Note 32.6 At 400kHz, spikes of a maximum pulse width of 50ns must be suppressed by the input filter.

Note 32.7 If using 100 kHz clock frequency, the next data bit output to the SDA line will be 1250 ns (1000 ns (TR max) + 250 ns (TSU:DAT min) @ 100 kHz) before the SCLK line is released.



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Chapter 33 Package Outline

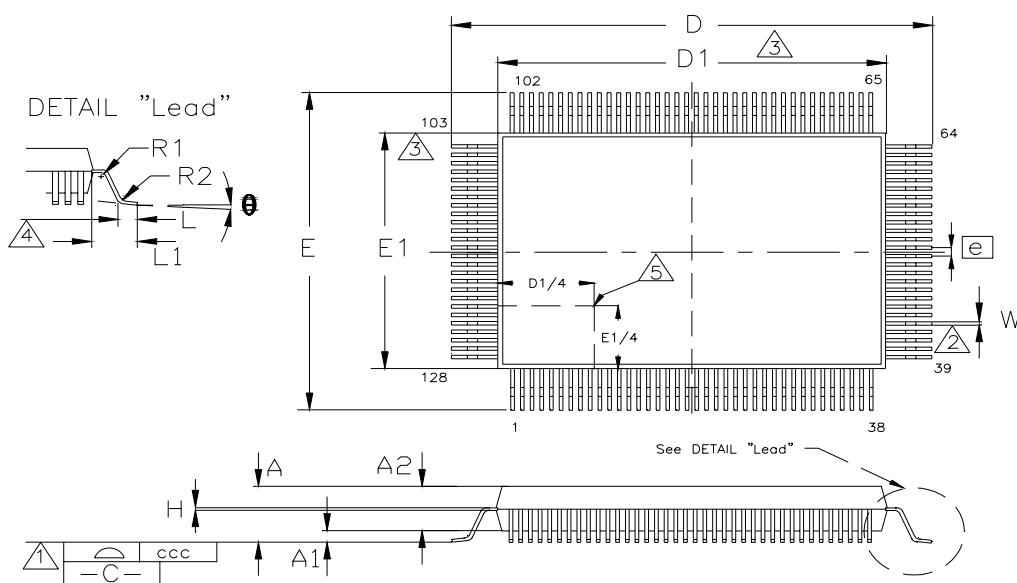


Figure 33.1 128 Pin QFP Package Outline, 14X20X2.7 Body, 3.2 mm Footprint.

Table 33.1 128 Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.00	23.20	23.40	X Span
D1	19.90	20.00	20.10	X body Size
E	17.00	17.20	17.40	Y Span
E1	13.90	14.00	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.60	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Controlling Unit: millimeter.
3. Tolerance on the position of the leads is ± 0.04 mm maximum.
4. Package body dimensions D1 and E1 do not include the mold protrusion.
5. Maximum mold protrusion is 0.25 mm.
6. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
7. Details of pin 1 identifier are optional but must be located within the zone indicated.



Appendix A ADC Voltage Conversion

Table A.1 Analog-to-Digital Voltage Conversions for Hardware Monitoring Block

INPUT VOLTAGE				A/D OUTPUT	
+12 V	+5 V Note 33.1	+3.3 V Note 33.2	V _{CCPIN}	Decimal	Binary
<0.062	<0.026	<0.0172	<0.012	0	0000 0000
0.062–0.125	0.026–0.052	0.017–0.034	0.012–0.023	1	0000 0001
0.125–0.188	0.052–0.078	0.034–0.052	0.023–0.035	2	0000 0010
0.188–0.250	0.078–0.104	0.052–0.069	0.035–0.047	3	0000 0011
0.250–0.313	0.104–0.130	0.069–0.086	0.047–0.058	4	0000 0100
0.313–0.375	0.130–0.156	0.086–0.103	0.058–0.070	5	0000 0101
0.375–0.438	0.156–0.182	0.103–0.120	0.070–0.082	6	0000 0110
0.438–0.500	0.182–0.208	0.120–0.138	0.082–0.093	7	0000 0111
0.500–0.563	0.208–0.234	0.138–0.155	0.093–0.105	8	0000 1000
⋮	⋮	⋮	⋮	⋮	⋮
4.000–4.063	1.666–1.692	1.100–1.117	0.749–0.761	64 (1/4 Scale)	0100 0000
⋮	⋮	⋮	⋮	⋮	⋮
8.000–8.063	3.330–3.560	2.200–2.217	1.499–1.511	128 (1/2 Scale)	1000 0000
⋮	⋮	⋮	⋮	⋮	⋮
12.000–12.063	5.000–5.026	3.300–3.317	2.249–2.261	192 (3/4 Scale)	1100 0000
⋮	⋮	⋮	⋮	⋮	⋮
15.312–15.375	6.380–6.406	4.210–4.230	2.869–2.881	245	1111 0101
15.375–15.437	6.406–6.432	4.230–4.245	2.881–2.893	246	1111 0110
15.437–15.500	6.432–6.458	4.245–4.263	2.893–2.905	247	1111 0111
15.500–15.563	6.458–6.484	4.263–4.280	2.905–2.916	248	1111 1000
15.625–15.625	6.484–6.510	4.280–4.300	2.916–2.928	249	1111 1001
15.625–15.688	6.510–6.536	4.300–4.314	2.928–2.940	250	1111 1010
15.688–15.750	6.536–6.562	4.314–4.330	2.940–2.951	251	1111 1011
15.750–15.812	6.562–6.588	4.331–4.348	2.951–2.964	252	1111 1100
15.812–15.875	6.588–6.615	4.348–4.366	2.964–2.975	253	1111 1101
15.875–15.938	6.615–6.640	4.366–4.383	2.975–2.987	254	1111 1110
>15.938	>6.640	>4.383	>2.988	255	1111 1111

Note 33.1 The 5V input and 5VTR input are +5V nominal inputs.

Note 33.2 The VCC, VTR, and Vbat inputs are +3.3V nominal inputs. VCC and VTR are nominal 3.3V power supplies. Vbat is a nominal 3.0V power supply.

Datasheet

Appendix B Example Fan Circuits

The following figures show examples of circuitry on the board for the PWM outputs, tachometer inputs, and remote diodes. [Figure B.1](#) shows how the part can be used to control four fans by connecting two fans to one PWM output.

Note: These examples represent the minimum required components. Some designs may require additional components.

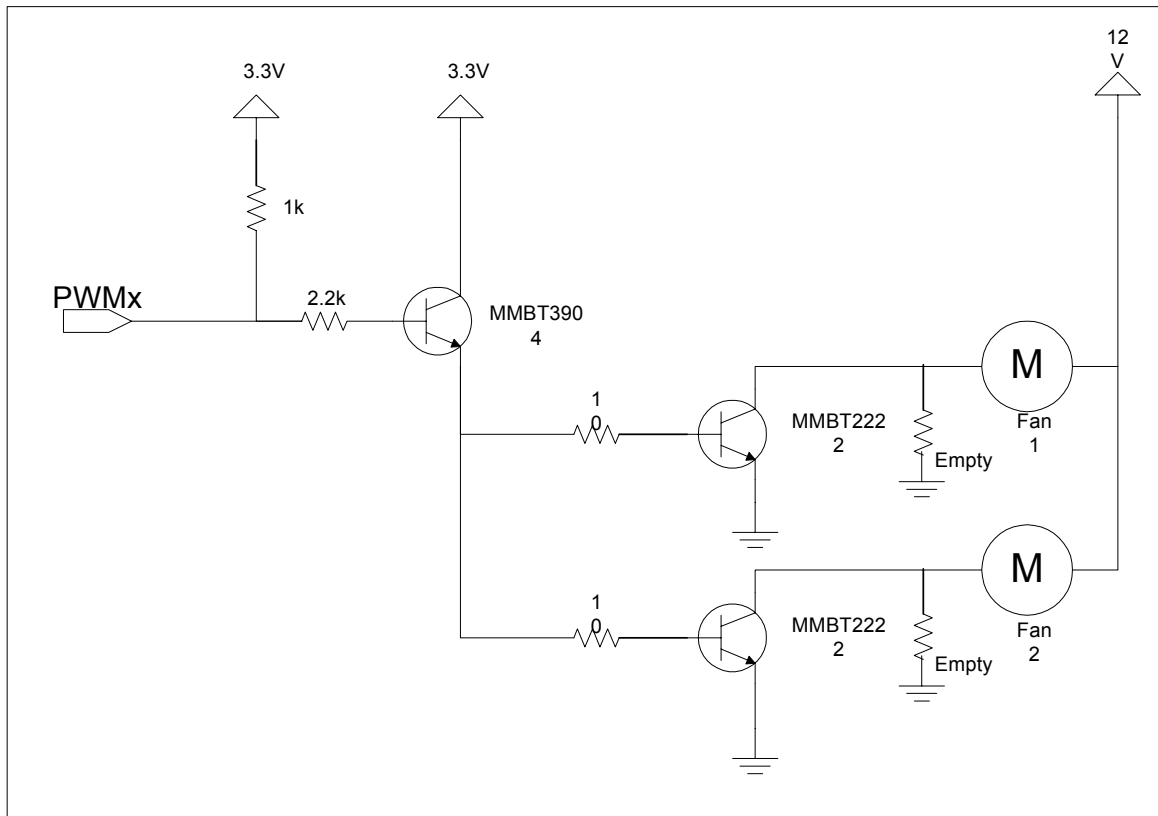


Figure B.1 Fan Drive Circuitry for Low Frequency Option (Apply to PWM Driving Two Fans)

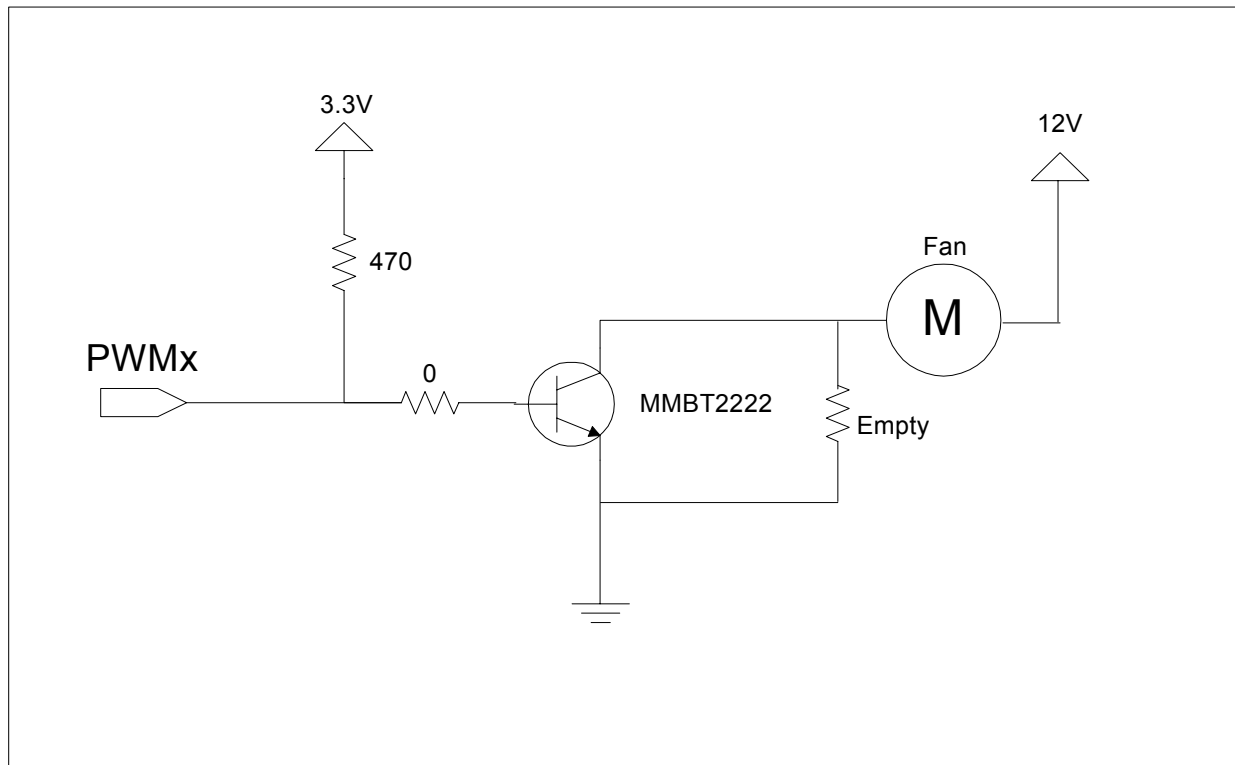


Figure B.2 Fan Drive Circuitry for Low Frequency Option (Apply to PWM Driving One Fan)

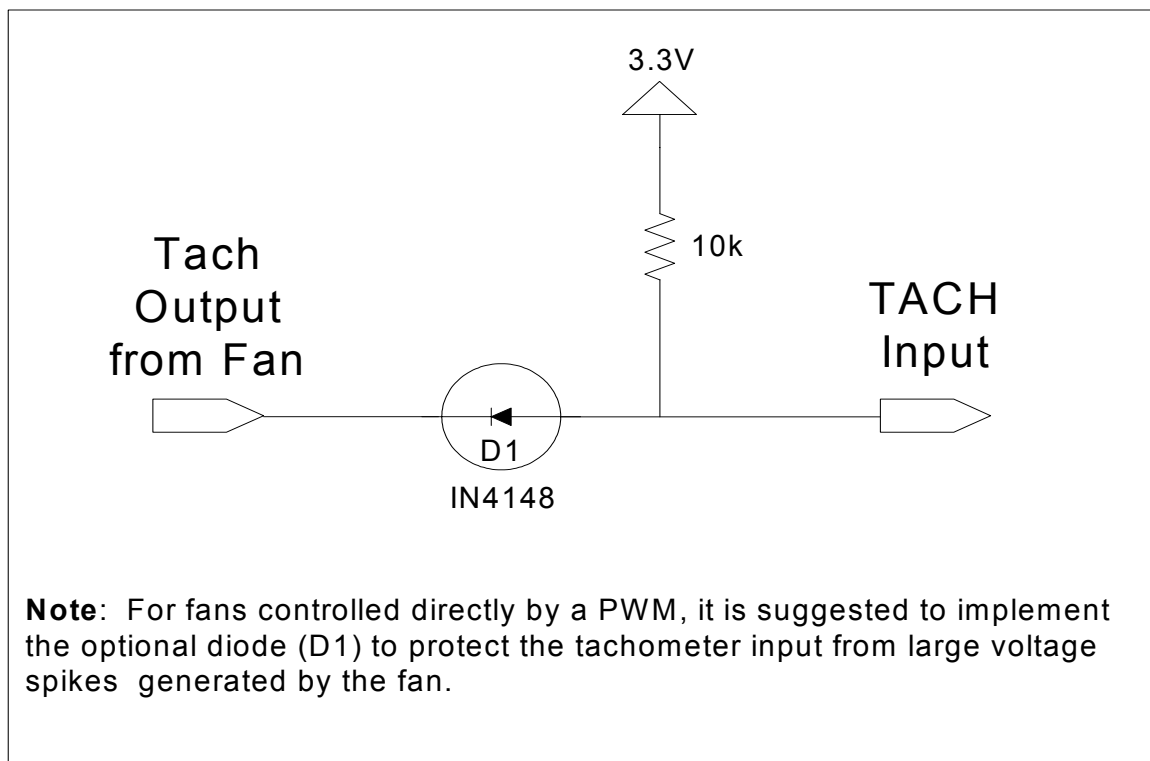
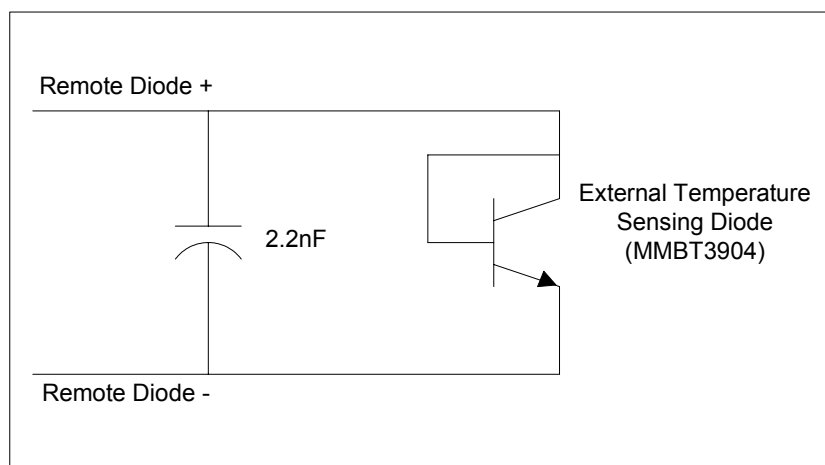
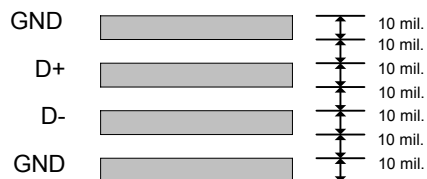


Figure B.3 Fan Tachometer Circuitry (Apply to Each Fan)

Datasheet**Figure B.4 Remote Diode (Apply to Remote2 Lines)****Notes:**

1. 2.2nF cap is optional and should be placed close to the SCH5017 if used.
2. The voltage at PWM3 must be at least 2.0V to avoid triggering Address Enable.
3. The Remote Diode + and Remote Diode - tracks should be kept close together, in parallel with grounded guard tracks on each side. Using wide tracks will help to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended. See Figure B.5, "Suggested Minimum Track Width and Spacing".

**Figure B.5 Suggested Minimum Track Width and Spacing**



Appendix C Test Mode

The SCH5017 provides board test capability through the implementation of one XNOR chain and one XOR chain. The XNOR chain is dedicated to the Super I/O portion of the chip (pins 3 – 100) and the XOR chain is dedicated solely to the Hardware Monitoring Block (pins 106 – 128).

C.1 Super I/O Block XNOR-Chain Test Mode

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See [Figure C.1](#). When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SCH5017 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

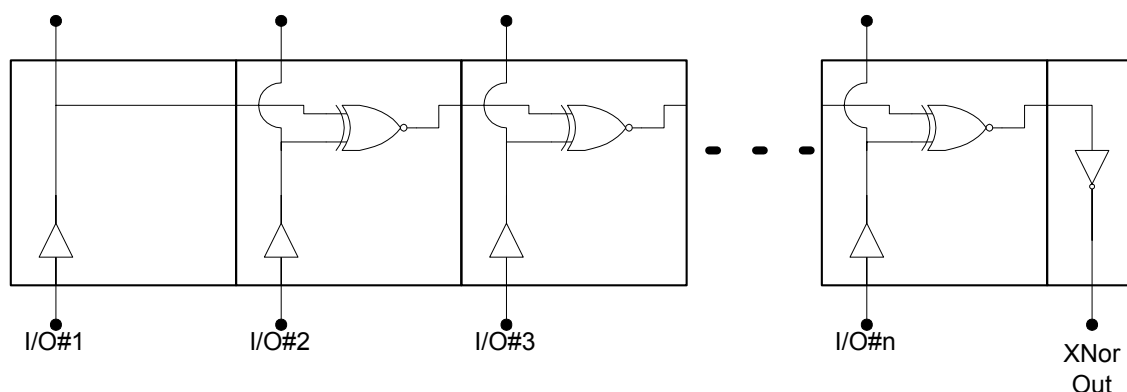


Figure C.1 XNOR-Chain Test Structure

C.1.1 Board Test Mode

Board test mode can be entered as follows:

On the rising (deasserting) edge of PCI_RESET#, drive LFRAME# low and drive LAD[0] low.

Exit board test mode as follows:

On the rising (deasserting) edge of PCI_RESET#, drive either LFRAME# or LAD[0] high.

See [Section C.2.2, "HW Monitor XOR-Chain Test Mode"](#) for a description of this board test mode.

The PCI_RESET# pin is not included in the XNOR-Chain. The XNOR-Chain output pin# is TXD1. See the following subsections for more details.

Pin List of Super I/O XNOR Chain

Pins 3 – 100 on the chip are inputs to the first XNOR chain, with the exception of the following:

- VCC (5 pins), VTR, and Vbat
- VSS (6 pins) and AVSS
- TXD1 This is the chain output.
- PCI_RESET#.

- SDA2, SCLK2, SDA1, SCLK1

To put the chip in the first XNOR chain test mode, tie LAD0 and LFRAME# low. Then toggle PCI_RESET# from a low to a high state. Once the chip is put into XNOR chain test mode, LAD0 and LFRAME# become part of the chain.

To exit the SIO XNOR chain test mode tie LAD0 or LFRAME# high. Then toggle PCI_RESET# from a low to a high state. A VCC POR will also cause the XNOR chain test mode to be exited. To verify the test mode has been exited, observe the output at TXD1. Toggling any of the input pins in the chain should not cause its state to change.

Setup of Super I/O XNOR Chain

Warning: Ensure power supply is off during setup.

- Connect the VSS, the AVSS, HVSS pins to ground.
- Connect the VCC, the VTR, and HVTR pins to 3.3V.
- Connect an oscilloscope or voltmeter to TXD1.
- All other pins should be tied to ground.

Testing

1. Turn power on.
2. With LAD0 and LFRAME# low, bring PCI_RESET# high. The chip is now in XNOR chain test mode. At this point, all inputs to the first XNOR chain are low. The output, on TXD1 should also be low. Refer to INITIAL CONFIG on [Table C.1](#).
3. Bring pin 100 high. The output on TXD1 (pin66) should go toggle. Refer to STEP ONE in [Table C.1](#).
4. In descending pin order, bring each input high. The output should switch states each time an input is toggled. Continue until all inputs are high. The output on TXD1 should now be low. Refer to END CONFIG in [Table C.1](#).
5. The current state of the chip is now represented by INITIAL CONFIG in [Table C.2](#).
6. Each input should now be brought low, starting at pin one and continuing in ascending order. Continue until all inputs are low. The output on TXD1 should now be low. Refer to [Table C.2](#).
7. To exit test mode, tie LAD0 (pin 20) OR LFRAME# high, and toggle PCI_RESET# from a low to a high state.

Table C.1 Toggling Inputs in Descending Order

	PIN 100	PIN 99	PIN 98	PIN 97	PIN 96	PIN ...	PIN 3	OUTPUT PIN 85
INITIAL CONFIG	L	L	L	L	L	L	L	H
STEP 1	H	L	L	L	L	L	L	L
STEP 2	H	H	L	L	L	L	L	H
STEP 3	H	H	H	L	L	L	L	L
STEP 4	H	H	H	H	L	L	L	H
STEP 5	H	H	H	H	H	L	L	L
...	...	...	...	...	...	...	...	...
STEP N	H	H	H	H	H	H	L	H
END CONFIG	H	H	H	H	H	H	H	L

Table C.2 Toggling Inputs in Ascending Order

	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN ...	PIN 128	OUTPUT PIN 85
INITIAL CONFIG	H	H	H	H	H	H	H	L
STEP 1	L	H	H	H	H	H	H	H
STEP 2	L	L	H	H	H	H	H	L
STEP 3	L	L	L	H	H	H	H	H
STEP 4	L	L	L	L	H	H	H	L
STEP 5	L	L	L	L	L	H	H	H
...	...	...	...	...	...	...	...	...
STEP N	L	L	L	L	L	L	H	H
END CONFIG	L	L	L	L	L	L	L	H

C.2 Hardware Monitoring Block

C.2.1 Board Test Mode

Board test mode for the Hardware Monitor Block is implemented as an XOR-chain as described in the subsection below. The XOR chain for the Hardware Monitor Block is self-contained within the Hardware Monitor Block. The XOR chain for the rest of the chip is separate from the XOR chain for the Hardware Monitor Block.

Board test mode for the Hardware Monitoring Block can be entered by setting the 'XEN' bit high via SMBus, the part enters XOR test mode. programming a '1' to the XNOR_IN pin at power-up.

To exit the test mode, the XNOR_IN pin should be tied to '0' on the subsequent power up.

C.2.2 HW Monitor XOR-Chain Test Mode

The following signals are included in the XOR test tree:

- VID0, VID1, VID2, VID3, VID4, VID5/FANTACH3
- FANTACH1, FANTACH2, FANTACH4
- PWM2, PWM3
- nHWM_INT

The test mode is enabled by setting the 'XEN' bit high via SMBus, the part enters XOR test mode.

Since the test mode is XOR tree, the order of the signals in the tree is not important. SDA and SCL are not included in the test tree.

The following signals are not included in the XOR test tree:

- The SMBus pins: SDA, SCL, SDA2, SCL2, SDA1, SCL1
- All analog inputs: Remote2-, Remote2+, Remote1-, Remote1+, VCCP_IN, +12V_IN, +5V_IN, +5VTR_IN.
- All power supply pins - HVTR, HVSS