ISO7831 High-Performance, 8000 V_{PK} Reinforced Triple Digital Isolators

1 Features

- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25 V to 5.5 V Level Translation
- Wide Temperature Range: –55°C to 125°C
- Low Power Consumption, Typical 2.5 mA per Channel at 1 Mbps
- Low Propagation Delay: 11 ns Typical (5 V Supplies)
- Industry leading CMTI: ±100 kV/μs
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: >25 Years
- Wide Body SOIC-16 Package
- Safety and Regulatory Approvals:
  - 8000 V_{PK} V_{IOTM} and 2121 V_{PK} V_{IORM} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5.7 kV_{RMS} Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 60601-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

3 Description

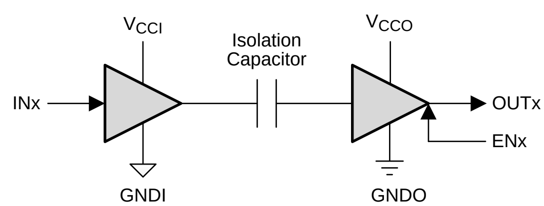
The ISO7831 is a high-performance, 3 -channel digital isolator with 8000 V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, and CQC. The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. ISO7831 has two forward and one reverse-direction channels . If the input power or signal is lost, default output is 'high' for the ISO7831 and 'low' for the ISO7831F device. See *Device Functional Modes* for further details. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of ISO7831 has been significantly enhanced to ease system-level ESD, EFT, Surge and Emissions compliance. ISO7831 is available in 16-pin SOIC wide-body (DW) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7831 ISO7831F	SOIC, DW (16)	10.30 mm x 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

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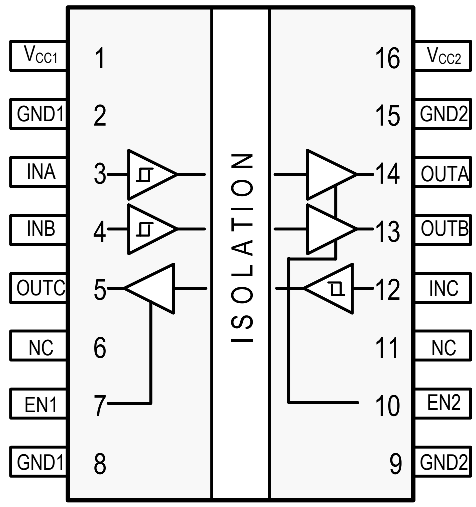
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2015) to Revision A	**Page**
• Changed From: 1-page Product Preview To: Production datasheet	1

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	—	Ground connection for V_{CC2}
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	12	I	Input, channel C
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	5	O	Output, channel C
NC	6,11	—	Not connected
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

See [1]

			MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage[2]		–0.5	6	V
	Voltage	INx	–0.5	V_{CCX} + 0.5[3]	V
		OUTx			
		ENx			
I_O	Output current		–15	15	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO}[1] = 5 V	–4			mA
		V_{CCO}[1] = 3.3 V	–2			
		V_{CCO}[1] = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO}[1] = 5 V			4	mA
		V_{CCO}[1] = 3.3 V			2	
		V_{CCO}[1] = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI}[1]		V_{CCI}[1]	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}[1]	V
DR	Signaling rate		0		100	Mbps
T_J	Junction temperature[2]		–55		150	°C
T_A	Ambient temperature		–55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) To maintain the recommended operating conditions for T_J, see *Thermal Information*.

6.4 Thermal Information

THERMAL METRIC[1]		DW (SOIC) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	
ψ_{JT}	Junction-to-top characterization parameter	15.5	
ψ_{JB}	Junction-to-board characterization parameter	43.1	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Rating

			VALUE	UNIT
P_D	Maximum power dissipation by ISO7831	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave	150	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7831		50	
P_{D2}	Maximum power dissipation by side-2 of ISO7831		100	

6.6 Electrical Characteristics, 5 V

$V_{CC1} = V_{CC2} = 5$ V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = –4$ mA; see Figure 7		V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 × V_{CCO} (1)			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ (1) at INx or ENx				10	μA
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx or ENx		–10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ (1) or 0 V; see Figure 10		70	100		kV/μs
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: $V_I = 0$ V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		1.0	1.6	mA
I_{CC2}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: $V_I = 0$ V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		0.8	1.3	mA
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , $V_I = 0$ V(Devices without suffix F)		3.3	4.8	mA
I_{CC2}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , $V_I = 0$ V(Devices without suffix F)		2	2.9	mA
I_{CC1}	Supply current	DC signal	DC signal: $V_I = 0$ V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		1.4	2.3	mA
I_{CC2}	Supply current	DC signal	DC signal: $V_I = 0$ V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		1.7	2.6	mA
I_{CC1}	Supply current	DC signal	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , $V_I = 0$ V(Devices without suffix F)		3.8	5.6	mA
I_{CC2}	Supply current	DC signal	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , $V_I = 0$ V(Devices without suffix F)		3	4.3	mA
I_{CC1}	Supply current	1 Mbps	AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		2.6	4	mA
I_{CC2}	Supply current	1 Mbps	AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		2.4	3.6	mA
I_{CC1}	Supply current	10 Mbps	AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		3.2	4.5	mA
I_{CC2}	Supply current	10 Mbps	AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		3.4	4.6	mA
I_{CC1}	Supply current	100 Mbps	AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		8.7	10.5	mA
I_{CC2}	Supply current	100 Mbps	AC signal: All channels switching with square wave clock input; $C_L = 15$ pF		13.2	15.8	mA

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.7 Electrical Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 7		V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 × V_{CCO} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			μA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0 V; see Figure 10		70	100		kV/μs
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.0	1.6	mA
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		0.8	1.3	
I_{CC1}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		3.3	4.8	
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		1.9	2.9	
I_{CC1}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.4	2.3	
I_{CC2}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , V_I = V_{CCI} (Devices without suffix F)		1.7	2.6	
I_{CC1}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		3.8	5.6	
I_{CC2}		DC signal	DC signal: V_I = V_{CCI} (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		2.9	4.3	
I_{CC1}		1 Mbps	AC signal: All channels switching with square wave clock input; C_L = 15 pF		2.6	4	
I_{CC2}		1 Mbps			2.4	3.5	
I_{CC1}		10 Mbps			3.0	4.3	
I_{CC2}		10 Mbps			3.1	4.3	
I_{CC1}		100 Mbps			6.9	8.3	
I_{CC2}		100 Mbps			10.1	12.2	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.8 Electrical Characteristics, 2.5 V

$V_{CC1} = V_{CC2} = 2.5$ V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 7		V_{CCO}[1] – 0.4	V_{CCO}[1] – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 7			0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis			0.1 × V_{CCO}[1]			V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$[1] at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$[1] or 0 V; see Figure 10		70	100		kV/μs
I_{CC1}	Supply current	Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		0.9	1.6	mA
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: V_I = 0 V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		0.8	1.3	
I_{CC1}		Disable; EN1 = EN2 = 0 V	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		3.3	4.8	
I_{CC2}		Disable; EN1 = EN2 = 0 V	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		1.9	2.9	
I_{CC1}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		1.4	2.3	
I_{CC2}		DC signal	DC signal: V_I = 0 V (Devices with suffix F) , $V_I = V_{CCI}$ (Devices without suffix F)		1.7	2.6	
I_{CC1}		DC signal	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		3.8	5.6	
I_{CC2}		DC signal	DC signal: $V_I = V_{CCI}$ (Devices with suffix F) , V_I = 0 V(Devices without suffix F)		2.9	4.3	
I_{CC1}		1 Mbps	AC signal: All channels switching with square wave clock input; C_L = 15 pF		2.6	4	
I_{CC2}		1 Mbps			2.3	3.5	
I_{CC1}		10 Mbps			2.9	4.3	
I_{CC2}		10 Mbps			2.9	4.1	
I_{CC1}		100 Mbps			5.8	7.2	
I_{CC2}		100 Mbps			8.2	10.0	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.9 Switching Characteristics, 5 V

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	6	11	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$	See Figure 7		0.55	4.1	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction channels			2.5	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 7		1.7	3.9	ns
t_f	Output signal fall time	See Figure 7		1.9	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 8		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output	See Figure 8		12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		10	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.90		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.10 Switching Characteristics, 3.3 V

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	6	10.8	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$	See Figure 7		0.7	4.2	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction channels			2.2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 7		0.8	3	ns
t_f	Output signal fall time	See Figure 7		0.8	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 8		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output	See Figure 8		17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.11 Switching Characteristics, 2.5 V

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7	7.5	11.7	17.5	ns
PWD (1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$	See Figure 7		0.66	4.2	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2.2	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 7		1	3.5	ns
t_f	Output signal fall time	See Figure 7		1.2	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 8		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output	See Figure 8		22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		18	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output	See Figure 8		2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		2	2.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output	See Figure 8		18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 9		0.2	9	μs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.12 Typical Characteristics

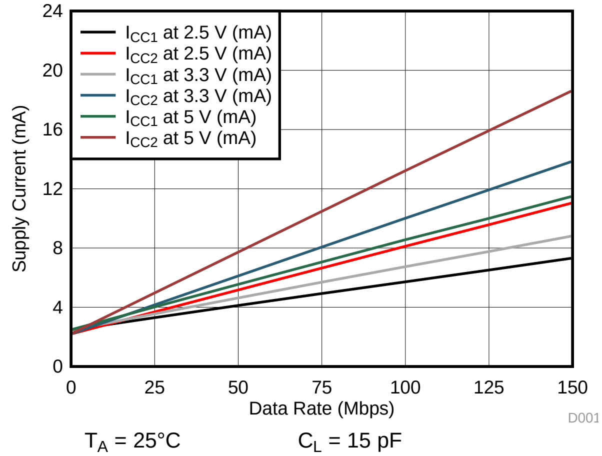


Figure 1. Supply Current vs Data Rate (With 15-pF Load)

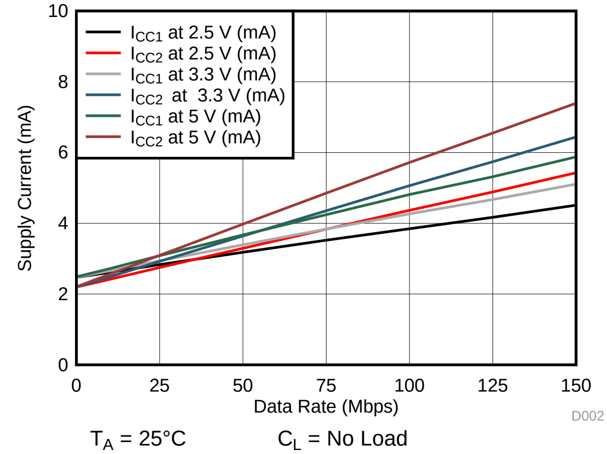


Figure 2. Supply Current vs Data Rate (With No Load)

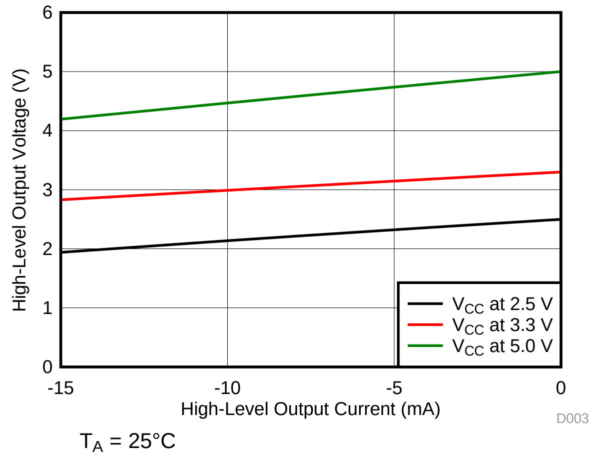


Figure 3. High-Level Output Voltage vs High-level Output Current

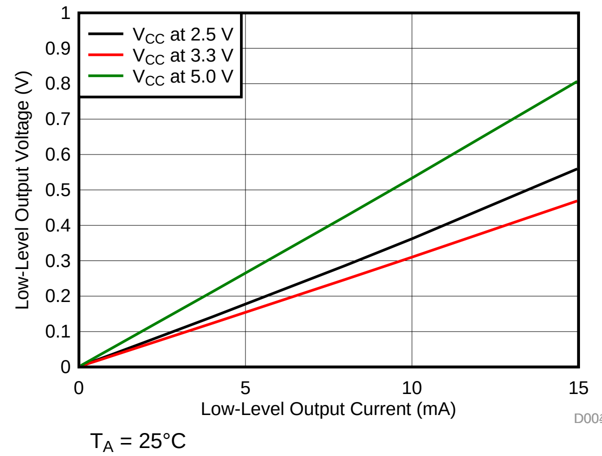


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

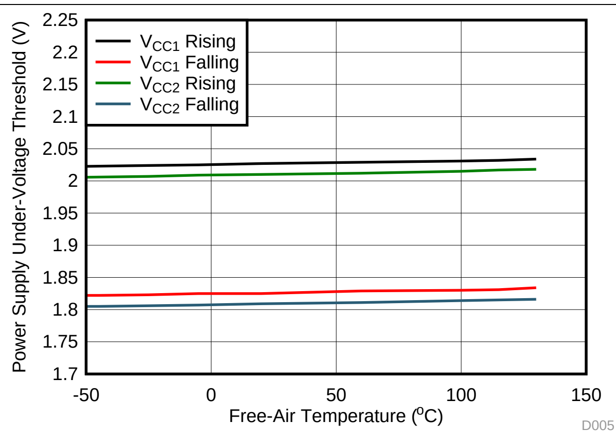


Figure 5. Power Supply Undervoltage Threshold vs Free-Air Temperature

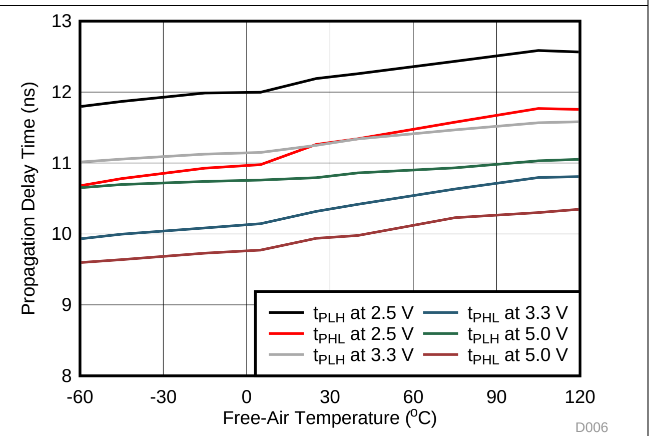
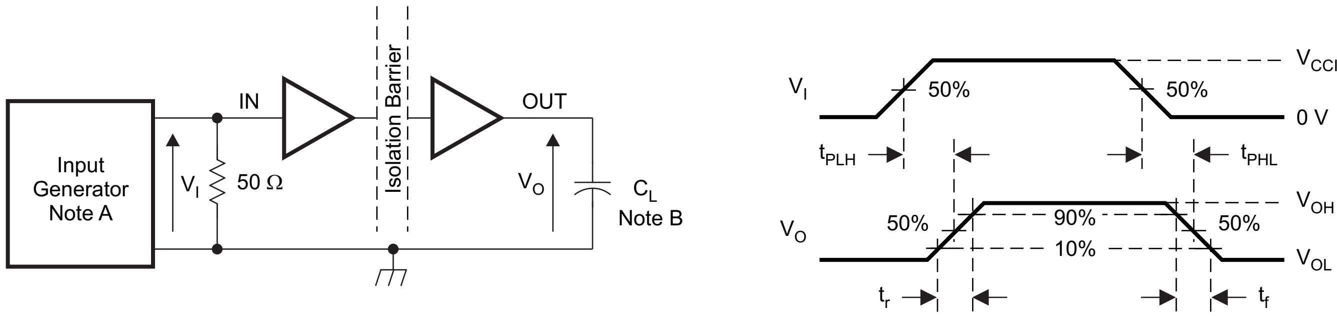


Figure 6. Propagation Delay Time vs Free-Air Temperature

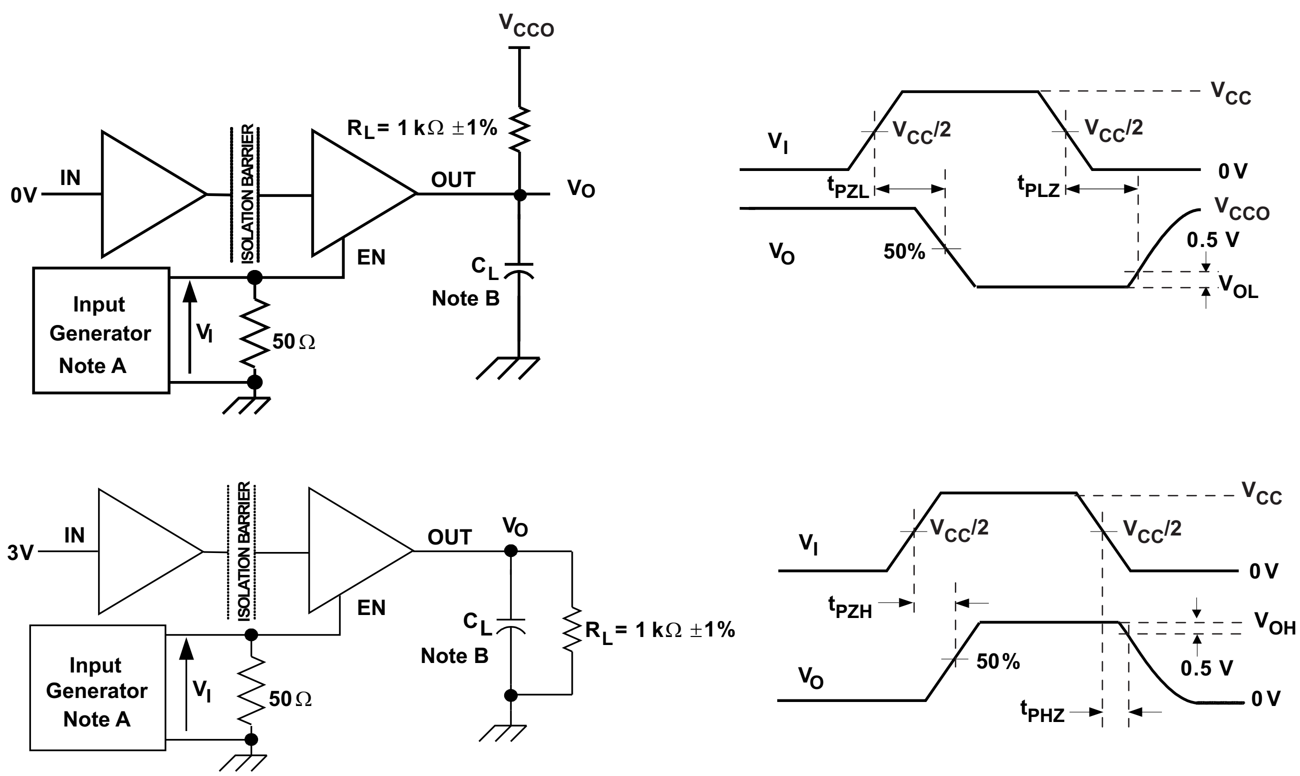
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7. Switching Characteristics Test Circuit and Voltage Waveforms

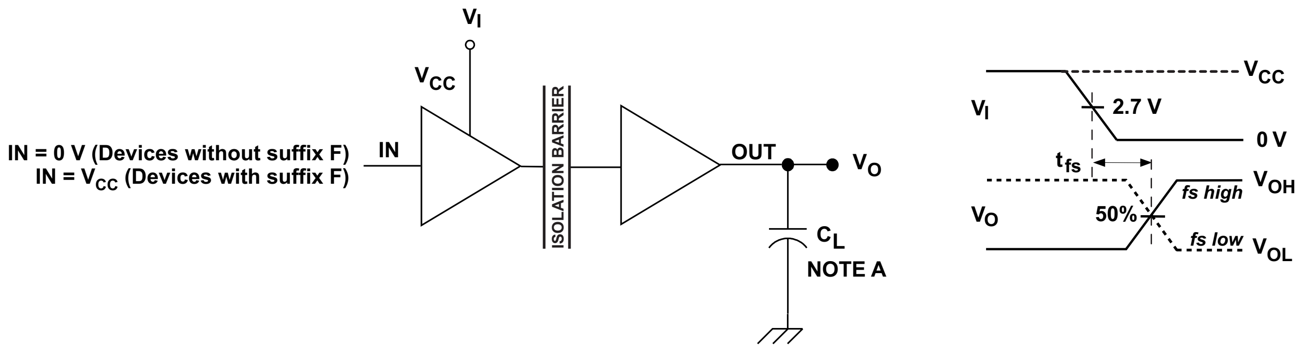


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

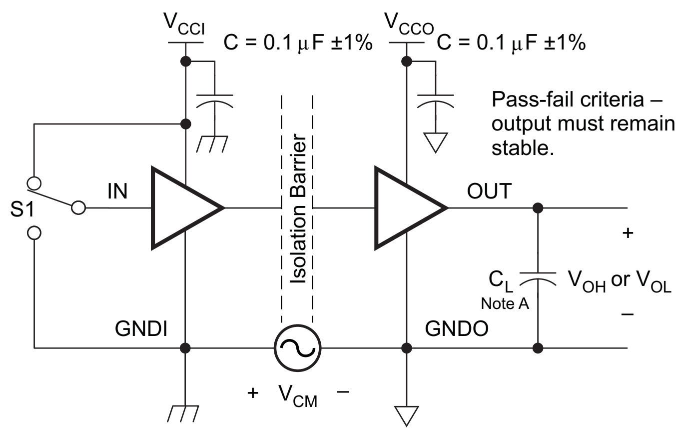
Figure 8. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

ISO7831 employs an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. ISO7831 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 11, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

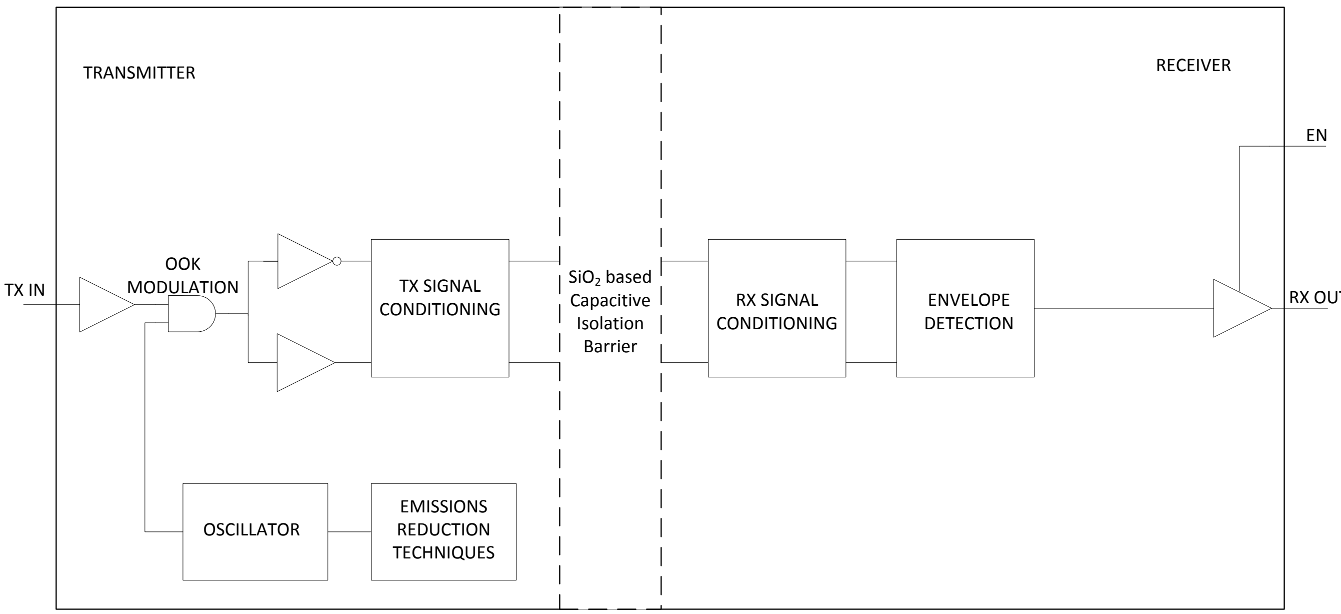


Figure 11. Conceptual Block Diagram of a Digital Capacitive Isolator

Also a conceptual detail of how the ON/OFF Keying scheme works is shown in Figure 12.

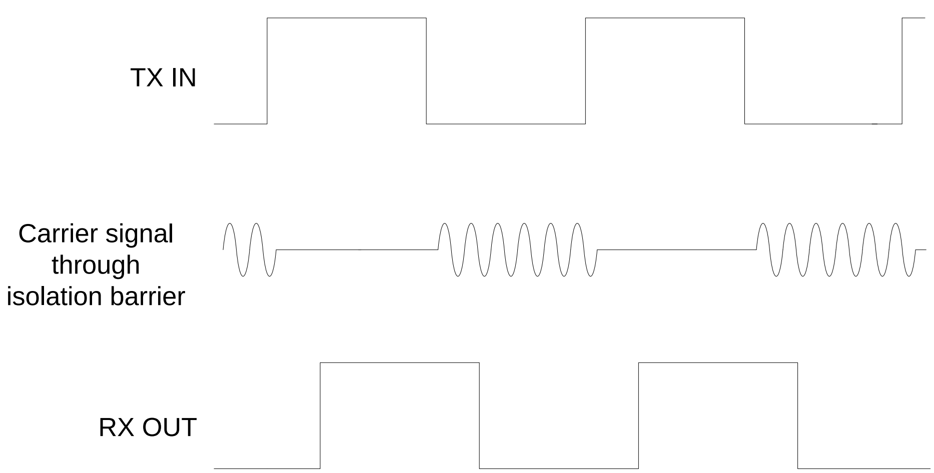


Figure 12. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7831	2 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High
ISO7831	2 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	Low

(1) See *Regulatory Information* for detailed isolation ratings.

8.3.1 High Voltage Feature Description

8.3.1.1 Package Insulation and Safety-Related Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	DW-16	8			mm
L(I02)(1)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	DW-16	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A		600			V
R_{IO}	Isolation resistance, input to output(2)	V_{IO} = 500 V, T_A = 25°C		10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		10^{11}			Ω
C_{IO}	Barrier capacitance, input to output(2)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz			2		pF
C_I	Input capacitance(3)	V_I = V_{CC}/2 + 0.4 x sin (2πft), f = 1 MHz, V_{CC} = 5 V			2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	μm
V_{IOWM}	Maximum isolation working voltage	Time dependent dielectric breakdown (TDDB) Test	1500	V_{RMS}
			2121	V_{DC}
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12				
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (qualification) t= 1 sec (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.6 x V_{IOSM} = 12800 V_{PK} (qualification)	8000	V_{PK}
V_{IORM}	Maximum repetitive peak isolation voltage		2121	V_{PK}
V_{PR}	Input-to-output test voltage	Method a, After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	2545	V_{PK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	3394	
		Method b1, V_{PR} = V_{IORM} x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	
R_S	Isolation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstanding isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 sec (qualification), V_{TEST} = 1.2 x V_{ISO} = 6840 V_{RMS}, t = 1 sec (100% production)	5700	V_{RMS}

(1) Climatic Classification 55/125/21

8.3.1.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	I
Installation classification	Rated mains voltage ≤ 600 V_{RMS}	I–IV
	Rated mains voltage ≤ 1000 V_{RMS}	I–III

8.3.1.4 Regulatory Information

DW package certifications are complete.

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed., 300 V_{RMS} max working voltage; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage	Single protection, 5700 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716

(1) Production tested ≥ 6840 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current for DW-16 Package	$R_{θJA}$ = 78.9°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			288	mA
		$R_{θJA}$ = 78.9°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			440	
		$R_{θJA}$ = 78.9°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			576	
P_S	Safety input, output, or total power	$R_{θJA}$ = 78.9°C/W, T_J = 150°C, T_A = 25°C			1584	mW
T_S	Maximum case temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a High-K test board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance

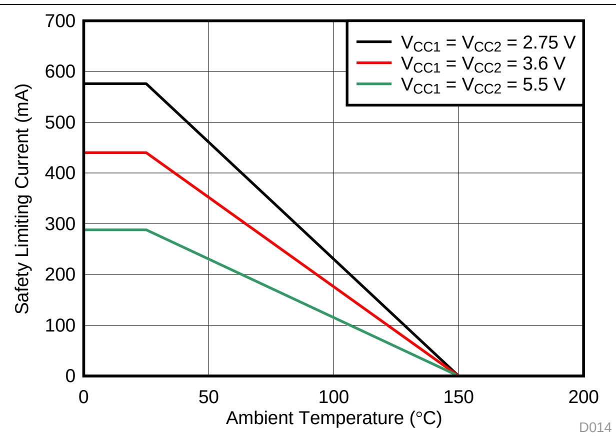


Figure 13. Thermal Derating Curve per VDE for DW-16 Package

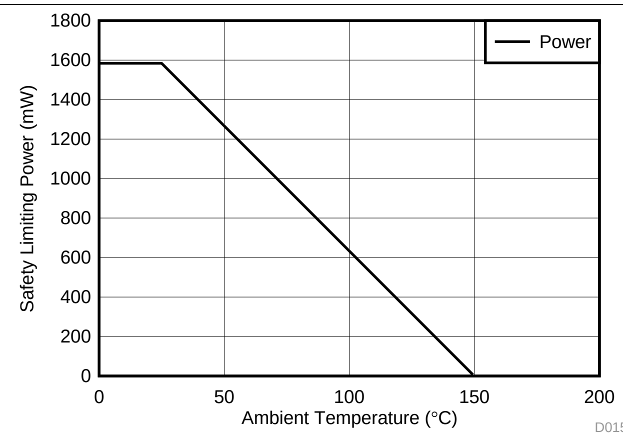


Figure 14. Thermal Derating Curve for Safety Limiting Power per VDE

8.4 Device Functional Modes

ISO7831 functional modes are shown in Table 1.

Table 1. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq 2.25$ V); PD = Powered down ($V_{CC} \leq 1.7$ V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

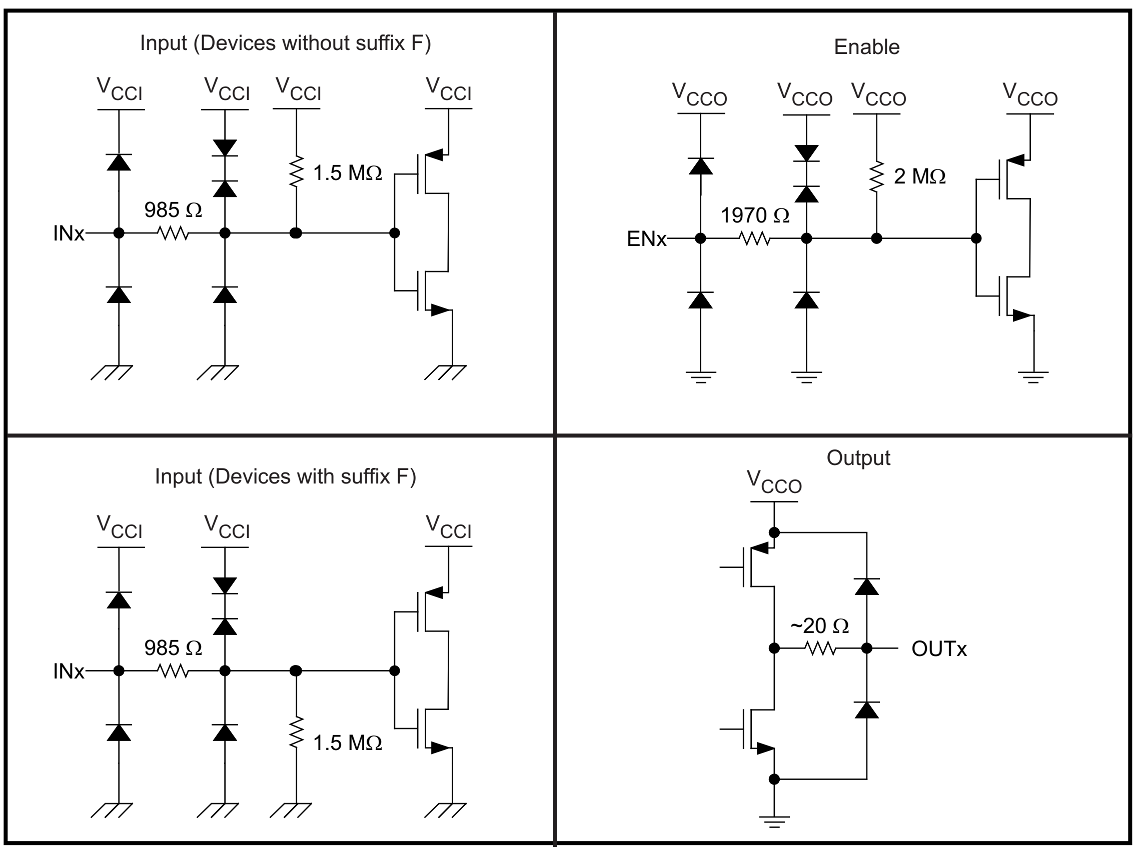


Figure 15. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7831 is a high-performance, quad-channel digital isolator with 5.7 kV_{RMS} isolation voltage. The device comes with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption. ISO7831 uses single-ended CMOS-logic switching technology. Its supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The Isolated SPI Interface is shown in Figure 16.

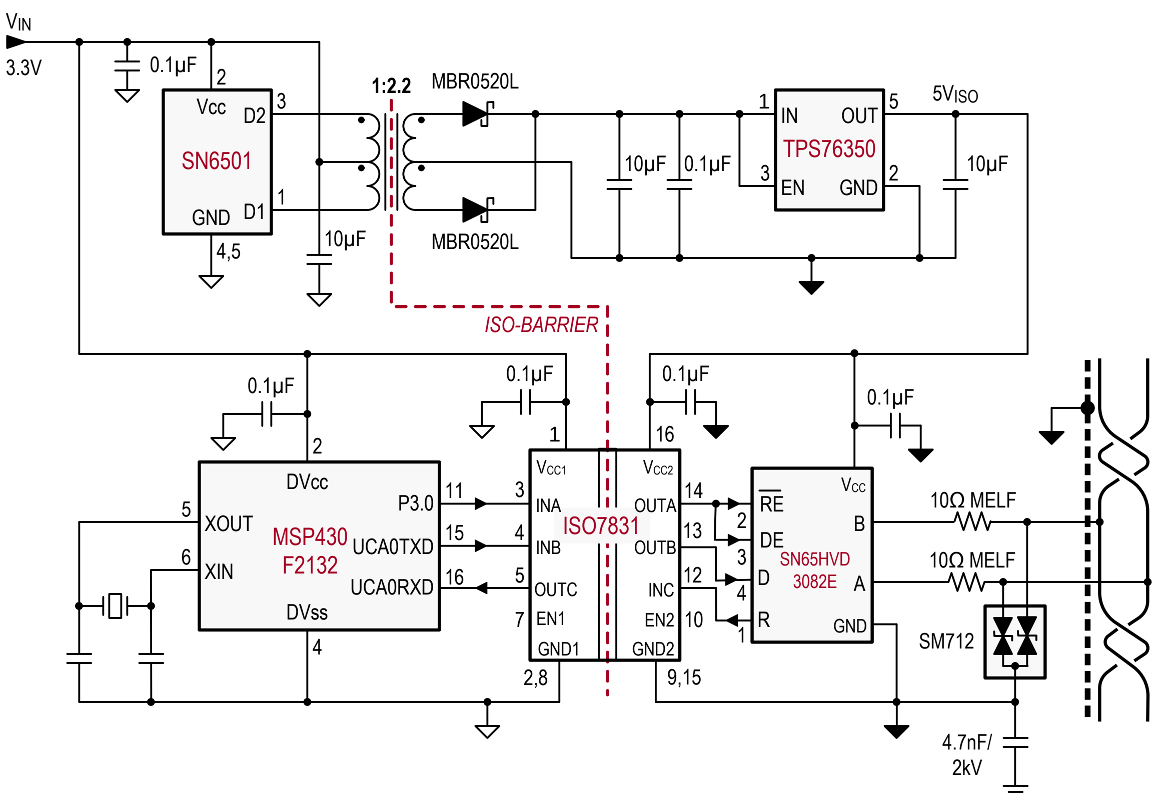


Figure 16. Isolated SPI Interface for an Analog Input Module With 16 Input

Typical Application (continued)

9.2.1 Design Requirements

For ISO7831, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO7831 only needs two external bypass capacitors to operate.

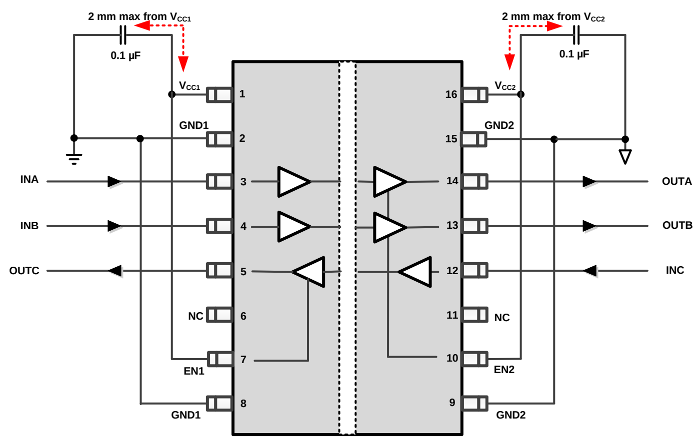


Figure 17. Typical ISO7831 Circuit Hook-up

9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7831 incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.2.3 Application Curve

Typical eye diagram of ISO7831 indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

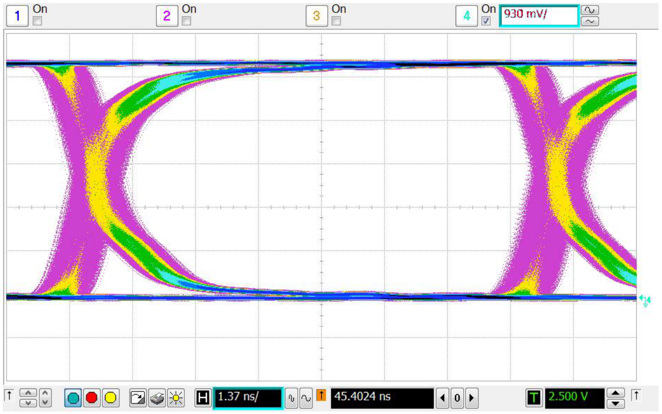


Figure 18. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 19). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see application note SLLA284, *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (flame retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

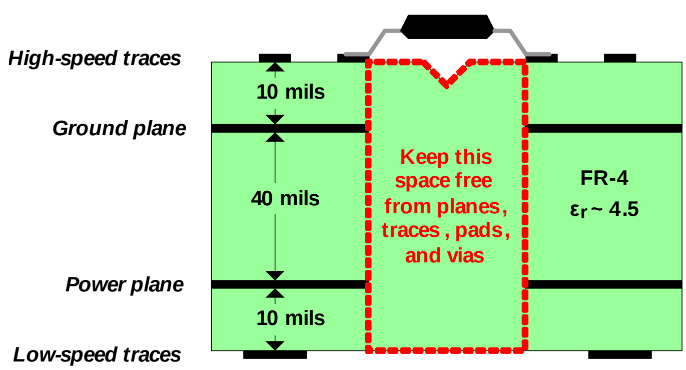


Figure 19. Layout Example Schematic

12 Device and Documentation Support

12.1 Documentation Support

SN6501 Transformer Driver for Isolated Power Supplies, SLLSEA0

Digital Isolator Design Guide, SLLA284, .

12.1.1 Related Documentation

See the *Isolation Glossary* (SLLA353)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7831	Click here	Click here	Click here	Click here	Click here
ISO7831F	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

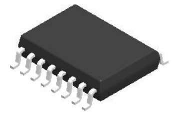
12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

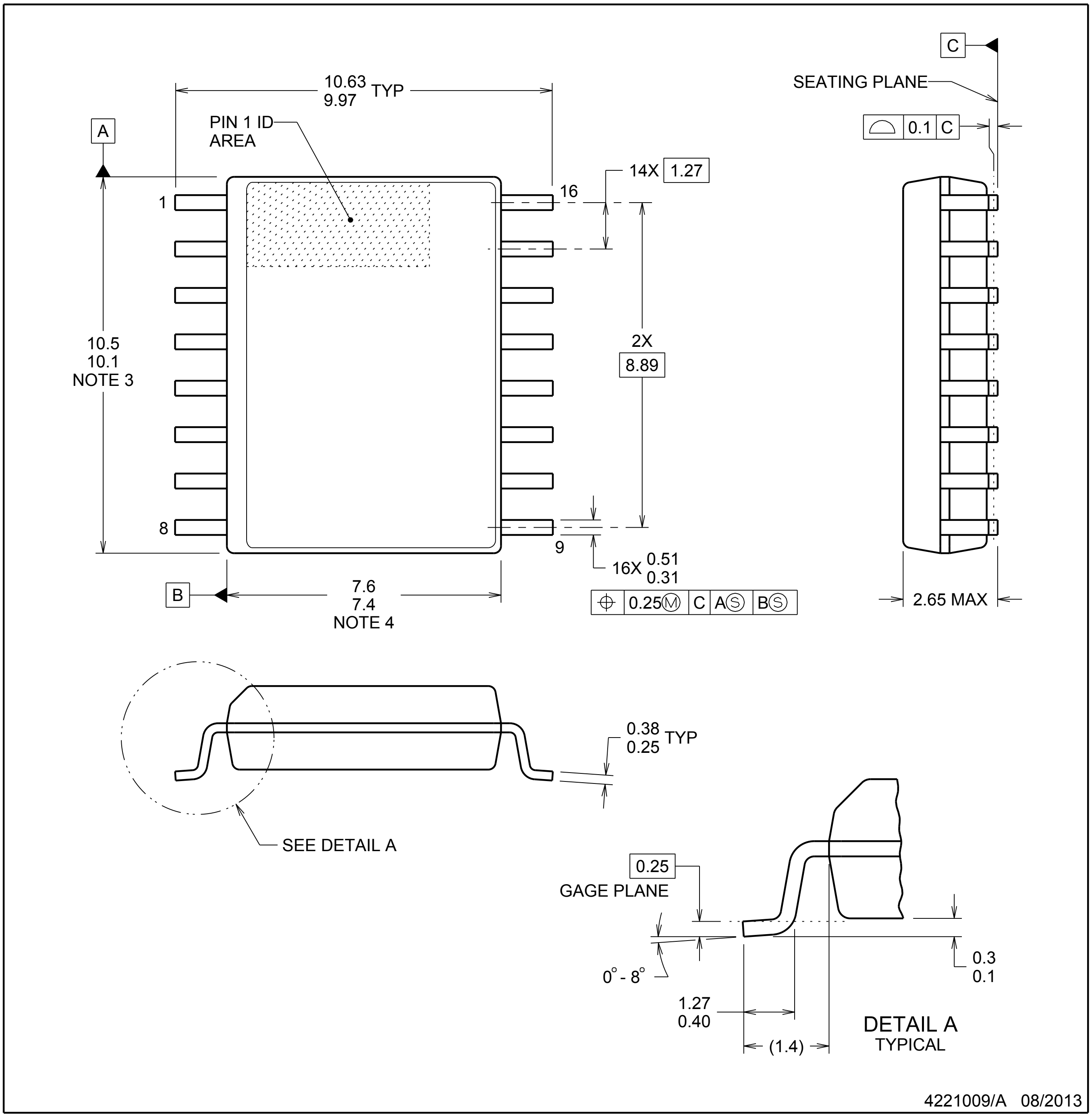
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DW0016B

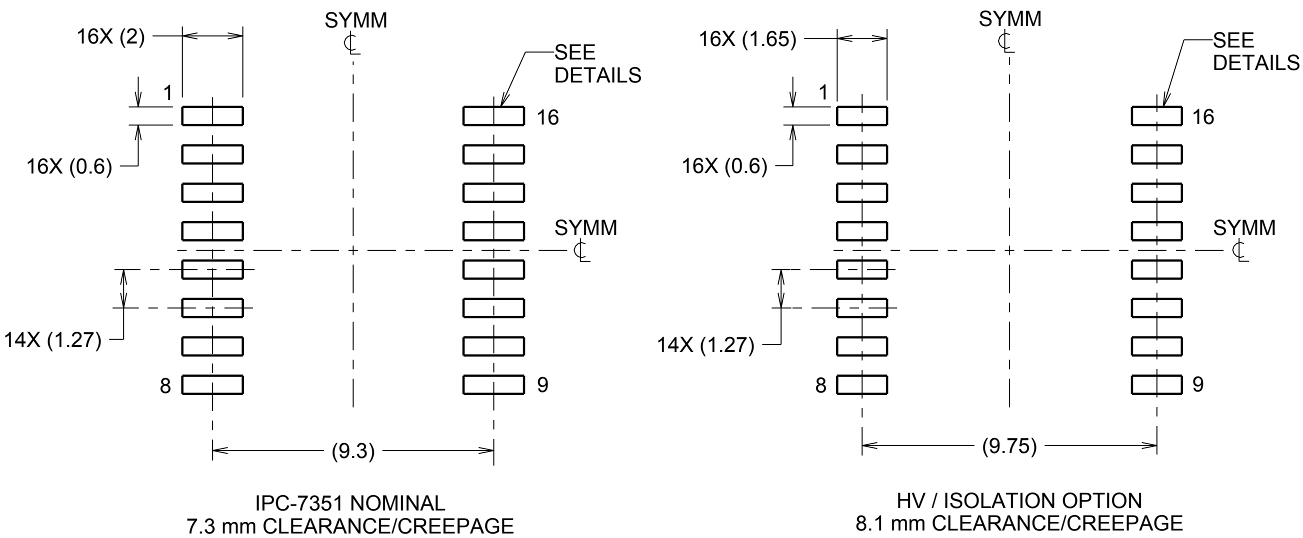
SOIC - 2.65 mm max height

SOIC

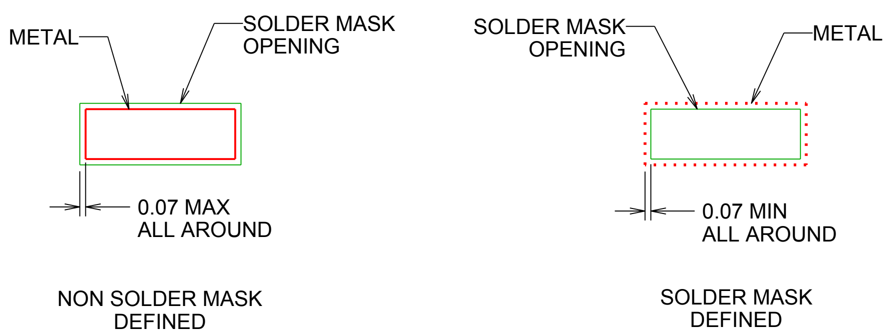


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.



LAND PATTERN EXAMPLE
SCALE:4X

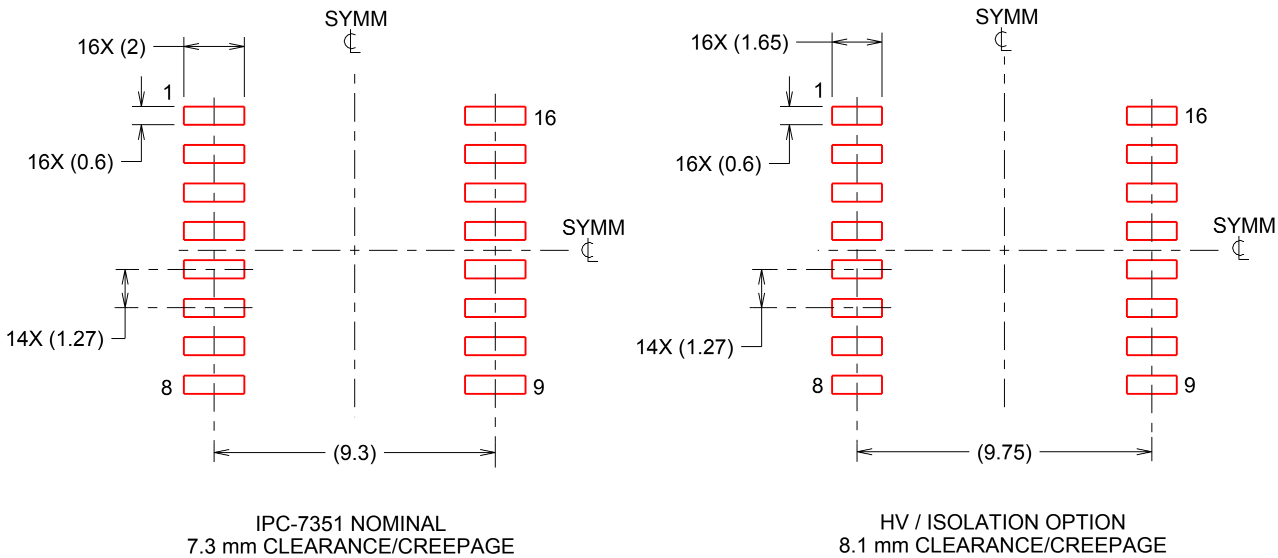


SOLDER MASK DETAILS

4221009/A 08/2013

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/A 08/2013

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7831DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7831	Samples
ISO7831DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7831	Samples
ISO7831FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7831F	Samples
ISO7831FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7831F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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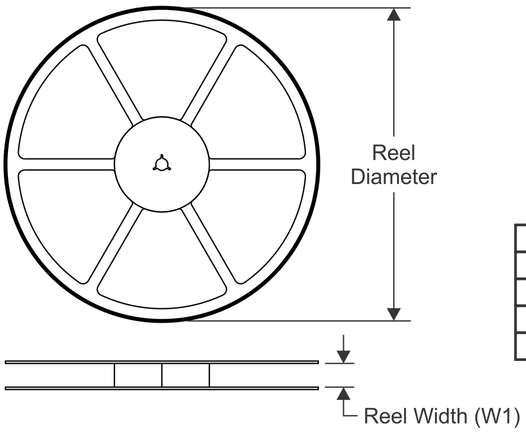
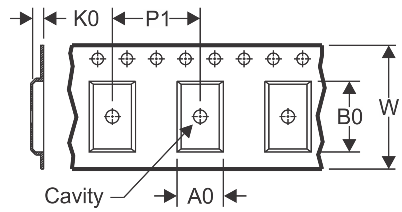
TAPE AND REEL INFORMATION

REEL DIMENSIONS

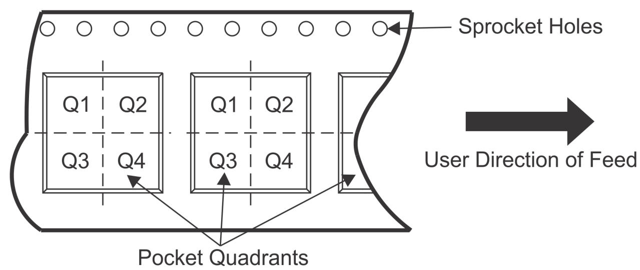


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

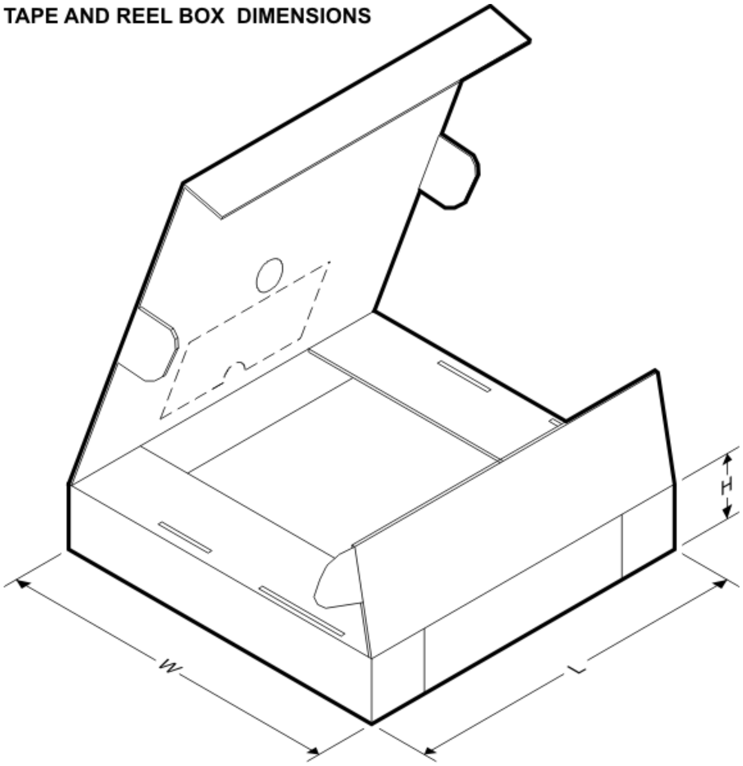
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7831DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7831FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7831DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7831FDWR	SOIC	DW	16	2000	367.0	367.0	38.0

IMPORTANT NOTICE

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