# SmartFusion2 System-on-Chip FPGAs

## Introduction

Microsemi's SmartFusion®2 system-on-chip (SoC) FPGAs integrate fourth generation flash-based FPGA fabric, an ARM® Cortex™-M3 processor, and high performance communications interfaces on a single chip. The SmartFusion2 FPGA is the industry's lowest power, the most secure, and has the highest reliability of any programmable logic solution. SmartFusion2 offers up to 3.6X the gate density and up to 2X the performance of previous flash-based FPGA families and includes multiple memory blocks and multiply accumulate blocks for DSP processing. The 166 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high speed USB. High speed serial interfaces enable PCIe®, XAUI/XGXS plus native SERDES communication while DDR2/DDR3 memory controllers provide high speed memory interfaces.

## SmartFusion2 Device Status

| Family Devices | Status |
|---|---|
| M2S005 | Preliminary |
| M2S010T/M2S010 | Preliminary |
| M2S025T/M2S025 | Preliminary |
| M2S050T/M2S050 | Production* |
| M2S090T/M2S090 | Advance |
| M2S100T/M2S100 | Advance |
| M2S150T/M2S150 | Advance |

*Note: Power numbers have a status of Preliminary.*

## SmartFusion2 Product Brief and Pin Descriptions

The product brief and pin descriptions are published separately:

*SmartFusion2 Product Brief*

*SmartFusion2 Pin Descriptions*

# Table of Contents

# List of Figures

# List of Tables

## Logic Element Specifications



## Global Resource Characteristics



## FPGA Fabric SRAM



## On-Chip Oscillators



## Clock Conditioning Circuits (CCC)



## JTAG



## Serial Peripheral Interface (SPI) Characteristics



## System Controller SPI Characteristics



## Inter-Integrated Circuit ($I^2C$) Characteristics

## Mathblock Timing Characteristics



## PCIe Electrical and Timing AC and DC Characteristics

Microsemi

# SmartFusion2 DC and Switching Characteristics

## General Specifications

### Operating Conditions

Stresses beyond those listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2-2 on page 2-2 is not implied.

***Table 1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | | Units | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| VDD | DC core supply voltage. Must always power this pin. | –0.3 | 1.32 | V | |
| VPP | Power supply for charge pumps (for normal operation and programming). Must always power this pin. | –0.3 | 3.63 | V | |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | –0.3 | 3.63 | V | |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | –0.3 | 3.63 | V | |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | –0.3 | 3.63 | V | |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0–5 | –0.3 | 3.63 | V | |
| SERDES_[01]_PLL_VDDA | High supply voltage for PLL SERDES[01] | –0.3 | 3.63 | V | |
| SERDES_[01]_L[0123]_VDDAPLL | Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply. | –0.3 | 2.75 | V | |
| SERDES_[01]_L[0123]_VDDAIO | Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply. | –0.3 | 1.32 | V | |
| SERDES_[01]_VDD | PCIe/PCS power supply | –0.3 | 1.32 | V | |
| VDDIx | DC FPGA I/O buffer supply voltage for MSIO I/O bank | –0.3 | 3.63 | V | |
| | DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks | –0.3 | 2.75 | V | |
| VI | I/O Input voltage for MSIO I/O bank | –0.3 | 3.63 | V | |
| | I/O Input voltage for MSIOD/DDRIO I/O bank | –0.3 | 2.75 | V | |
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP. | –0.3 | 3.63 | V | |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C | 1 |
| $T_J$ | Junction temperature | – | 125 | °C | |

*Note: 1. For flash programming and retention maximum limits, refer to Table 3 on page 11. For recommended operating conditions, refer to Table 2 on page 10.*

**Table 2 • Recommended Operating Conditions**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| $T_J$ | Operating junction temperature | Commercial | 0 | 25 | 85 | °C | |
| | | Industrial | –40 | 25 | 100 | °C | |
| | Programming junction temperatures | Commercial | 0 | 25 | 85 | °C | |
| | | Industrial | 0 | 25 | 85 | °C | |
| VDD | DC core supply voltage. Must always power this pin. | | 1.14 | 1.2 | 1.26 | V | |
| VPP | Power supply for charge pumps (for normal operation and programming) | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0 to PLL5 | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| SERDES_[01]_PLL_VDDA | High supply voltage for PLL SERDES[01] | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| SERDES_[01]_L[0123]_VDDAPLL | Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply. | | 2.375 | 2.5 | 2.625 | V | |
| SERDES_[01]_L[0123]_VDDAIO | Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply. | | 1.14 | 1.2 | 1.26 | V | |
| SERDES_[01]_VDD | PCIe/PCS power supply | | 1.14 | 1.2 | 1.26 | V | |
| VDDIx | 1.2 V DC supply voltage | | 1.14 | 1.2 | 1.26 | V | |
| | 1.5 V DC supply voltage | | 1.425 | 1.5 | 1.575 | V | |
| | 1.8 V DC supply voltage | | 1.71 | 1.8 | 1.89 | V | |
| | 2.5 V DC supply voltage | | 2.375 | 2.5 | 2.625 | V | |
| | 3.3 V DC supply voltage | | 3.15 | 3.3 | 3.45 | V | |
| | LVDS differential I/O | | 2.375 | 2.5 | 3.45 | V | |
| | B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O | | 2.375 | 2.5 | 2.625 | V | |
| | LVPECL differential I/O | | 3.15 | 3.3 | 3.45 | V | |
| VREFx | Reference voltage supply for FDDR (bank 0) and MDDR (bank 5) | | 0.49 * VDDIx | 0.5 * VDDIx | 0.51 * VDDIx | V | |
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP. | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| | | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |

**Table 3 • FPGA and Embedded Flash Programming, Storage, and Operating Limits**

| Product Grade | Storage Temperature | Programming Temperature | Element | Grade Programming Cycles | Retention |
|---|---|---|---|---|---|
| Commercial | Min. $T_J$ = 0°C<br>Max. $T_J$ = 85°C | Min. $T_J$ = 0°C<br>Max. $T_J$ = 85°C | FPGA | 500 | 20 years |
| | | Min. $T_J$ = 0°C<br>Max. $T_J$ = 85°C | Embedded flash | < 1,000 | 20 years |
| | | | | < 10,000 | 10 years |
| Industrial | Min. $T_J$ = –40°C<br>Max. $T_J$ = 100°C | Min. $T_J$ = 0°C<br>Max. $T_J$ = 85°C | FPGA | 500 | 20 years |
| | | Min. $T_J$ = –40°C<br>Max. $T_J$ = 100°C | Embedded flash | < 1,000 | 20 years |
| | | | | < 10,000 | 10 years |

# Thermal Characteristics

## Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad \textit{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad \textit{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \textit{EQ 3}$$

where

$\theta_{JA}$ = Junction-to-air thermal resistance
$\theta_{JB}$ = Junction-to-board thermal resistance
$\theta_{JC}$ = Junction-to-case thermal resistance
$T_J$ = Junction temperature
$T_A$ = Ambient temperature
$T_B$ = Board temperature (measured 1.0 mm away from the package edge)
$T_C$ = Case temperature
P = Total power dissipated by the device

***Table 4 •*** **Package Thermal Resistance**

| Product | $\theta_{JA}$ | | | $\theta_{JC}$ | $\theta_{JB}$ | Units |
|---|---|---|---|---|---|---|
| | Still Air | 1.0 m/s | 2.5 m/s | | | |
| **M2S005** | | | | | | |
| FG484 | 19.4 | 15.8 | 14.6 | 9.7 | 5.3 | °C/W |
| VF400 | 19.36 | 15.81 | 14.63 | 9.74 | 5.27 | °C/W |
| **M2S010** | | | | | | |
| FG484 | 18.2 | 14.8 | 13.6 | 8.8 | 4.9 | °C/W |
| VF400 | 18.22 | 14.83 | 13.62 | 8.83 | 4.92 | °C/W |
| **M2S025** | | | | | | |
| FG484 | 17.0 | 13.7 | 12.5 | 7.7 | 4.2 | °C/W |
| VF400 | 17.03 | 13.66 | 12.45 | 7.66 | 4.18 | °C/W |
| FCS325 | 29.17 | 24.87 | 23.12 | 14.44 | 2.31 | °C/W |
| **M2S050** | | | | | | |
| FG484 | 15.3 | 12.2 | 11 | 6.3 | 3.2 | °C/W |
| FG896 | 14.7 | 12.5 | 10.9 | 7.2 | 4.9 | °C/W |
| VF400 | 17.53 | 14.17 | 12.63 | 3.32 | 2.81 | °C/W |
| FCS325 | 27.38 | 23.18 | 21.41 | 12.47 | 1.59 | °C/W |
| **M2S090** | | | | | | |
| FG484 | 14.64 | 11.37 | 10.16 | 5.43 | 2.77 | °C/W |
| FG676 | 14.5 | 11.2 | 10.4 | 6.8 | 3.2 | °C/W |

## Theta-JA

Junction-to-ambient thermal resistance ($\theta_{JA}$) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

*EQ 4*

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2S050T-FG896 package at commercial temperature and in still air, where

$\theta_{JA}$ = 14.7°C/W (taken from Table 4 on page 12).

$T_A$ = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{14.7°C/W} = 1.088\ W$$

*EQ 5*

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

### Theta-JB

Junction-to-board thermal resistance ($\theta_{JB}$) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

### Theta-JC

Junction-to-case thermal resistance ($\theta_{JC}$) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

# Calculating Power Dissipation

## Quiescent Supply Current

***Table 5 •*** **Quiescent Supply Current Characteristics**

| Power Supplies/Blocks | Modes and Configurations | | Notes |
|---|---|---|---|
| | Non-Flash*Freeze mode | Flash*Freeze mode | |
| FPGA Core | On | Off | |
| VDD / SERDES_[01]_VDD | On | On | 1 |
| VPP / VPPNVM | On | On | |
| MSS_MDDR_PLL_VDDA / FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA / PLL0_PLL1_MSS_MDDR_VDDA | 0 V | 0 V | |
| SERDES_[01]_PLL_VDDA | 0 V | 0 V | 3 |
| SERDES_[01]_L[0123]_VDDAPLL | On | On | 3 |
| SERDES_[01]_L[0123]_VDDAIIO | On | On | 3 |
| VDDIx | On | On | 2, 4 |
| VREFx | On | On | |
| MSSDDR CLK | 32 KHz | 32 KHz | |
| RAM | On | Sleep state | |
| MSS Controller | 50 MHz | 50 MHz | |
| 50 MHz Oscillator (enable/disable) | Enabled | Disabled | |
| 1 MHz Oscillator (enable/disable) | Disabled | Disabled | |
| Crystal Oscillator (enable/disable) | Disabled | Disabled | |

*Notes:*

1. *SERDES_[01]_VDD Power Supply is shorted to VDD.*
2. *VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the SmartFusion2 Board Design Guidelines application note.*
3. *SERDES and DDR blocks to be unused.*
4. *No Differential (i.e. LVDS) I/O's or ODT attributes to be used.*

***Table 6 •*** **Quiescent Supply Current**

| Parameter | Modes | Conditions[1] | M2S005 VDD=1.2 V | M2S010 VDD=1.2 V | M2S025 VDD=1.2 V | M2S050 VDD=1.2 V | M2S090 VDD=1.2 V | M2S100 VDD=1.2 V | M2S150 VDD=1.2 V | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| IDC1 | Non-Flash*Freeze | Typical | 5.4 | 6.6 | 8.6 | 11.4 | 15.0 | 21.7 | 21.7 | mA |
| | | Commercial | 17.4 | 25.0 | 36.4 | 52.3 | 72.8 | 112.2 | 112.2 | mA |
| | | Industrial | 25.1 | 36.6 | 54.0 | 78.1 | 109.4 | 169.4 | 169.4 | mA |
| IDC2 | Flash*Freeze | Typical | 1.6 | 2.2 | 2.8 | 3.1 | 4.2 | 5.2 | 5.2 | mA |
| | | Commercial | 10.8 | 15.2 | 19.6 | 21.8 | 29.0 | 35.6 | 35.6 | mA |
| | | Industrial | 16.6 | 23.4 | 30.1 | 33.6 | 44.7 | 54.8 | 54.8 | mA |

*Notes:*

1. *Typical conditions are at 25°C, Commercial conditions are at 85°C, and Industrial conditions are at 100°C.*
2. *The power numbers are preliminary.*

# Average Fabric Temperature and Voltage Derating Factors

***Table 7 •*** **Average Temperature and Voltage Derating Factors for Fabric Timing Delays (normalized to $T_J$ = 85°C, worst-case VDD = 1.14 V)**

| Array Voltage VDD (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | **–40°C** | **0°C** | **25°C** | **70°C** | **85°C** | **100°C** |
| 1.14 | 0.83 | 0.89 | 0.92 | 0.98 | 1.00 | 1.02 |
| 1.2 | 0.75 | 0.80 | 0.83 | 0.89 | 0.91 | 0.93 |
| 1.26 | 0.69 | 0.73 | 0.76 | 0.81 | 0.83 | 0.85 |

# Timing Model

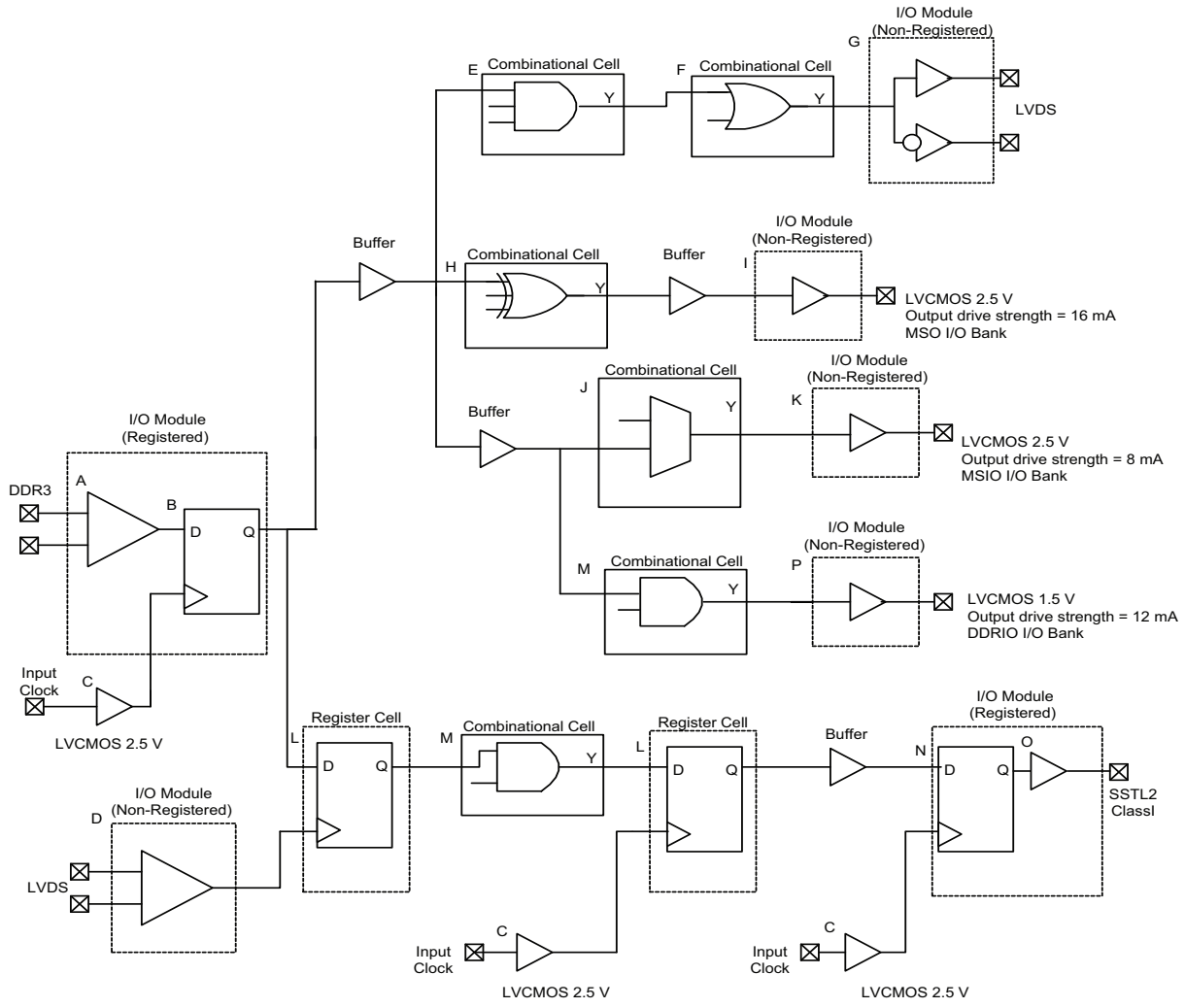



***Figure 1 •*** **Timing Model**

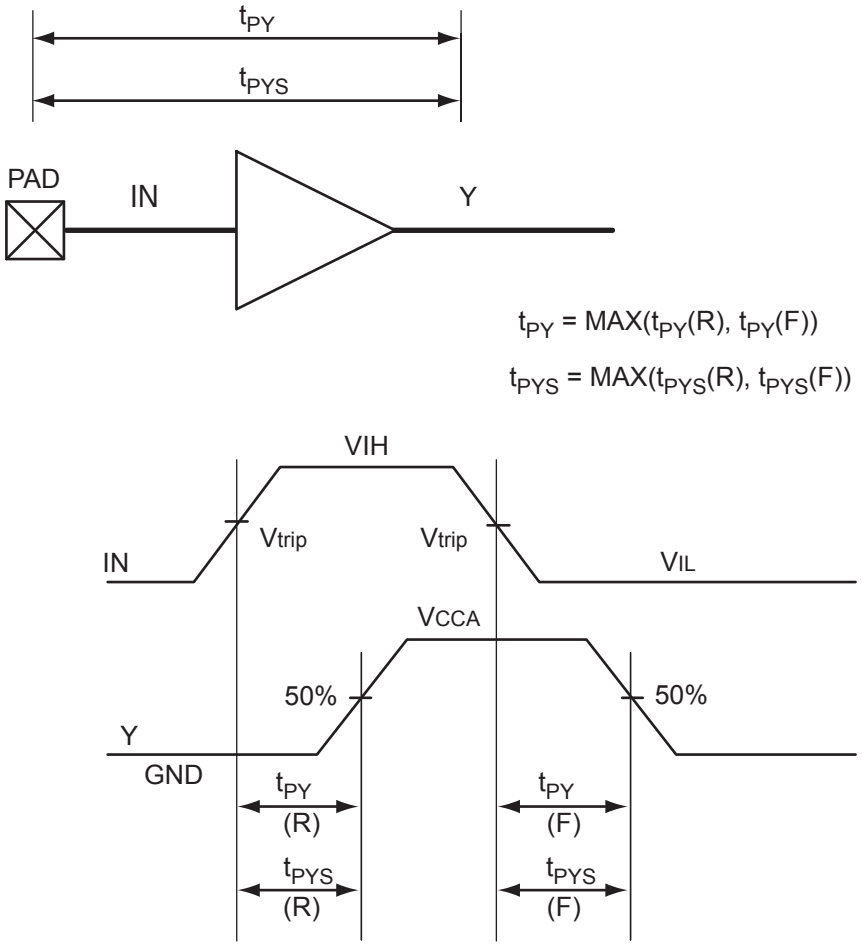
**Table 8 • Timing Model Parameters**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Index | Parameter | Description | Value | Units | For more information |
|---|---|---|---|---|---|
| A | $t_{PY}$ | Propagation delay of DDR3 receiver | 1.605 | ns | Refer to page 51 |
| B | $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.16 | ns | Refer to page 67 |
| | $t_{ISUD}$ | Setup Time of the Input Data Register | 0.357 | ns | Refer to page 67 |
| C | $t_{RCKH}$ | Input High Delay for Global Clock | 1.53 | ns | Refer to page 81 |
| | $t_{RCKL}$ | Input Low Delay for Global Clock | 0.897 | ns | Refer to page 81 |
| D | $t_{PY}$ | Input Propagation Delay of LVDS Receiver | 2.774 | ns | Refer to page 56 |
| E | $t_{DP}$ | Propagation Delay of a three-input AND Gate | 0.198 | ns | Refer to page 77 |
| F | $t_{DP}$ | Propagation Delay of an OR Gate | 0.179 | ns | Refer to page 77 |
| G | $t_{DP}$ | Propagation Delay of an LVDS Transmitter | 2.136 | ns | Refer to page 56 |
| H | $t_{DP}$ | Propagation Delay of a three-input XOR Gate | 0.241 | ns | Refer to page 77 |
| I | $t_{DP}$ | Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16 mA on the MSIO Bank | 2.412 | ns | Refer to page 25 |
| J | $t_{DP}$ | Propagation Delay of a two-input MUX gate | 0.179 | ns | Refer to page 77 |
| K | $t_{DP}$ | Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8 mA on the MSIO Bank | 2.309 | ns | Refer to page 25 |
| L | $t_{CLKQ}$ | Clock-to-Q of the Data Register | 0.108 | ns | Refer to page 79 |
| | $t_{SUD}$ | Setup Time of the Data Register | 0.254 | ns | Refer to page 79 |
| M | $t_{DP}$ | Propagation Delay of a two-input AND gate | 0.179 | ns | Refer to page 77 |
| N | $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 0.263 | ns | Refer to page 67 |
| | $t_{OSUD}$ | Setup Time of the Output Data Register | 0.19 | ns | Refer to page 67 |
| O | $t_{DP}$ | Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank | 2.055 | ns | Refer to page 45 |
| P | $t_{DP}$ | Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12 mA, fast slew on the DDRIO Bank | 3.316 | ns | Refer to page 33 |

# User I/O Characteristics

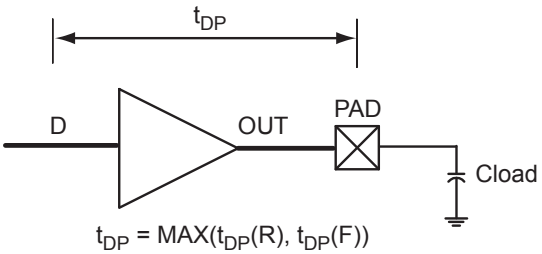
There are three types of I/Os supported in the SmartFusion2 FPGA Family: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *SmartFusion2 FPGA Fabric Architecture User Guide*.

## Input Buffer and AC Loading



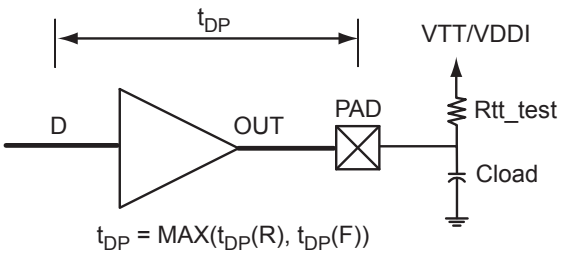
## Output Buffer and AC Loading

Single-Ended I/O Test Setup



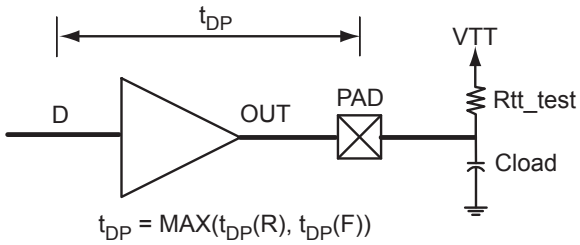

$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

HSTL/PCI Test Setup



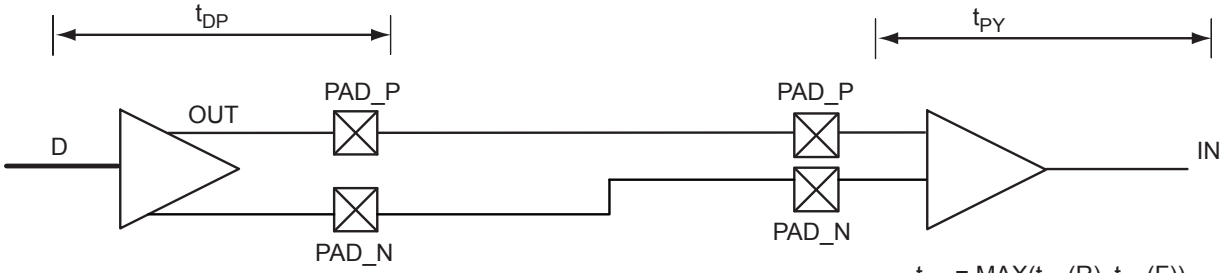

$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

Voltage-Referenced, Singled-Ended I/O Test Setup




$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

Differential I/O Test Setup




$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$

$t_{PYS} = MAX(t_{PYS}(R), t_{PYS}(F))$

## Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 2.

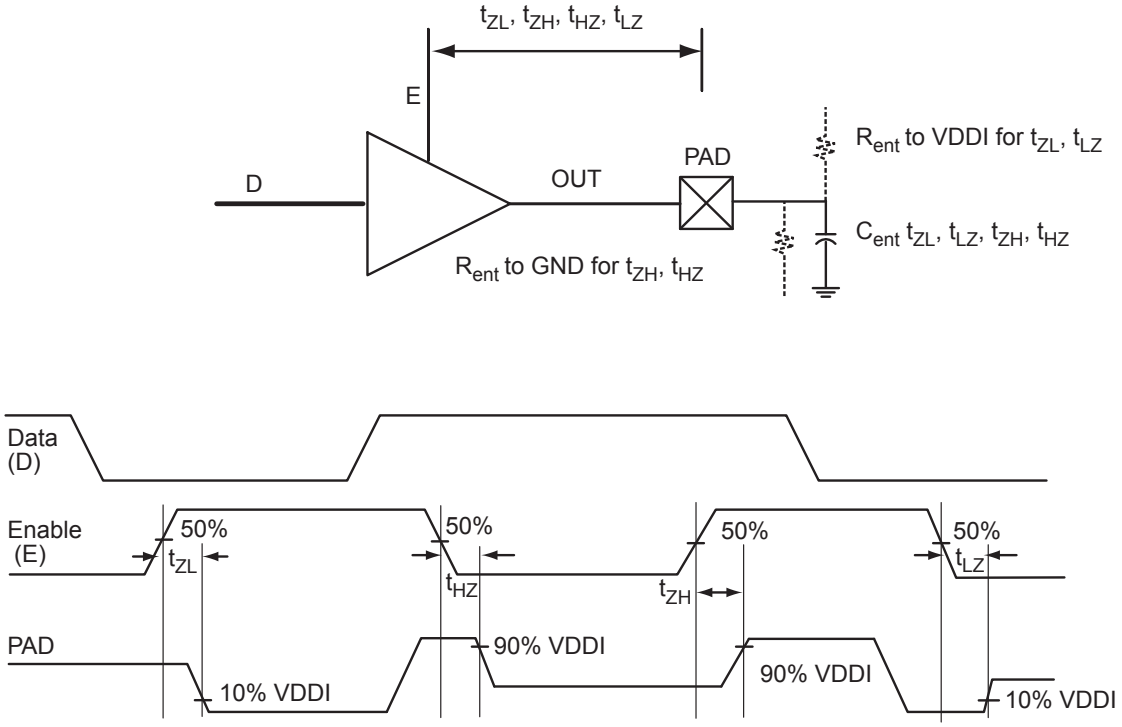



***Figure 2* • Tristate Buffer for Enable Path Test Point**

## Detailed I/O Characteristics

**Table 9 • Input Capacitance**

| Symbol | Definition | Minimum | Maximum | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | – | 10 | pF |

**Table 10 • I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level**

| VDDI Domain | DDRIO I/O Bank | | | | Notes |
|---|---|---|---|---|---|
| | R(WEAK PULL-UP) at VOH (Ω) | | R(WEAK PULL-DOWN) at VOL (Ω) | | |
| | Min. | Max. | Min. | Max. | |
| 3.3 V | N/A | N/A | N/A | N/A | – |
| 2.5 V | 10 k | 15.1 k | 9.98 k | 15.3 k | 1, 2 |
| 1.8 V | 10.3 k | 16.2 k | 10.3 k | 16.6 k | 1, 2 |
| 1.5 V | 10.6 k | 17.2 k | 10.6 k | 17.9 k | 1, 2 |
| 1.2 V | 11.1 k | 19.3 k | 11.2 k | 20.9 k | 1, 2 |

*Notes:*

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

**Table 11 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level**

| VDDI Domain | MSIO I/O Bank | | | | Notes |
|---|---|---|---|---|---|
| | R(WEAK PULL-UP) at VOH (Ω) | | R(WEAK PULL-DOWN) at VOL (Ω) | | |
| | Min. | Max. | Min. | Max. | |
| 3.3 V | 9.9 k | 14.5 k | 9.98 k | 14.9 k | – |
| 2.5 V | 10 k | 15 k | 10.1 k | 15.6 k | 1, 2 |
| 1.8 V | 10.4 k | 16.2 k | 10.4 k | 17.3 k | 1, 2 |
| 1.5 V | 10.7 k | 17.3 k | 10.8 k | 18.9 k | 1, 2 |
| 1.2 V | 11.3 k | 19.7 k | 11.5 k | 22.7 k | 1, 2 |

*Notes:*

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

**Table 12 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank**
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level**

| VDDI Domain | R(WEAK PULL-UP) at VOH (Ω) | | R(WEAK PULL-DOWN) at VOL (Ω) | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| 3.3 V | N/A | N/A | N/A | N/A | – |
| 2.5 V | 9.6 K | 14.1 K | 9.5 K | 13.9 K | 1, 2 |
| 1.8 V | 9.7 K | 14.7 K | 9.7 K | 14.5 K | 1, 2 |
| 1.5 V | 9.9 K | 15.3 K | 9.8 K | 15 K | 1, 2 |
| 1.2 V | 10.3 K | 16.7 K | 10 K | 16.2 K | 1, 2 |

*Notes:*

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

**Table 13 • Schmitt Trigger Input Hysteresis**
**Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typical, unless otherwise noted) |
|---|---|
| 3.3 V LVTTL / LVCMOS / PCI / PCI-X | 0.05 × VDDI (worst-case) |
| 2.5 V LVCMOS | 0.05 × VDDI (worst-case) |
| 1.8 V LVCMOS | 0.1 × VDDI (worst-case) |
| 1.5 V LVCMOS | 60 mV |
| 1.2 V LVCMOS | 20 mV |

# Single-Ended I/O Standards

## Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in SmartFusion2 SoC FPGAs are LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

## 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 14 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank ONLY)**

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V | |
| **LVTTL/LVCMOS 3.3 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High | | 2.0 | – | 3.45 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.8 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **LVCMOS 3.3 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | VDDI – 0.4 | – | – | V | 1 |
| VOL | DC output logic Low | | – | – | 0.4 | V | 1 |
| **LVTTL 3.3 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | 2.4 | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.4 | V | |

*Note: 1. The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*

**Table 15 • LVTTL/LVCMOS 3.3 V AC Specifications (Applicable to MSIO I/O Bank ONLY)**

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVTTL/LVCMOS 3.3 V Maximum Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC Loading: 17pF load, maximum drive/slew | – | – | 600 | Mbps | |
| **LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 1.4 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

**Table 16 • LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications**

| Output Drive Selection / MSIO I/O Bank | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA | Notes |
|---|---|---|---|---|---|
| 2 mA | VDDI – 0.4 | 0.4 | 2 | 2 | |
| 4 mA | VDDI – 0.4 | 0.4 | 4 | 4 | |
| 8 mA | VDDI – 0.4 | 0.4 | 8 | 8 | |
| 12 mA | VDDI – 0.4 | 0.4 | 12 | 12 | |
| 16 mA | VDDI – 0.4 | 0.4 | 16 | 16 | |
| 20 mA | VDDI – 0.4 | 0.4 | 20 | 20 | |

*Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.*

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 3.0 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 17 • LVTTL/LVCMOS 3.3 V Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | $t_{PYS}$ | | Units |
|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | |
| **LVTTL/LVCMOS 3.3 V (for MSIO I/O bank)** | None | 2.262 | 2.663 | 2.289 | 2.695 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 18 • LVTTL/LVCMOS 3.3 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVTTL/LVCMOS 3.3 V (for MSIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 3.192 | 3.755 | 3.47 | 4.083 | 2.969 | 3.494 | 1.856 | 2.183 | 3.337 | 3.926 | ns |
| 4 mA | Slow | 2.331 | 2.742 | 2.673 | 3.145 | 2.526 | 2.973 | 3.034 | 3.569 | 4.451 | 5.236 | ns |
| 8 mA | Slow | 2.135 | 2.511 | 2.33 | 2.741 | 2.297 | 2.703 | 4.532 | 5.331 | 4.825 | 5.676 | ns |
| 12 mA | Slow | 2.052 | 2.414 | 2.107 | 2.479 | 2.162 | 2.544 | 5.75 | 6.764 | 5.445 | 6.406 | ns |
| 16 mA | Slow | 2.062 | 2.425 | 2.072 | 2.438 | 2.145 | 2.525 | 5.993 | 7.05 | 5.625 | 6.618 | ns |
| 20 mA | Slow | 2.148 | 2.527 | 1.999 | 2.353 | 2.088 | 2.458 | 6.262 | 7.367 | 5.876 | 6.913 | ns |

## LVCMOS 2.5 V

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-5A.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 19 • LVCMOS 2.5 V DC Voltage Specification**

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 2.5 V Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | |
| **LVCMOS 2.5 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High for (MSIOD and DDRIO I/O bank) | | 1.7 | – | 2.625 | V | |
| VIH (DC) | DC input logic High (for MSIO I/O bank) | | 1.7 | – | 3.45 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.7 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **LVCMOS 2.5 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | VDDI – 0.4 | – | – | V | 1 |
| VOL | DC output logic Low | | – | – | 0.4 | V | 1 |

*Note: 1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.*

**Table 20 • LVCMOS 2.5 V AC Specifications**

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 2.5 V Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for DDRIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 250 | Mbps | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 410 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 420 | Mbps | |
| **LVCMOS 2.5 V AC Calibrated Impedance Option** | | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O bank) | | – | 75, 60, 50, 33, 25, 20 | – | Ohms | |
| **LVCMOS 2.5 V AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 1.2 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

**Table 21 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA | Notes |
|---|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (with Software Default Fixed Calibration Codes) | Min. | Max. | | | |
| 2 mA | 2 mA | 2 mA | VDDI – 0.4 | 0.4 | 2 | 2 | |
| 4 mA | 4 mA | 4 mA | VDDI – 0.4 | 0.4 | 4 | 4 | |
| 6 mA | 6 mA | 6 mA | VDDI – 0.4 | 0.4 | 6 | 6 | |
| 8 mA | 8 mA | 8 mA | VDDI – 0.4 | 0.4 | 8 | 8 | |
| 12 mA | 12 mA | 12 mA | VDDI – 0.4 | 0.4 | 12 | 12 | |
| 16 mA | N/A | 16 mA | VDDI – 0.4 | 0.4 | 16 | 16 | |

*Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.*

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 22 • LVCMOS 2.5 V Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | $t_{PYS}$ | | Units |
|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | |
| **LVCMOS 2.5 V (for DDRIO I/O bank)** | None | 1.823 | 2.145 | 1.932 | 2.274 | ns |
| **LVCMOS 2.5 V (for MSIO I/O bank)** | None | 2.486 | 2.925 | 2.495 | 2.935 | ns |
| **LVCMOS 2.5 V (for MSIOD I/O bank)** | None | 2.29 | 2.694 | 2.305 | 2.712 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 23 • LVCMOS 2.5 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 2.5 V (for DDRIO I/O bank with FIXED CODES)** | | | | | | | | | | | | |
| 2 mA | Slow | 3.657 | 4.302 | 3.393 | 3.991 | 3.675 | 4.323 | 3.894 | 4.582 | 3.552 | 4.18 | ns |
| | Medium | 3.374 | 3.97 | 3.139 | 3.693 | 3.396 | 3.995 | 3.635 | 4.277 | 3.253 | 3.828 | ns |
| | Medium fast | 3.239 | 3.811 | 3.036 | 3.572 | 3.261 | 3.836 | 3.519 | 4.141 | 3.128 | 3.681 | ns |
| | Fast | 3.224 | 3.793 | 3.029 | 3.563 | 3.246 | 3.818 | 3.512 | 4.132 | 3.119 | 3.67 | ns |
| 4 mA | Slow | 3.095 | 3.641 | 2.705 | 3.182 | 3.088 | 3.633 | 4.738 | 5.575 | 4.348 | 5.116 | ns |
| | Medium | 2.825 | 3.324 | 2.488 | 2.927 | 2.823 | 3.321 | 4.492 | 5.285 | 4.063 | 4.781 | ns |
| | Medium fast | 2.701 | 3.178 | 2.384 | 2.804 | 2.698 | 3.173 | 4.364 | 5.135 | 3.945 | 4.642 | ns |
| | Fast | 2.69 | 3.165 | 2.377 | 2.796 | 2.687 | 3.161 | 4.359 | 5.129 | 3.94 | 4.636 | ns |

**Table 23 • LVCMOS 2.5 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| 6 mA | Slow | 2.919 | 3.434 | 2.491 | 2.93 | 2.902 | 3.414 | 5.085 | 5.983 | 4.674 | 5.5 | ns |
| | Medium | 2.65 | 3.118 | 2.279 | 2.681 | 2.642 | 3.108 | 4.845 | 5.701 | 4.375 | 5.148 | ns |
| | Medium fast | 2.529 | 2.975 | 2.176 | 2.56 | 2.521 | 2.965 | 4.724 | 5.558 | 4.259 | 5.011 | ns |
| | Fast | 2.516 | 2.96 | 2.168 | 2.551 | 2.508 | 2.95 | 4.717 | 5.55 | 4.251 | 5.002 | ns |
| 8 mA | Slow | 2.863 | 3.368 | 2.427 | 2.855 | 2.844 | 3.346 | 5.196 | 6.114 | 4.769 | 5.612 | ns |
| | Medium | 2.599 | 3.058 | 2.217 | 2.608 | 2.59 | 3.047 | 4.952 | 5.827 | 4.471 | 5.261 | ns |
| | Medium fast | 2.483 | 2.921 | 2.114 | 2.487 | 2.473 | 2.91 | 4.832 | 5.685 | 4.364 | 5.134 | ns |
| | Fast | 2.467 | 2.902 | 2.106 | 2.478 | 2.457 | 2.89 | 4.826 | 5.678 | 4.348 | 5.116 | ns |
| 12 mA | Slow | 2.747 | 3.232 | 2.296 | 2.701 | 2.724 | 3.204 | 5.39 | 6.342 | 4.938 | 5.81 | ns |
| | Medium | 2.493 | 2.934 | 2.102 | 2.473 | 2.483 | 2.921 | 5.166 | 6.078 | 4.65 | 5.471 | ns |
| | Medium fast | 2.382 | 2.803 | 2.006 | 2.36 | 2.371 | 2.789 | 5.067 | 5.962 | 4.546 | 5.349 | ns |
| | Fast | 2.369 | 2.787 | 1.999 | 2.352 | 2.357 | 2.773 | 5.063 | 5.958 | 4.538 | 5.339 | ns |
| 16 mA | Slow | 2.677 | 3.149 | 2.213 | 2.604 | 2.649 | 3.116 | 5.575 | 6.56 | 5.08 | 5.977 | ns |
| | Medium | 2.432 | 2.862 | 2.028 | 2.386 | 2.421 | 2.848 | 5.372 | 6.32 | 4.801 | 5.649 | ns |
| | Medium fast | 2.324 | 2.734 | 1.937 | 2.278 | 2.311 | 2.718 | 5.297 | 6.233 | 4.7 | 5.531 | ns |
| | Fast | 2.313 | 2.721 | 1.929 | 2.269 | 2.3 | 2.706 | 5.296 | 6.231 | 4.699 | 5.529 | ns |
| **LVCMOS 2.5 V (for MSIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 3.48 | 4.095 | 3.855 | 4.534 | 3.785 | 4.453 | 2.12 | 2.494 | 3.45 | 4.059 | ns |
| 4 mA | Slow | 2.583 | 3.039 | 3.042 | 3.579 | 3.138 | 3.691 | 4.143 | 4.874 | 4.687 | 5.513 | ns |
| 6 mA | Slow | 2.392 | 2.815 | 2.669 | 3.139 | 2.82 | 3.317 | 4.909 | 5.775 | 5.083 | 5.98 | ns |
| 8 mA | Slow | 2.309 | 2.717 | 2.565 | 3.017 | 2.74 | 3.223 | 5.812 | 6.837 | 5.523 | 6.497 | ns |
| 12 mA | Slow | 2.333 | 2.745 | 2.437 | 2.867 | 2.626 | 3.089 | 6.131 | 7.213 | 5.712 | 6.72 | ns |
| 16 mA | Slow | 2.412 | 2.838 | 2.335 | 2.747 | 2.533 | 2.979 | 6.54 | 7.694 | 6.007 | 7.067 | ns |
| **LVCMOS 2.5 V (for MSIOD I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 2.206 | 2.596 | 2.678 | 3.15 | 2.64 | 3.106 | 4.935 | 5.805 | 4.74 | 5.576 | ns |
| 4 mA | Slow | 1.835 | 2.159 | 2.242 | 2.637 | 2.256 | 2.654 | 5.413 | 6.368 | 5.15 | 6.059 | ns |
| 6 mA | Slow | 1.709 | 2.01 | 2.132 | 2.508 | 2.167 | 2.549 | 5.813 | 6.838 | 5.499 | 6.469 | ns |
| 8 mA | Slow | 1.63 | 1.918 | 1.958 | 2.303 | 2.012 | 2.367 | 6.226 | 7.324 | 5.816 | 6.842 | ns |
| 12 mA | Slow | 1.648 | 1.939 | 1.86 | 2.187 | 1.921 | 2.259 | 6.519 | 7.669 | 6.027 | 7.09 | ns |

## 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-7A.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 24 • LVCMOS 1.8 V DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.710 | 1.8 | 1.89 | V | |
| **LVCMOS 1.8 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High for (MSIOD and DDRIO I/O bank) | | 0.65 * VDDI | – | 1.89 | V | |
| VIH (DC) | DC input logic High (for MSIO I/O bank) | | 0.65 * VDDI | – | 3.45 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.35 * VDDI | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **LVCMOS 1.8 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | VDDI – 0.45 | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.45 | V | |

**Table 25 • LVCMOS 1.8 V AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 1.8 V Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for DDRIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 280 | Mbps | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 295 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 320 | Mbps | |
| **LVCMOS 1.8 V AC Calibrated Impedance Option** | | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O bank) | | | 75, 60, 50, 33, 25, 20 | | Ohms | |
| **LVCMOS 1.8 V AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.9 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

**Table 26 • LVCMOS 1.8 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA | Notes |
|---|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min. | Max. | | | |
| 2 mA | 2 mA | 2 mA | VDDI – 0.45 | 0.45 | 2 | 2 | |
| 4 mA | 4 mA | 4 mA | VDDI – 0.45 | 0.45 | 4 | 4 | |
| 6 mA | 6 mA | 6 mA | VDDI – 0.45 | 0.45 | 6 | 6 | |
| 8 mA | 8 mA | 8 mA | VDDI – 0.45 | 0.45 | 8 | 8 | |
| 10 mA | 10 mA | 10 mA | VDDI – 0.45 | 0.45 | 10 | 10 | |
| 12 mA | N/A | 12 mA | VDDI – 0.45 | 0.45 | 12 | 12 | |
| N/A | N/A | 16 mA | VDDI – 0.45 | 0.45 | 16 | 16 | |

*Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.*

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 1.71 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 27 • LVCMOS 1.8 V Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | $t_{PYS}$ | | Units |
|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | |
| LVCMOS 1.8 V (for DDRIO I/O bank) | None | 1.968 | 2.315 | 2.099 | 2.47 | ns |
| | 50 | 1.992 | 2.343 | 2.229 | 2.622 | ns |
| | 75 | 1.979 | 2.327 | 2.179 | 2.564 | ns |
| | 150 | 1.978 | 2.327 | 2.136 | 2.512 | ns |
| LVCMOS 1.8 V (for MSIO I/O bank) | None | 2.898 | 3.411 | 2.883 | 3.393 | ns |
| | 50 | 3.05 | 3.59 | 3.044 | 3.583 | ns |
| | 75 | 2.999 | 3.53 | 2.987 | 3.516 | ns |
| | 150 | 2.947 | 3.469 | 2.933 | 3.452 | ns |
| LVCMOS 1.8 V (for MSIOD I/O bank) | None | 2.611 | 3.071 | 2.598 | 3.057 | ns |
| | 50 | 2.775 | 3.264 | 2.775 | 3.265 | ns |
| | 75 | 2.72 | 3.2 | 2.712 | 3.19 | ns |
| | 150 | 2.666 | 3.137 | 2.655 | 3.123 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 28 • LVCMOS 1.8 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.8 V (for DDRIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 4.234 | 4.981 | 3.646 | 4.29 | 4.245 | 4.995 | 4.908 | 5.774 | 4.434 | 5.216 | ns |
| | Medium | 3.824 | 4.498 | 3.282 | 3.861 | 3.834 | 4.511 | 4.625 | 5.441 | 4.116 | 4.843 | ns |
| | Medium fast | 3.627 | 4.267 | 3.111 | 3.66 | 3.637 | 4.279 | 4.481 | 5.272 | 3.984 | 4.687 | ns |
| | Fast | 3.605 | 4.241 | 3.097 | 3.644 | 3.615 | 4.253 | 4.472 | 5.262 | 3.973 | 4.674 | ns |
| 4 mA | Slow | 3.923 | 4.615 | 3.314 | 3.9 | 3.918 | 4.61 | 5.403 | 6.356 | 4.894 | 5.757 | ns |
| | Medium | 3.518 | 4.138 | 2.961 | 3.484 | 3.515 | 4.135 | 5.121 | 6.025 | 4.561 | 5.366 | ns |
| | Medium fast | 3.321 | 3.907 | 2.783 | 3.275 | 3.317 | 3.903 | 4.966 | 5.843 | 4.426 | 5.206 | ns |
| | Fast | 3.301 | 3.883 | 2.77 | 3.259 | 3.296 | 3.878 | 4.957 | 5.831 | 4.417 | 5.196 | ns |
| 6 mA | Slow | 3.71 | 4.364 | 3.104 | 3.652 | 3.702 | 4.355 | 5.62 | 6.612 | 5.08 | 5.977 | ns |
| | Medium | 3.333 | 3.921 | 2.779 | 3.27 | 3.325 | 3.913 | 5.346 | 6.289 | 4.777 | 5.62 | ns |
| | Medium fast | 3.155 | 3.712 | 2.62 | 3.083 | 3.146 | 3.702 | 5.21 | 6.13 | 4.657 | 5.479 | ns |
| | Fast | 3.134 | 3.688 | 2.608 | 3.068 | 3.125 | 3.677 | 5.202 | 6.12 | 4.648 | 5.468 | ns |
| 8 mA | Slow | 3.619 | 4.258 | 3.007 | 3.538 | 3.607 | 4.244 | 5.815 | 6.841 | 5.249 | 6.175 | ns |
| | Medium | 3.246 | 3.819 | 2.686 | 3.16 | 3.236 | 3.807 | 5.542 | 6.52 | 4.936 | 5.807 | ns |
| | Medium fast | 3.066 | 3.607 | 2.525 | 2.971 | 3.054 | 3.593 | 5.405 | 6.359 | 4.811 | 5.66 | ns |
| | Fast | 3.046 | 3.584 | 2.513 | 2.957 | 3.034 | 3.57 | 5.401 | 6.353 | 4.803 | 5.651 | ns |
| 10 mA | Slow | 3.498 | 4.115 | 2.878 | 3.386 | 3.481 | 4.096 | 6.046 | 7.113 | 5.444 | 6.404 | ns |
| | Medium | 3.138 | 3.692 | 2.569 | 3.023 | 3.126 | 3.678 | 5.782 | 6.803 | 5.129 | 6.034 | ns |
| | Medium fast | 2.966 | 3.489 | 2.414 | 2.841 | 2.951 | 3.472 | 5.666 | 6.665 | 5.013 | 5.897 | ns |
| | Fast | 2.945 | 3.464 | 2.401 | 2.826 | 2.93 | 3.448 | 5.659 | 6.658 | 5.003 | 5.886 | ns |
| 12 mA | Slow | 3.417 | 4.02 | 2.807 | 3.303 | 3.401 | 4.002 | 6.083 | 7.156 | 5.464 | 6.428 | ns |
| | Medium | 3.076 | 3.618 | 2.519 | 2.964 | 3.063 | 3.604 | 5.828 | 6.856 | 5.176 | 6.089 | ns |
| | Medium fast | 2.913 | 3.427 | 2.376 | 2.795 | 2.898 | 3.41 | 5.725 | 6.736 | 5.072 | 5.966 | ns |
| | Fast | 2.894 | 3.405 | 2.362 | 2.78 | 2.879 | 3.388 | 5.715 | 6.724 | 5.064 | 5.957 | ns |
| 16 mA | Slow | 3.366 | 3.96 | 2.751 | 3.237 | 3.348 | 3.939 | 6.226 | 7.324 | 5.576 | 6.56 | ns |
| | Medium | 3.03 | 3.565 | 2.47 | 2.906 | 3.017 | 3.55 | 5.981 | 7.036 | 5.282 | 6.214 | ns |
| | Medium fast | 2.87 | 3.377 | 2.328 | 2.739 | 2.854 | 3.358 | 5.895 | 6.935 | 5.18 | 6.094 | ns |
| | Fast | 2.853 | 3.357 | 2.314 | 2.723 | 2.837 | 3.338 | 5.889 | 6.929 | 5.177 | 6.09 | ns |

**Table 28 • LVCMOS 1.8 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.8 V (for MSIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 3.441 | 4.047 | 4.165 | 4.9 | 4.413 | 5.192 | 4.891 | 5.755 | 5.138 | 6.044 | ns |
| 4 mA | Slow | 3.218 | 3.786 | 3.642 | 4.284 | 3.941 | 4.636 | 5.665 | 6.665 | 5.568 | 6.551 | ns |
| 6 mA | Slow | 3.141 | 3.694 | 3.501 | 4.118 | 3.823 | 4.498 | 6.587 | 7.75 | 6.032 | 7.096 | ns |
| 8 mA | Slow | 3.165 | 3.723 | 3.319 | 3.904 | 3.654 | 4.298 | 6.898 | 8.115 | 6.216 | 7.313 | ns |
| 10 mA | Slow | 3.202 | 3.767 | 3.278 | 3.857 | 3.616 | 4.254 | 7.25 | 8.529 | 6.435 | 7.571 | ns |
| 12 mA | Slow | 3.277 | 3.855 | 3.175 | 3.736 | 3.519 | 4.139 | 7.392 | 8.697 | 6.538 | 7.692 | ns |
| **LVCMOS 1.8 V (for MSIOD I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 2.725 | 3.206 | 3.316 | 3.901 | 3.484 | 4.099 | 5.204 | 6.123 | 4.997 | 5.88 | ns |
| 4 mA | Slow | 2.242 | 2.638 | 2.777 | 3.267 | 2.947 | 3.466 | 5.729 | 6.74 | 5.448 | 6.41 | ns |
| 6 mA | Slow | 1.995 | 2.347 | 2.466 | 2.901 | 2.63 | 3.094 | 6.372 | 7.496 | 5.987 | 7.043 | ns |
| 8 mA | Slow | 2.001 | 2.354 | 2.44 | 2.87 | 2.6 | 3.058 | 6.633 | 7.804 | 6.193 | 7.286 | ns |
| 10 mA | Slow | 2.025 | 2.382 | 2.312 | 2.719 | 2.47 | 2.906 | 6.94 | 8.165 | 6.412 | 7.544 | ns |

## 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-11A.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 29 • LVCMOS 1.5 V DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 1.5 V Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.425 | 1.5 | 1.575 | V | |
| **LVCMOS 1.5 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High (for MSIOD and DDRIO I/O banks) | | 0.65 * VDDI | – | 1.575 | V | |
| VIH (DC) | DC input logic High (for MSIO I/O bank) | | 0.65 * VDDI | – | 3.45 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.35 * VDDI | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC | Input current Low | | – | – | 10 | µA | |
| **LVCMOS 1.5 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | VDDI * 0.75 | – | – | V | |
| VOL | DC output logic Low | | – | – | VDDI * 0.25 | V | |

**Table 30 • LVCMOS 1.5 V AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 1.5 V Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for DDRIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 235 | Mbps | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 160 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 220 | Mbps | |
| **LVCMOS 1.5 V AC Calibrated Impedance Option** | | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O bank) | | | 75, 60, 50, 40 | | Ohms | |
| **LVCMOS 1.5 V AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point | | – | 0.75 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

**Table 31 • LVCMOS 1.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA | Notes |
|---|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min. | Max. | | | |
| 2 mA | 2 mA | 2 mA | VDDI * 0.75 | VDDI * 0.25 | 2 | 2 | |
| 4 mA | 4 mA | 4 mA | VDDI * 0.75 | VDDI * 0.25 | 4 | 4 | |
| 6 mA | 6 mA | 6 mA | VDDI * 0.75 | VDDI * 0.25 | 6 | 6 | |
| 8 mA | N/A | 8 mA | VDDI * 0.75 | VDDI * 0.25 | 8 | 8 | |
| N/A | N/A | 10 mA | VDDI * 0.75 | VDDI * 0.25 | 10 | 10 | |
| N/A | N/A | 12 mA | VDDI * 0.75 | VDDI * 0.25 | 12 | 12 | |

*Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.*

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 1.425 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 32 • LVCMOS 1.5 V Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | $t_{PYS}$ | | Units |
|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | |
| LVCMOS 1.5 V (for DDRIO I/O bank) | None | 2.051 | 2.413 | 2.086 | 2.455 | ns |
| | 50 | 2.118 | 2.492 | 2.273 | 2.674 | ns |
| | 75 | 2.099 | 2.47 | 2.198 | 2.586 | ns |
| | 150 | 2.083 | 2.451 | 2.133 | 2.51 | ns |
| LVCMOS 1.5 V (for MSIO I/O bank) | None | 3.311 | 3.896 | 3.285 | 3.865 | ns |
| | 50 | 3.654 | 4.299 | 3.623 | 4.263 | ns |
| | 75 | 3.533 | 4.156 | 3.501 | 4.119 | ns |
| | 150 | 3.415 | 4.018 | 3.388 | 3.986 | ns |
| LVCMOS 1.5 V (for MSIOD I/O bank) | None | 2.959 | 3.481 | 2.93 | 3.447 | ns |
| | 50 | 3.298 | 3.88 | 3.268 | 3.845 | ns |
| | 75 | 3.162 | 3.719 | 3.128 | 3.68 | ns |
| | 150 | 3.053 | 3.592 | 3.021 | 3.554 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 33 • LVCMOS 1.5 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.5 V (for DDRIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 5.122 | 6.026 | 4.31 | 5.07 | 5.145 | 6.052 | 5.258 | 6.186 | 4.672 | 5.496 | ns |
| | Medium | 4.58 | 5.389 | 3.86 | 4.54 | 4.6 | 5.411 | 4.977 | 5.855 | 4.357 | 5.126 | ns |
| | Medium fast | 4.323 | 5.086 | 3.629 | 4.269 | 4.341 | 5.107 | 4.804 | 5.652 | 4.228 | 4.974 | ns |
| | Fast | 4.296 | 5.054 | 3.609 | 4.245 | 4.314 | 5.075 | 4.791 | 5.636 | 4.219 | 4.963 | ns |
| 4 mA | Slow | 4.449 | 5.235 | 3.707 | 4.361 | 4.443 | 5.227 | 6.058 | 7.127 | 5.458 | 6.421 | ns |
| | Medium | 3.961 | 4.66 | 3.264 | 3.839 | 3.954 | 4.651 | 5.778 | 6.797 | 5.116 | 6.018 | ns |
| | Medium fast | 3.729 | 4.387 | 3.043 | 3.579 | 3.72 | 4.376 | 5.63 | 6.624 | 4.981 | 5.86 | ns |
| | Fast | 3.704 | 4.358 | 3.027 | 3.56 | 3.695 | 4.347 | 5.624 | 6.617 | 4.973 | 5.851 | ns |
| 6 mA | Slow | 4.244 | 4.993 | 3.465 | 4.076 | 4.233 | 4.979 | 6.39 | 7.518 | 5.736 | 6.748 | ns |
| | Medium | 3.774 | 4.44 | 3.05 | 3.587 | 3.762 | 4.426 | 6.114 | 7.193 | 5.397 | 6.35 | ns |
| | Medium fast | 3.544 | 4.17 | 2.839 | 3.339 | 3.529 | 4.152 | 5.978 | 7.033 | 5.27 | 6.2 | ns |
| | Fast | 3.519 | 4.14 | 2.82 | 3.317 | 3.504 | 4.122 | 5.965 | 7.017 | 5.259 | 6.187 | ns |
| 8 mA | Slow | 4.099 | 4.823 | 3.311 | 3.894 | 4.087 | 4.807 | 6.584 | 7.746 | 5.854 | 6.888 | ns |
| | Medium | 3.656 | 4.301 | 2.927 | 3.443 | 3.642 | 4.284 | 6.311 | 7.425 | 5.553 | 6.533 | ns |
| | Medium fast | 3.437 | 4.044 | 2.731 | 3.213 | 3.42 | 4.023 | 6.182 | 7.273 | 5.435 | 6.394 | ns |
| | Fast | 3.41 | 4.012 | 2.715 | 3.193 | 3.393 | 3.991 | 6.178 | 7.269 | 5.425 | 6.383 | ns |
| 10 mA | Slow | 4.029 | 4.74 | 3.238 | 3.809 | 4.015 | 4.723 | 6.732 | 7.921 | 5.965 | 7.018 | ns |
| | Medium | 3.601 | 4.237 | 2.867 | 3.372 | 3.586 | 4.218 | 6.473 | 7.615 | 5.669 | 6.669 | ns |
| | Medium fast | 3.384 | 3.981 | 2.672 | 3.143 | 3.365 | 3.958 | 6.351 | 7.471 | 5.55 | 6.529 | ns |
| | Fast | 3.357 | 3.949 | 2.655 | 3.123 | 3.338 | 3.927 | 6.345 | 7.464 | 5.54 | 6.518 | ns |
| 12 mA | Slow | 3.974 | 4.675 | 3.196 | 3.759 | 3.958 | 4.656 | 6.842 | 8.049 | 6.068 | 7.139 | ns |
| | Medium | 3.55 | 4.176 | 2.827 | 3.326 | 3.534 | 4.157 | 6.584 | 7.746 | 5.751 | 6.766 | ns |
| | Medium fast | 3.345 | 3.935 | 2.638 | 3.103 | 3.325 | 3.911 | 6.488 | 7.633 | 5.641 | 6.637 | ns |
| | Fast | 3.316 | 3.902 | 2.621 | 3.083 | 3.297 | 3.878 | 6.486 | 7.63 | 5.626 | 6.619 | ns |
| **LVCMOS 1.5 V (for MSIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 4.423 | 5.203 | 5.397 | 6.35 | 5.686 | 6.69 | 5.609 | 6.599 | 5.561 | 6.542 | ns |
| 4 mA | Slow | 4.05 | 4.765 | 4.503 | 5.298 | 4.92 | 5.788 | 7.358 | 8.657 | 6.525 | 7.677 | ns |
| 6 mA | Slow | 4.081 | 4.801 | 4.259 | 5.012 | 4.699 | 5.528 | 7.659 | 9.011 | 6.709 | 7.893 | ns |
| 8 mA | Slow | 4.234 | 4.98 | 4.068 | 4.786 | 4.521 | 5.319 | 8.218 | 9.668 | 7.05 | 8.294 | ns |

**Table 33 • LVCMOS 1.5 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.5 V (for MSIOD I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 2.735 | 3.218 | 3.371 | 3.966 | 3.618 | 4.257 | 6.03 | 7.095 | 5.705 | 6.712 | ns |
| 4 mA | Slow | 2.426 | 2.854 | 2.992 | 3.521 | 3.221 | 3.79 | 6.738 | 7.927 | 6.298 | 7.41 | ns |
| 6 mA | Slow | 2.433 | 2.862 | 2.81 | 3.306 | 3.031 | 3.566 | 7.123 | 8.38 | 6.596 | 7.76 | ns |

## 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-12A.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 34 • LVCMOS 1.2 V DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 1.2 V Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.140 | 1.2 | 1.26 | V | |
| **LVCMOS 1.2 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High for (MSIOD and DDRIO I/O bank) | | 0.65 * VDDI | – | 1.26 | V | |
| VIH (DC) | DC input logic High (for MSIO I/O bank) | | 0.65 * VDDI | – | 3.45 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.35 * VDDI | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **LVCMOS 1.2 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | VDDI * 0.75 | – | – | V | |
| VOL | DC output logic Low | | – | – | VDDI * 0.25 | V | |

**Table 35 • LVCMOS 1.2 V AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 1.2 V Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for DDRIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 200 | Mbps | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 120 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 160 | Mbps | |
| **LVCMOS 1.2 V AC Calibrated Impedance Option** | | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O bank) | | | 75, 60, 50, 40 | | Ohms | |
| **LVCMOS 1.2 V AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point | | – | 0.6 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

**Table 36 • LVCMOS 1.2 V Transmitter Drive Strength Specifications**

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA | Notes |
|---|---|---|---|---|---|---|---|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank | Min. | Max. | | | |
| 2 mA | 2 mA | 2 mA | VDDI * 0.75 | VDDI * 0.25 | 2 | 2 | |
| 4 mA | 4 mA | 4 mA | VDDI * 0.75 | VDDI * 0.25 | 4 | 4 | |
| N/A | N/A | 6 mA | VDDI * 0.75 | VDDI * 0.25 | 6 | 6 | |

*Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.*

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 1.14 V

### AC Switching Characteristics for Receiver (Input Buffers))

**Table 37 • LVCMOS 1.2 V Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | $t_{PYS}$ | | Units |
|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.2 V (for DDRIO I/O bank)** | None | 2.448 | 2.88 | 2.466 | 2.901 | ns |
| | 50 | 2.578 | 3.033 | 2.823 | 3.321 | ns |
| | 75 | 2.49 | 2.929 | 2.68 | 3.153 | ns |
| | 150 | 2.419 | 2.846 | 2.56 | 3.012 | ns |
| **LVCMOS 1.2 V (for MSIO I/O bank)** | None | 4.714 | 5.545 | 4.675 | 5.5 | ns |
| | 50 | 6.668 | 7.845 | 6.579 | 7.74 | ns |
| | 75 | 5.832 | 6.862 | 5.76 | 6.777 | ns |
| | 150 | 5.162 | 6.073 | 5.111 | 6.014 | ns |
| **LVCMOS 1.2 V (for MSIOD I/O bank)** | None | 4.154 | 4.887 | 4.114 | 4.84 | ns |
| | 50 | 6.918 | 8.139 | 6.806 | 8.008 | ns |
| | 75 | 5.613 | 6.603 | 5.533 | 6.509 | ns |
| | 150 | 4.716 | 5.549 | 4.657 | 5.479 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 38 • LVCMOS 1.2 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.2 V (for DDRIO I/O bank)** | | | | | | | | | | | | |
| **2 mA** | Slow | 6.713 | 7.897 | 5.362 | 6.308 | 6.723 | 7.909 | 7.233 | 8.51 | 6.375 | 7.499 | ns |
| | Medium | 5.912 | 6.955 | 4.616 | 5.43 | 5.915 | 6.959 | 6.887 | 8.102 | 6.009 | 7.069 | ns |
| | Medium fast | 5.5 | 6.469 | 4.231 | 4.978 | 5.5 | 6.471 | 6.672 | 7.849 | 5.835 | 6.865 | ns |
| | Fast | 5.462 | 6.426 | 4.194 | 4.935 | 5.463 | 6.427 | 6.646 | 7.819 | 5.828 | 6.857 | ns |
| **4 mA** | Slow | 6.109 | 7.186 | 4.708 | 5.539 | 6.098 | 7.174 | 8.005 | 9.418 | 7.033 | 8.274 | ns |
| | Medium | 5.355 | 6.299 | 4.034 | 4.746 | 5.338 | 6.28 | 7.637 | 8.985 | 6.672 | 7.849 | ns |
| | Medium fast | 4.953 | 5.826 | 3.685 | 4.336 | 4.932 | 5.802 | 7.44 | 8.752 | 6.499 | 7.646 | ns |
| | Fast | 4.911 | 5.777 | 3.658 | 4.303 | 4.89 | 5.754 | 7.427 | 8.737 | 6.488 | 7.632 | ns |
| **6 mA** | Slow | 5.89 | 6.929 | 4.506 | 5.301 | 5.874 | 6.911 | 8.337 | 9.808 | 7.315 | 8.605 | ns |
| | Medium | 5.176 | 6.089 | 3.862 | 4.543 | 5.155 | 6.065 | 7.986 | 9.394 | 6.943 | 8.168 | ns |
| | Medium fast | 4.792 | 5.637 | 3.523 | 4.145 | 4.765 | 5.606 | 7.808 | 9.186 | 6.775 | 7.97 | ns |
| | Fast | 4.754 | 5.593 | 3.486 | 4.101 | 4.728 | 5.563 | 7.777 | 9.149 | 6.769 | 7.963 | ns |

**Table 38 • LVCMOS 1.2 V Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)**

| Output Drive Selection | Slew Control | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LVCMOS 1.2 V (for MSIO I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 6.746 | 7.937 | 7.458 | 8.774 | 8.172 | 9.614 | 9.867 | 11.608 | 8.393 | 9.874 | ns |
| 4 mA | Slow | 7.068 | 8.315 | 6.678 | 7.857 | 7.474 | 8.793 | 10.986 | 12.924 | 9.043 | 10.638 | ns |
| **LVCMOS 1.2 V (for MSIOD I/O bank)** | | | | | | | | | | | | |
| 2 mA | Slow | 3.883 | 4.568 | 4.868 | 5.726 | 5.329 | 6.269 | 7.994 | 9.404 | 7.527 | 8.855 | ns |
| 4 mA | Slow | 3.774 | 4.44 | 4.188 | 4.926 | 4.613 | 5.426 | 8.972 | 10.555 | 8.315 | 9.782 | ns |

## 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 39 • PCI/PCI-X DC Voltage Specification – Applicable to MSIO Bank ONLY**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **PCI/PCIX Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V | |
| **PCI/PCIX DC Input Voltage Specification** | | | | | | | |
| VI | DC input voltage | | 0 | – | 3.45 | V | |
| IIH(DC) | Input current High | | – | – | 10 | µA | |
| IIL(DC) | Input current Low | | – | – | 10 | µA | |
| **PCI/PCIX DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | Per PCI Specification | | | V | |
| VOL | DC output logic Low | | Per PCI Specification | | | V | |

**Table 40 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank ONLY)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **PCI/PCI-X Minimum and Maximum AC Switching Speed (Applicable to MSIO Bank ONLY)** | | | | | | | |
| Fmax | Maximum data rate (MSIO I/O bank) | AC Loading: per JEDEC specifications | – | – | 630 | Mbps | |
| **PCI/PCI-X AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path (falling edge) | | – | 0.615 * VDDI | – | V | |
| Vtrip | Measuring/trip point for data path (rising edge) | | – | 0.285 * VDDI | – | V | |
| Rtt_test | Resistance for data test path | | – | 25 | – | Ohms | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |

### AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 3.0 V

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 41 • AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | $t_{PYS}$ | | Units |
|---|---|---|---|---|---|---|
| | | –1 | Std. | –1 | Std. | |
| **PCI/PCIX (for MSIO I/O bank)** | None | 2.229 | 2.623 | 2.238 | 2.633 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 42 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **PCI/PCIX (for MSIO I/O bank)** | | | | | | | | | | | |
| | 2.146 | 2.525 | 2.043 | 2.404 | 2.084 | 2.452 | 6.095 | 7.171 | 5.558 | 6.539 | ns |

# Memory Interface and Voltage Referenced I/O Standards

## High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). SmartFusion2 devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

### Minimum and Maximum DC/AC Input and Output Levels Specification

***Table 43 •*** **HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **HSTL Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.425 | 1.5 | 1.575 | V | |
| VTT | Termination voltage | | 0.698 | 0.750 | 0.803 | V | |
| VREF | Input reference voltage | | 0.698 | 0.750 | 0.803 | V | |
| **HSTL DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High | | VREF + 0.1 | – | 1.575 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | VREF – 0.1 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **HSTL DC Output Voltage Specification** | | | | | | | |
| **HSTL Class I** | | | | | | | |
| VOH | DC output logic High | | VDDI – 0.4 | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.4 | V | |
| IOH at VOH | Output minimum source DC current | | –8.0 | – | – | mA | 1 |
| IOL at VOL | Output minimum sink current | | 8.0 | – | – | mA | 1 |
| **HSTL Class II** | | | | | | | |
| VOH | DC output logic High | | VDDI – 0.4 | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.4 | V | |
| IOH at VOH | Output minimum source DC current | | –16.0 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | 16.0 | – | – | mA | |
| **HSTL DC Differential Voltage Specifications** | | | | | | | |
| VID | DC input differential voltage | | 0.2 | – | – | V | |

*Note: 1. MSIOD I/O bank HSTL Class I does not meet standard JEDEC test point. Use provided lower current values as specified.*

**Table 44 • HSTL AC Specifications (Applicable to DDRIO Bank ONLY)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **HSTL AC Differential Voltage Specifications** | | | | | | | |
| VDIFF | AC input differential voltage | | 0.4 | – | – | V | |
| Vx | AC differential cross point voltage | | 0.68 | – | 0.9 | V | |
| **HSTL Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate | AC loading: per JEDEC specifications | – | – | 400 | Mbps | |
| **HSTL Impedance Specification** | | | | | | | |
| Rref | Supported output driver calibrated impedance (for DDRIO I/O bank) | Reference resistance = 191 Ohms | – | 25.5, 47.8 | – | Ohms | |
| RTT | Effective impedance value (ODT for DDRIO I/O bank only) | Reference resistance = 191 Ohms | – | 47.8 | – | Ohms | |
| **HSTL AC Test Parameters Specification** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | | 0.75 | | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Rtt_test | Reference resistance for data test path for HSTL15 Class I ($t_{DP}$) | | | 50 | | Ohms | |
| Rtt_test | Reference resistance for data test path for HSTL15 Class II ($t_{DP}$) | | – | 25 | – | Ohms | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 45 • HSTL Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| **HSTL (for DDRIO I/O bank)** | | | | |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 47.8 | 1.614 | 1.898 | ns |
| True differential | None | 1.622 | 1.909 | ns |
| | 47.8 | 1.628 | 1.916 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 46 • HSTL Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **HSTL Class I** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.6 | 3.059 | 2.514 | 2.958 | 2.514 | 2.958 | 2.431 | 2.86 | 2.431 | 2.86 | ns |
| Differential | 2.621 | 3.083 | 2.648 | 3.115 | 2.647 | 3.113 | 2.925 | 3.442 | 2.923 | 3.44 | ns |
| **HSTL Class II** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.511 | 2.954 | 2.488 | 2.927 | 2.49 | 2.93 | 2.409 | 2.833 | 2.411 | 2.836 | ns |
| Differential | 2.528 | 2.974 | 2.552 | 3.003 | 2.551 | 3.001 | 2.897 | 3.409 | 2.896 | 3.408 | ns |

## Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in SmartFusion2 devices. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. SmartFusion2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

## Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in SmartFusion2 devices and also comply with reduced and full drive of double data rate (DDR) standards. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### Minimum and Maximum DC/AC Input and Output Levels Specification

***Table 47 •*** **DDR1/SSTL2 DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | |
| VTT | Termination voltage | | 1.164 | 1.250 | 1.339 | V | |
| VREF | Input reference voltage | | 1.164 | 1.250 | 1.339 | V | |
| **DDR/SSTL2 DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High | | VREF + 0.15 | – | 2.625 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | VREF – 0.15 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Lo | | – | – | 10 | µA | |
| **DDR/SSTL2 DC Output Voltage Specification** | | | | | | | |
| **SSTL2 Class I (DDR Reduced Drive)** | | | | | | | |
| VOH | DC output logic High | | VTT + 0.608 | – | – | V | |
| VOL | DC output logic Low | | – | – | VTT – 0.608 | V | |
| IOH at VOH | Output minimum source DC current | | 8.1 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | –8.1 | – | – | mA | |
| **SSTL2 Class II (DDR Full Drive) (Applicable to MSIO and DDRIO I/O Banks ONLY)** | | | | | | | |
| VOH | DC output logic High | | VTT + 0.81 | – | – | V | |
| VOL | DC output logic Low | | – | – | VTT – 0.81 | V | |
| IOH at VOH | Output minimum source DC current | | 16.2 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | –16.2 | – | – | mA | |
| **SSTL2 DC Differential Voltage Specification** | | | | | | | |
| VID (DC) | DC input differential voltage | | 0.3 | – | – | V | |

***Table 48 •*** **DDR1/SSTL2 AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **SSTL2 AC Differential Voltage Specification** | | | | | | | |
| VDIFF | AC input differential voltage | | 0.7 | – | – | V | |
| Vx | AC differential cross point voltage | | 0.5 * VDDI – 0.2 | – | 0.5 * VDDI + 0.2 | V | |
| **SSTL2 Minimum and Maximum AC Switching Speeds** | | | | | | | |
| Fmax | Maximum data rate (for DDRIO I/O bank) | AC loading: per JEDEC specifications | – | – | 400 | Mbps | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 17 pF load | – | – | 575 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 3 pF / 50 Ohm load | – | – | 700 | Mbps | |
| | | AC loading: 17 pF load | – | – | 510 | Mbps | |
| **SSTL2 Impedance Specifications** | | | | | | | |
| | Supported output driver calibrated impedance (for DDRIO I/O bank) | Reference resistor = 150 Ohms | – | 20, 42 | – | Ohms | |
| **SSTL2 AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 1.25 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2 k | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Rs | Series resistance for data test path ($t_{DP}$) | | – | 25 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for SSTL2 Class I ($t_{DP}$) | | – | 50 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for SSTL2 Class II ($t_{DP}$) | | – | 25 | – | Ohms | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 49 • DDR1/SSTL2 Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| **SSTL2 (for DDRIO I/O bank)** | | | | |
| Pseudo differential | None | 1.549 | 1.821 | ns |
| True differential | None | 1.589 | 1.87 | ns |
| **SSTL2 (for MSIO I/O bank)** | | | | |
| Pseudo differential | None | 2.798 | 3.293 | ns |
| True differential | None | 2.733 | 3.215 | ns |
| **SSTL2 (for MSIOD I/O bank)** | | | | |
| Pseudo differential | None | 2.476 | 2.913 | ns |
| True differential | None | 2.475 | 2.911 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 50 • DDR1/SSTL2 Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | STD | –1 | STD | –1 | STD | –1 | STD | –1 | STD | |
| **SSTL2 Class I** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.26 | 2.66 | 1.99 | 2.341 | 1.985 | 2.335 | 2.135 | 2.512 | 2.13 | 2.505 | ns |
| Differential | 2.26 | 2.658 | 2.202 | 2.591 | 2.201 | 2.589 | 2.393 | 2.815 | 2.392 | 2.814 | ns |
| **For MSIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.055 | 2.417 | 2.037 | 2.396 | 2.03 | 2.388 | 2.068 | 2.433 | 2.061 | 2.425 | ns |
| Differential | 2.192 | 2.58 | 2.434 | 2.864 | 2.425 | 2.852 | 2.164 | 2.545 | 2.156 | 2.536 | ns |
| **For MSIOD I/O Bank** | | | | | | | | | | | |
| Single-ended | 1.512 | 1.779 | 1.462 | 1.72 | 1.462 | 1.72 | 1.676 | 1.972 | 1.676 | 1.971 | ns |
| Differential | 1.676 | 1.971 | 1.774 | 2.087 | 1.766 | 2.077 | 1.854 | 2.181 | 1.845 | 2.171 | ns |
| **SSTL2 Class II** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.122 | 2.497 | 1.906 | 2.243 | 1.902 | 2.237 | 2.061 | 2.424 | 2.056 | 2.418 | ns |
| Differential | 2.127 | 2.501 | 2.042 | 2.402 | 2.043 | 2.403 | 2.363 | 2.78 | 2.365 | 2.781 | ns |
| **For MSIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.29 | 2.693 | 1.988 | 2.338 | 1.978 | 2.326 | 1.989 | 2.34 | 1.979 | 2.328 | ns |
| Differential | 2.418 | 2.846 | 2.304 | 2.711 | 2.297 | 2.702 | 2.131 | 2.506 | 2.124 | 2.499 | ns |

## Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double date rate (DDR2) standard. SmartFusion2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 51 • SSTL18 Minimum and Maximum DC Input and Output Levels (Applicable to DDRIO Bank ONLY)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.71 | 1.8 | 1.89 | V | |
| VTT | Termination voltage | | 0.838 | 0.900 | 0.964 | V | |
| VREF | Input reference voltage | | 0.838 | 0.900 | 0.964 | V | |
| **SSTL18 DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High | | Vref + 0.125 | - | 1.89 | V | |
| VIL (DC) | DC input logic Low | | -0.3 | - | Vref - 0.125 | V | |
| IIH (DC) | Input current High | | - | - | 10 | uA | |
| IIL (DC) | Input current Low | | - | - | 10 | uA | |
| **SSTL18 DC Output Voltage Specification** | | | | | | | |
| **SSTL18 Class I (DDR2 Reduced Drive)** | | | | | | | |
| VOH | DC output logic High | | VTT + 0.603 | - | - | V | |
| VOL | DC output logic Low | | - | - | VTT - 0.603 | V | |
| IOH at VOH | Output minimum source DC current | | 6.5 | - | - | mA | |
| IOL at VOL | Output minimum sink current | | -6.5 | - | - | mA | |
| **STL18 Class II (DDR2 Full Drive)** | | | | | | | 1 |
| VOH | DC output logic High | | VTT + 0.603 | - | - | V | |
| VOL | DC output logic Low | | - | - | VTT - 0.603 | V | |
| IOH at VOH | Output minimum source DC current | | 13.4 | - | - | mA | |
| IOL at VOL | Output minimum sink current | | -13.4 | - | - | mA | |
| **SSTL18 DC Differential Voltage Specification** | | | | | | | |
| VID | DC input differential voltage | | 0.3 | – | – | V | |

*Note: 1: To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.*

**Table 52 • SSTL18 AC Specifications (Applicable to DDRIO Bank ONLY)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **SSTL18 AC Differential Voltage Specification** | | | | | | | |
| VDIFF | AC input differential voltage | | 0.7 | | | V | |
| Vx | AC differential cross point voltage | | 0.5 * VDDI – 0.175 | – | 0.5 * VDDI + 0.175 | V | |
| **SSTL18 Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate | AC loading: per JEDEC specification | – | – | 667 | Mbps | |
| **SSTL18 Impedance Specifications** | | | | | | | |
| Rref | Supported output driver calibrated impedance (for DDRIO I/O bank) | Reference resistor = 150 Ohms | – | 20, 42 | | Ohms | |
| RTT | Effective impedance value (ODT) | Reference resistor = 150 Ohms | – | 50, 75, 150 | | Ohms | |
| **AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.9 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2 k | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Rs | Series resistance for data test path ($t_{DP}$) | | – | 25 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for SSTL18 Class I ($t_{DP}$) | | – | 50 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for SSTL18 Class II ($t_{DP}$) | | – | 25 | – | Ohms | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 1.71 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 53 • DDR2/SSTL18 Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | STD | |
| **SSTL18 (for DDRIO I/O bank)** | | | | |
| Pseudo differential | None | 1.567 | 1.844 | ns |
| | 50 | 1.573 | 1.851 | ns |
| | 75 | 1.571 | 1.849 | ns |
| | 150 | 1.569 | 1.846 | ns |
| True differential | None | 1.588 | 1.869 | ns |
| | 50 | 1.593 | 1.875 | ns |
| | 75 | 1.589 | 1.871 | ns |
| | 150 | 1.585 | 1.866 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 54 • DDR2/SSTL18 Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | STD | –1 | STD | –1 | STD | –1 | STD | –1 | STD | |
| **SSTL18 Class I** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.413 | 2.84 | 2.797 | 3.29 | 2.797 | 3.29 | 2.282 | 2.685 | 2.282 | 2.685 | ns |
| **SSTL18 Class II** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.315 | 2.724 | 2.698 | 3.173 | 2.698 | 3.173 | 2.242 | 2.639 | 2.242 | 2.639 | ns |

## Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double data rate (DDR3) standard. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 55 • SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.425 | 1.5 | 1.575 | V | |
| VTT | Termination voltage | | 0.698 | 0.750 | 0.803 | V | |
| VREF | Input reference voltage | | 0.698 | 0.750 | 0.803 | V | |
| **SSTL15 DC Input Voltage Specification** | | | | | | | |
| VIH(DC) | DC input logic High | | VREF + 0.1 | – | 1.575 | V | |
| VIL(DC) | DC input logic Low | | –0.3 | – | VREF – 0.1 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **SSTL15 DC Output Voltage Specification** | | | | | | | |
| **DDR3/SSTL15 Class I (DDR3 Reduced Drive)** | | | | | | | |
| VOH | DC output logic High | | 0.8 * VDDI | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.2 * VDDI | V | |
| IOH at VOH | Output minimum source DC current | | 6.5 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | –6.5 | – | – | mA | |
| **SSTL15 Class II (DDR3 Full Drive)** | | | | | | | 1 |
| VOH | DC output logic High | | 0.8 * VDDI | – | – | V | |
| VOL | DC output logic Low | | – | - | 0.2 * VDDI | V | |
| IOH at VOH | Output minimum source DC current | | 7.6 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | –7.6 | – | – | mA | |
| **SSTL15 Differential Voltage Specification** | | | | | | | |
| VID (DC) | DC input differential voltage | | 0.2 | – | – | V | |

*Note: 1. To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.*

**Table 56 • SSTL15 AC Specifications (for DDRIO I/O Banks Only)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **SSTL15 Differential Voltage Specification** | | | | | | | |
| VDIFF | AC input differential voltage | | 0.7 | – | – | V | |
| Vx | AC differential cross point voltage | | 0.5 * VDDI – 0.150 | – | 0.5 * VDDI + 0.150 | V | |
| **SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Banks only)** | | | | | | | |
| Fmax | Maximum data rate (for DDRIO I/O bank) | AC loading: per JEDEC specifications | | | 667 | Mbps | |
| **SSTL15 AC Calibrated Impedance Option** | | | | | | | |
| Rref | Supported output driver calibrated impedance | Reference resistor = 240 Ohms | | 34, 40 | | Ohms | |
| RTT | Effective impedance value (ODT) | Reference resistor = 240 Ohms | | 20, 30, 40, 60, 120 | | Ohms | |
| **SSTL15 AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.75 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Rs | Series resistance for data test path ($t_{DP}$) | | – | 25 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for SSTL15 Class I ($t_{DP}$) | | – | 50 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for SSTL15 Class II ($t_{DP}$) | | – | 25 | – | Ohms | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 1.425 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 57 • SSTL15 Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| **DDR3/SSTL15 (for DDRIO I/O bank)** | | | | |
| Pseudo differential | None | 1.605 | 1.888 | ns |
| | 20 | 1.616 | 1.901 | ns |
| | 30 | 1.613 | 1.897 | ns |
| | 40 | 1.611 | 1.895 | ns |
| | 60 | 1.609 | 1.893 | ns |
| | 120 | 1.607 | 1.89 | ns |
| True differential | None | 1.623 | 1.91 | ns |
| | 20 | 1.637 | 1.926 | ns |
| | 30 | 1.63 | 1.918 | ns |
| | 40 | 1.626 | 1.914 | ns |
| | 60 | 1.622 | 1.91 | ns |
| | 120 | 1.619 | 1.905 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 58 • DDR3/SSTL15 Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | STD | –1 | STD | –1 | STD | –1 | STD | –1 | STD | |
| **DDR3 Reduced Drive/SSTL15 Class I** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.533 | 2.98 | 2.522 | 2.967 | 2.523 | 2.968 | 2.427 | 2.855 | 2.428 | 2.856 | ns |
| Differential | 2.555 | 3.005 | 3.073 | 3.615 | 3.073 | 3.615 | 2.416 | 2.843 | 2.416 | 2.843 | ns |
| **DDR3 Full DriveSSTL15 Class II** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.53 | 2.977 | 2.514 | 2.958 | 2.516 | 2.96 | 2.422 | 2.849 | 2.425 | 2.852 | ns |
| Differential | 2.552 | 3.002 | 2.591 | 3.048 | 2.59 | 3.047 | 2.882 | 3.391 | 2.881 | 3.39 | ns |

## Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in SmartFusion2 FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 59 • LPDDR DC Voltage Specification (for DDRIO I/O banks only)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LPDDR Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.71 | 1.8 | 1.89 | V | |
| VTT | Termination voltage | | 0.838 | 0.900 | 0.964 | V | |
| VREF | Input reference voltage | | 0.838 | 0.900 | 0.964 | V | |
| **LPDDR DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High | | 0.7 * VDDI | – | 1.89 | V | |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.3 * VDDI | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **LPDDR DC Output Voltage Specification** | | | | | | | |
| **LPDDR reduced drive** | | | | | | | |
| VOH | DC output logic High | | 0.9 * VDDI | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.1 * VDDI | V | |
| IOH at VOH | Output minimum source DC current | | 0.1 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | –0.1 | – | – | mA | |
| **LPDDR full drive** | | | | | | | 1 |
| VOH | DC output logic High | | 0.9 * VDDI | – | – | V | |
| VOL | DC output logic Low | | – | – | 0.1 * VDDI | V | |
| IOH at VOH | Output minimum source DC current | | 0.1 | – | – | mA | |
| IOL at VOL | Output minimum sink current | | –0.1 | – | – | mA | |
| **LPDDR Differential Voltage Specification** | | | | | | | |
| VID (DC) | DC input differential voltage | | 0.4 * VDDI | – | – | V | |

*Note: 1. To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.*

**Table 60 • LPDDR AC Specifications (for DDRIO I/O banks only)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LPDDR AC Differential Voltage Specification** | | | | | | | |
| VDIFF | AC input differential voltage | | 0.6 * VDDI | | | V | |
| Vx | AC differential cross point voltage | | 0.4 * VDDI | – | 0.6 * VDDI | V | |
| **LPDDR Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate | AC loading: per JEDEC specifications | | | 400 | Mbps | |
| **LPDDR AC Calibrated Impedance Option** | | | | | | | |
| Rref | Supported output driver calibrated impedance | Reference resistor = 150 Ohms | | 20, 42 | | Ohms | |
| Rtt | Effective impedance value – ODT | Reference resistor = 150 Ohms | | 50, 75, 150 | | Ohms | |
| **LPDDR AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.9 | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |
| Rs | Series resistance for data test path ($t_{DP}$) | | – | 25 | – | Ohms | |
| Rtt_test | Reference resistance for data test path for LPDDR ($t_{DP}$) | | – | 50 | – | Ohms | |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | Ohms | |

## AC Switching Characteristics

**Table 61 • LPDDR Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| **LPDDR (for DDRIO I/O Bank)** | | | | |
| Pseudo differential | None | 1.568 | 1.845 | ns |
| | 50 | 1.574 | 1.852 | ns |
| | 75 | 1.572 | 1.85 | ns |
| | 150 | 1.57 | 1.847 | ns |
| True differential | None | 1.588 | 1.869 | ns |
| | 50 | 1.593 | 1.875 | ns |
| | 75 | 1.589 | 1.871 | ns |
| | 150 | 1.585 | 1.866 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 62 • LPDDR Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **LPDDR Reduced Drive** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.383 | 2.804 | 2.23 | 2.623 | 2.229 | 2.622 | 2.202 | 2.591 | 2.201 | 2.59 | ns |
| Differential | 2.396 | 2.819 | 2.764 | 3.252 | 2.764 | 3.252 | 2.255 | 2.653 | 2.255 | 2.653 | ns |
| **LPDDR Full Drive** | | | | | | | | | | | |
| **For DDRIO I/O Bank** | | | | | | | | | | | |
| Single-ended | 2.281 | 2.683 | 2.196 | 2.584 | 2.195 | 2.583 | 2.171 | 2.555 | 2.17 | 2.554 | ns |
| Differential | 2.298 | 2.703 | 2.288 | 2.692 | 2.288 | 2.692 | 2.593 | 3.051 | 2.593 | 3.051 | ns |

## Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

### *LVDS*

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

#### *Minimum and Maximum Input and Output Levels*

***Table 63 •*** **LVDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVDS Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | 2.5 V range | 2.375 | 2.5 | 2.625 | V | |
| VDDI | Supply voltage | 3.3 V range | 3.15 | 3.3 | 3.45 | V | |
| **LVDS DC Input Voltage Specification** | | | | | | | |
| VI | DC Input voltage | 2.5 V range | 0 | – | 2.925 | V | |
| VI | DC input voltage | 3.3 V range | 0 | – | 3.45 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **LVDS DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V | |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V | |
| **LVDS Differential Voltage Specification** | | | | | | | |
| VOD | Differential output voltage swing | | 250 | 350 | 450 | mV | |
| VOCM | Output common mode voltage | | 1.125 | 1.25 | 1.375 | V | |
| VICM | Input common mode voltage | | 0.05 | 1.25 | 2.35 | V | |
| VID | Input differential voltage | | 100 | 350 | 600 | mV | |

***Table 64 •*** **LVDS AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVDS Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 12 pF / 100 Ohm differential load | – | – | 535 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 10 pF / 100 Ohm differential load | – | – | 620 | Mbps | |
| | | AC loading: 2 pF / 100 Ohm differential load | | | 700 | Mbps | |
| **LVDS Impedance Specification** | | | | | | | |
| Rt | Termination resistance | | – | 100 | – | Ohms | |
| **LVDS AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | Cross point | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |

### LVDS25 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 65 • LVDS25 Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| LVDS (for MSIO I/O bank) | None | 2.774 | 3.263 | ns |
| | 100 | 2.775 | 3.264 | ns |
| LVDS (for MSIOD I/O bank) | None | 2.554 | 3.004 | ns |
| | 100 | 2.549 | 2.999 | ns |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 66 • LVDS25 Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| LVDS (for MSIO I/O bank) | 2.136 | 2.513 | 2.416 | 2.842 | 2.402 | 2.825 | 2.144 | 2.522 | 2.155 | 2.536 | ns |
| LVDS (for MSIOD I/O bank) | | | | | | | | | | | |
| No pre-emphasis | 1.61 | 1.893 | 1.749 | 2.058 | 1.735 | 2.041 | 1.897 | 2.231 | 1.866 | 2.195 | ns |
| Min. pre-emphasis | 1.527 | 1.796 | 1.757 | 2.067 | 1.744 | 2.052 | 1.905 | 2.241 | 1.876 | 2.207 | ns |
| Med. pre-emphasis | 1.496 | 1.76 | 1.765 | 2.077 | 1.751 | 2.06 | 1.914 | 2.252 | 1.884 | 2.216 | ns |

### LVDS33 AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 67 • LVDS33 Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| LVDS33 (for MSIO I/O bank) | None | 2.572 | 3.025 | ns |
| | 100 | 2.569 | 3.023 | ns |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 68 • LVDS33 Transmitter Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| LVDS33 (for MSIO I/O bank) | 1.942 | 2.284 | 1.98 | 2.33 | 1.97 | 2.318 | 1.953 | 2.298 | 1.96 | 2.307 | ns |

## B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

### Minimum and Maximum DC/AC Input and Output Levels Specification

**Table 69 • B-LVDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Bus LVDS Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | |
| **Bus LVDS DC Input Voltage Specification** | | | | | | | |
| VI | DC input voltage | | 0 | – | 2.925 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **Bus LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)** | | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V | |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V | |
| **Bus LVDS Differential Voltage Specification** | | | | | | | |
| VOD | Differential output voltage swing (for MSIO I/O bank ONLY) | | 65 | – | 460 | mV | |
| VOCM | Output common mode voltage (for MSIO I/O bank ONLY) | | 1.1 | – | 1.5 | V | |
| VICM | Input common mode voltage | | 0.05 | – | 2.4 | V | |
| VID | Input differential voltage | | 100 | – | VDDI | mV | |

**Table 70 • B-LVDS AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Bus LVDS Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 2 pF / 100 Ohm differential load | – | – | 500 | Mbps | |
| **Bus LVDS Impedance Specifications** | | | | | | | |
| Rt | Termination resistance | | – | 27 | – | Ohms | |
| **Bus LVDS AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | Cross point | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 71 • AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| Bus-LVDS (for MSIO I/O Bank) | None | 2.738 | 3.221 | ns |
| | 100 | 2.735 | 3.218 | ns |
| Bus-LVDS (for MSIOD I/O Bank) | None | 2.495 | 2.934 | ns |
| | 100 | 2.495 | 2.935 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 72 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| Bus-LVDS (for MSIO I/O Bank) | 2.258 | 2.656 | 2.343 | 2.756 | 2.329 | 2.74 | 2.12 | 2.494 | 2.123 | 2.497 | ns |

## M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

### Minimum and Maximum Input and Output Levels

**Table 73 • M-LVDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **M-LVDS Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | 1 |
| **M-LVDS DC Input Voltage Specification** | | | | | | | |
| VI | DC input voltage | | 0 | – | 2.925 | V | |
| IIH (DC) | Input current High | | – | – | 10 | µA | |
| IIL (DC) | Input current Low | | – | – | 10 | µA | |
| **M-LVDS DC Output Voltage Specification (for MSIO I/O bank ONLY)** | | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V | |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V | |
| **M-LVDS Differential Voltage Specification** | | | | | | | |
| VOD | Differential output voltage Swing (for MSIO I/O bank ONLY) | | 300 | – | 650 | mV | |
| VOCM | Output common mode voltage (for MSIO I/O bank ONLY) | | 0.3 | – | 2.1 | V | |
| VICM | Input common mode voltage | | 0.3 | – | 1.2 | V | |
| VID | Input differential voltage | | 50 | – | 2400 | mV | |

*Note: 1. Only M-LVDS Type I is supported.*

**Table 74 • M-LVDS AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **M-LVDS Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 2 pF / 100 Ohm differential load | – | – | 500 | Mbps | |
| **M-LVDS Impedance Specification** | | | | | | | |
| Rt | Termination resistance | | – | 50 | – | Ohms | |
| **M-LVDS AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | Cross point | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 75 • AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| M-LVDS (for MSIO I/O bank) | None | 2.738 | 3.221 | ns |
| | 100 | 2.735 | 3.218 | ns |
| M-LVDS (for MSIOD I/O bank) | None | 2.495 | 2.934 | ns |
| | 100 | 2.495 | 2.935 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 76 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| M-LVDS (for MSIO I/O bank) | 2.258 | 2.656 | 2.348 | 2.762 | 2.334 | 2.746 | 2.123 | 2.497 | 2.125 | 2.5 | ns |

## Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

### Mini-LVDS Minimum and Maximum Input and Output Levels

**Table 77 • Mini-LVDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | |
| **Mini-LVDS DC Input Voltage Specification** | | | | | | | |
| VI | DC Input voltage | | 0 | – | 2.925 | V | |
| **Mini-LVDS DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V | |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V | |
| **Mini-LVDS Differential Voltage Specification** | | | | | | | |
| VOD | Differential output voltage swing | | 300 | – | 600 | mV | |
| VOCM | Output common mode voltage | | 1 | – | 1.4 | V | |
| VICM | Input common mode voltage | | 0.3 | – | 1.2 | V | |
| VID | Input differential voltage | | 100 | – | 600 | mV | |

**Table 78 • Mini-LVDS AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Mini-LVDS Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 2 pF / 100 Ohm differential load | – | – | 520 | Mbps | |
| Fmax | Maximum data rate (for MSIOD I/O bank) | AC loading: 2 pF / 100 Ohm differential load | – | – | 700 | Mbps | |
| **Mini-LVDS Impedance Specification** | | | | | | | |
| Rt | Termination resistance | | 50 | 100 | – | Ohms | |
| **Mini-LVDS AC Test Parameters Specifications** | | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | Cross point | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 79 • AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| Mini-LVDS (for MSIO I/O bank) | None | 2.855 | 3.359 | ns |
| | 100 | 2.85 | 3.353 | ns |
| Mini-LVDS (for MSIOD I/O bank) | None | 2.602 | 3.061 | ns |
| | 100 | 2.597 | 3.055 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 80 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **Mini-LVDS (for MSIO I/O bank)** | 2.097 | 2.467 | 2.308 | 2.715 | 2.296 | 2.701 | 1.964 | 2.31 | 1.949 | 2.293 | ns |
| **Mini-LVDS (for MSIOD I/O bank)** | | | | | | | | | | | |
| No pre-emphasis | 1.614 | 1.899 | 1.562 | 1.837 | 1.553 | 1.826 | 1.593 | 1.874 | 1.578 | 1.856 | ns |
| Min. pre-emphasis | 1.604 | 1.887 | 1.745 | 2.053 | 1.731 | 2.036 | 1.892 | 2.225 | 1.861 | 2.189 | ns |
| Med. pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max. pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

## RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

### Minimum and Maximum Input and Output Levels

**Table 81 • RSDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | |
| **RSDS DC Input Voltage Specification** | | | | | | | |
| VI | DC input voltage | | 0 | – | 2.925 | V | |
| **RSDS DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V | |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V | |
| **RSDS Differential Voltage Specification** | | | | | | | |
| VOD | Differential output voltage swing | | 100 | – | 600 | mV | |
| VOCM | Output common mode voltage | | 0.5 | – | 1.5 | V | |
| VICM | Input common mode voltage | | 0.3 | – | 1.5 | V | |
| VID | Input differential voltage | | 100 | – | 600 | mV | |

**Table 82 • RSDS AC Specifications**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **RSDS Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | AC loading: 2 pF / 100 Ohm differential load | – | – | 520 | Mbps | |
| Fmax | Maximum data Rate (for MSIOD I/O banks) | AC loading: 2 pF / 100 Ohm differential load | – | – | 700 | Mbps | |
| **RSDS Impedance Specification** | | | | | | | |
| Rt | Termination resistance | | | 100 | | Ohms | |
| **RSDS AC Test Parameters Specifications** | | | | | | | |
| VTrip | Measuring/trip point for data path | | – | Cross point | – | V | |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2K | – | Ohms | |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF | |

## AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

### AC Switching Characteristics for Receiver (Input Buffers)

**Table 83 • AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| RSDS (for MSIO I/O bank) | None | 2.855 | 3.359 | ns |
| | 100 | 2.85 | 3.353 | ns |
| RSDS (for MSIOD I/O bank) | None | 2.602 | 3.061 | ns |
| | 100 | 2.597 | 3.055 | ns |

### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 84 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | $t_{DP}$ | | $t_{ENZL}$ | | $t_{ENZH}$ | | $t_{ENHZ}$ | | $t_{ENLZ}$ | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | –1 | Std. | |
| **RSDS (for MSIO I/O bank)** | 2.097 | 2.467 | 2.303 | 2.709 | 2.291 | 2.695 | 1.961 | 2.307 | 1.947 | 2.29 | ns |
| **RSDS (for MSIOD I/O bank)** | | | | | | | | | | | |
| No pre-emphasis | 1.614 | 1.899 | 1.559 | 1.834 | 1.55 | 1.823 | 1.59 | 1.87 | 1.575 | 1.852 | ns |
| Min. pre-emphasis | 1.604 | 1.887 | 1.742 | 2.05 | 1.728 | 2.032 | 1.889 | 2.222 | 1.858 | 2.185 | ns |
| Med. pre-emphasis | 1.521 | 1.79 | 1.753 | 2.062 | 1.737 | 2.043 | 1.9 | 2.235 | 1.868 | 2.197 | ns |
| Max. pre-emphasis | 1.492 | 1.754 | 1.762 | 2.073 | 1.745 | 2.052 | 1.91 | 2.247 | 1.876 | 2.206 | ns |

## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. SmartFusion2 devices support only LVPECL receivers and do not support LVPECL transmitters.

### Minimum and Maximum Input and Output Levels

**Table 85 • LVPECL DC Voltage Specification – Applicable to MSIO I/O Banks Only**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V | |
| **LVPECL DC Input Voltage Specification** | | | | | | | |
| VI | DC input voltage | | 0 | – | 3.45 | V | |
| **LVPECL Differential Voltage Specification** | | | | | | | |
| VICM | Input common mode voltage | | 0.3 | – | 2.8 | V | |
| VIDIFF | Input differential voltage | | 100 | 300 | 1,000 | mV | |

**Table 86 • LVPECL AC Specifications (Applicable to MSIO I/O Banks Only)**

| Symbols | Parameters | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVPECL Minimum and Maximum AC Switching Speed** | | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O bank) | | – | – | 900 | Mbps | |

### AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V, VDDI = 2.375 V

***AC Switching Characteristics for Receiver (Input Buffers)***

**Table 87 • LVPECL Receiver Characteristics**
**Worst-Case Commercial Conditions: $T_J$ = 85°C, VDD = 1.14 V, Worst-Case VDDI**

| | On-Die Termination (ODT) | $t_{PY}$ | | Units |
|---|---|---|---|---|
| | | –1 | Std. | |
| **LVPECL (for MSIO I/O bank)** | None | 2.572 | 3.025 | ns |
| | 100 | 2.569 | 3.023 | ns |

# I/O Register Specifications

## Input Register

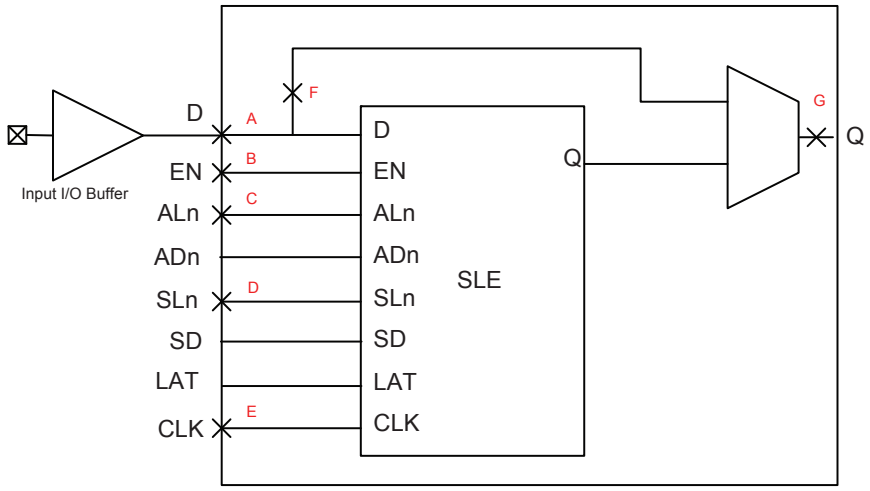



***Figure 3* • Timing Model for Input Register**

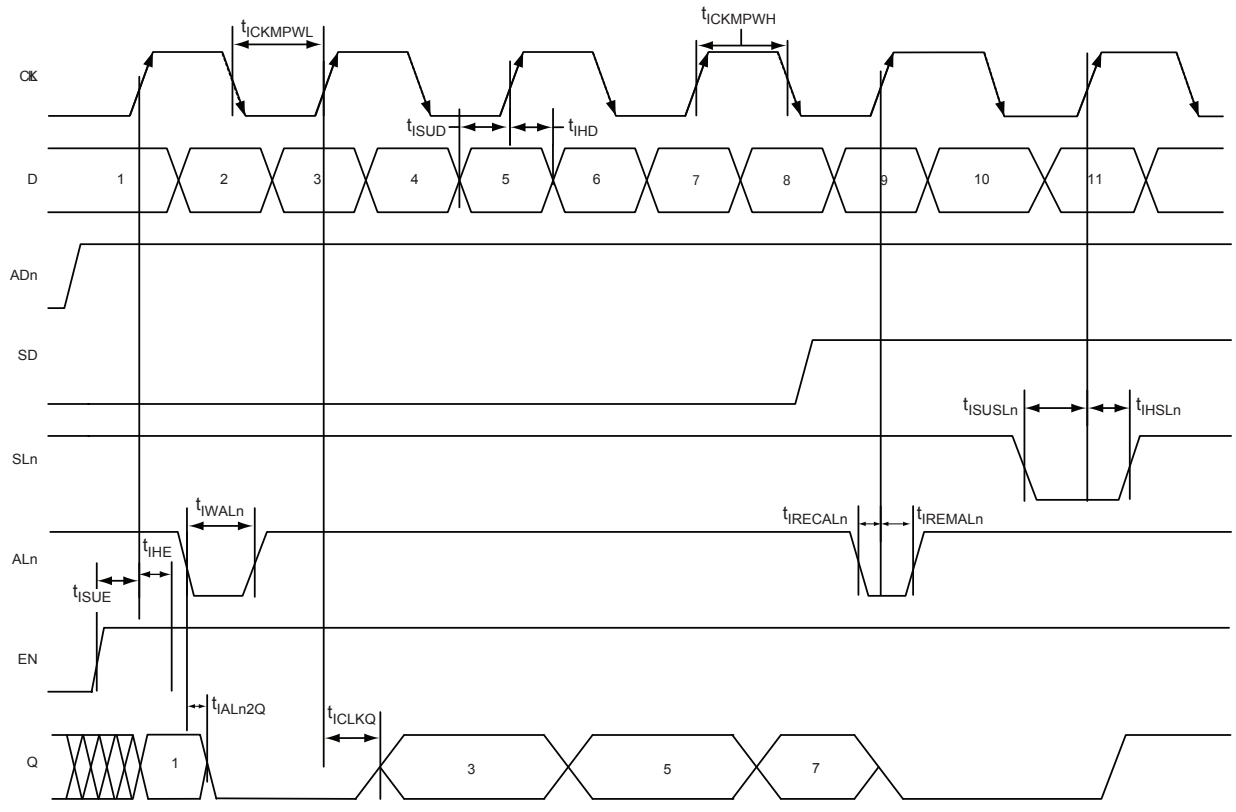



***Figure 4* • I/O Register Input Timing Diagram**

**Table 88 • Input Data Enable Register Propagation Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | Measuring Nodes (from, to)* | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{IBYP}$ | Bypass Delay of the Input Register | F, G | 0.353 | 0.415 | ns |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Register | E, G | 0.16 | 0.188 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Register | A, E | 0.357 | 0.421 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Register | A, E | 0 | 0 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Register | B, E | 0.46 | 0.542 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Register | B, E | 0 | 0 | ns |
| $t_{ISUSL}$ | Synchronous Load Setup Time for the Input Register | D, E | 0.46 | 0.542 | ns |
| $t_{IHSL}$ | Synchronous Load Hold Time for the Input Register | D, E | 0 | 0 | ns |
| $t_{IALn2Q}$ | Asynchronous Clear-to-Q of the Input Register (ADn=1) | C, G | 0.625 | 0.735 | ns |
| | Asynchronous Preset-to-Q of the Input Register (ADn=0) | C, G | 0.587 | 0.69 | ns |
| $t_{IREMALn}$ | Asynchronous Load Removal Time for the Input Register | C, E | 0 | 0 | ns |
| $t_{IRECALn}$ | Asynchronous Load Recovery Time for the Input Register | C, E | 0.074 | 0.087 | ns |
| $t_{IWALn}$ | Asynchronous Load Minimum Pulse Width for the Input Register | C, C | 0.304 | 0.357 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Register | E, E | 0.075 | 0.088 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Register | E, E | 0.159 | 0.187 | ns |

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.*

## Output/Enable Register

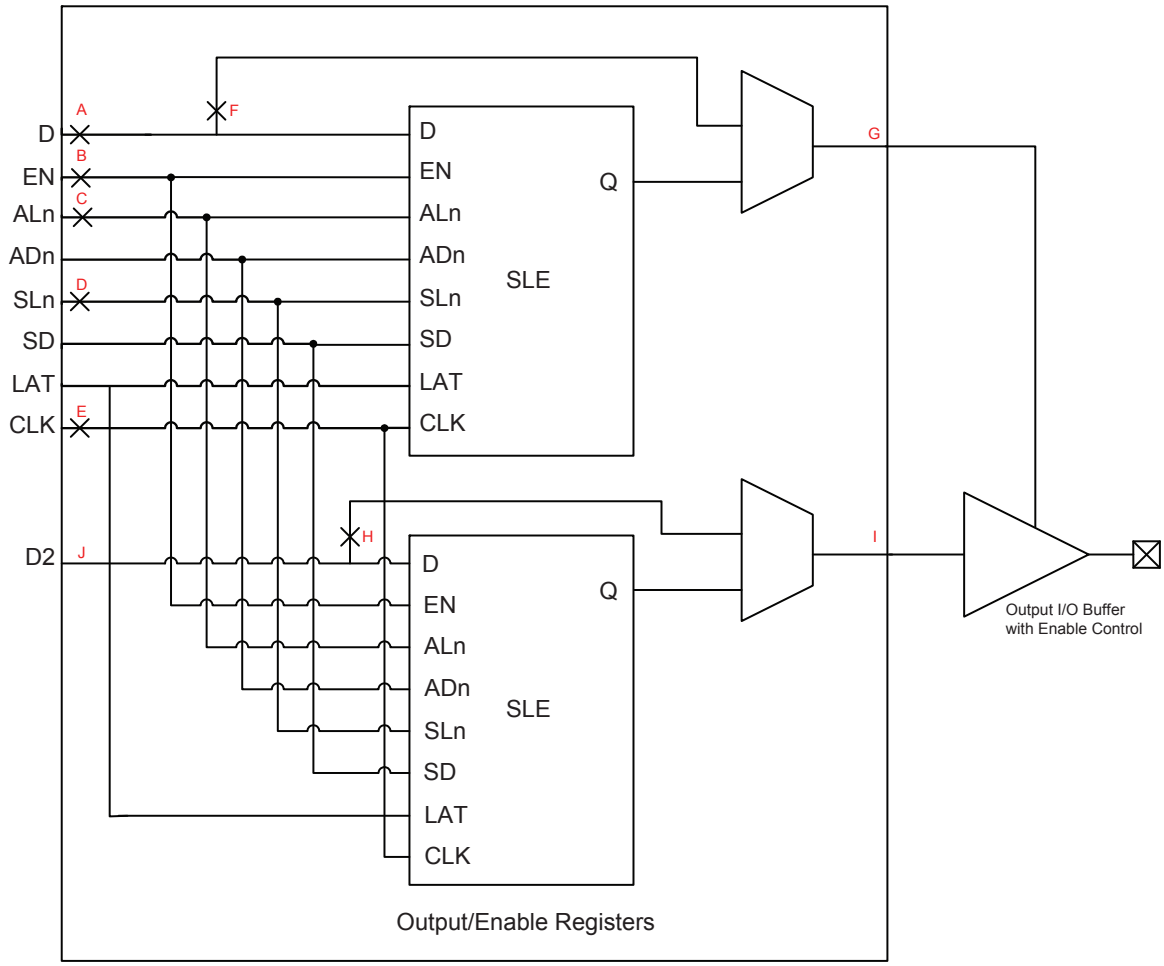



***Figure 5* • Timing Model for Output/Enable Register**

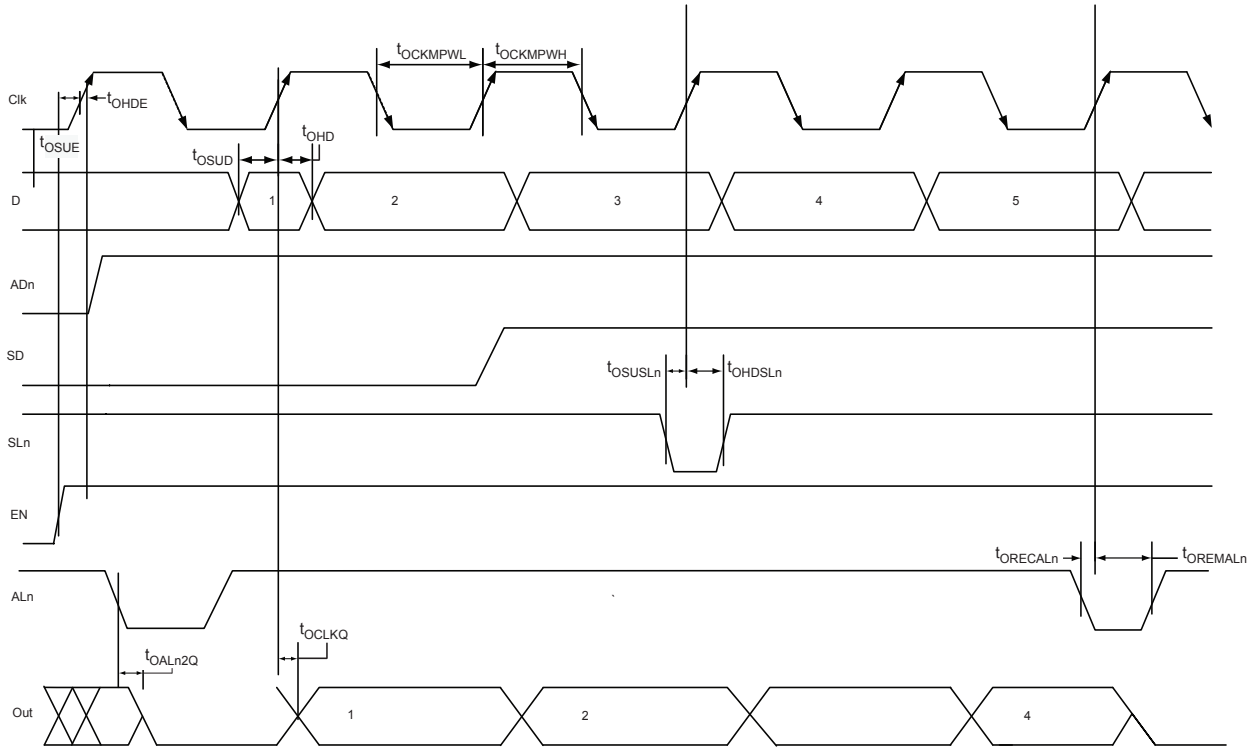



***Figure 6 •*** **I/O Register Output Timing Diagram**

**Table 89 • Output Data/Enable Register Propagation Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | Measuring Nodes (from, to)* | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{OBYP}$ | Bypass Delay of the Output/Enable Register | F, G or H, I | 0.353 | 0.415 | ns |
| $t_{OCLKQ}$ | Clock-to-Q of the Output/Enable Register | E, G or E, I | 0.263 | 0.309 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output/Enable Register | A, E or J, E | 0.19 | 0.223 | ns |
| $t_{OHD}$ | Data Hold Time for the Output/Enable Register | A, E or J, E | 0 | 0 | ns |
| $t_{OSUE}$ | Enable Setup Time for the Output/Enable Register | B, E | 0.419 | 0.493 | ns |
| $t_{OHE}$ | Enable Hold Time for the Output/Enable Register | B, E | 0 | 0 | ns |
| $t_{OSUSL}$ | Synchronous Load Setup Time for the Output/Enable Register | D, E | 0.196 | 0.231 | ns |
| $t_{OHSL}$ | Synchronous Load Hold Time for the Output/Enable Register | D, E | 0 | 0 | ns |
| $t_{OALn2Q}$ | Asynchronous Clear-to-Q of the Output/Enable Register (ADn = 1) | C, G or C, I | 0.505 | 0.594 | ns |
| | Asynchronous Preset-to-Q of the Output/Enable Register (ADn = 0) | C, G or C, I | 0.528 | 0.621 | ns |
| $t_{OREMALn}$ | Asynchronous Load Removal Time for the Output/Enable Register | C, E | 0 | 0 | ns |
| $t_{ORECALn}$ | Asynchronous Load Recovery Time for the Output/Enable Register | C, E | 0.034 | 0.04 | ns |
| $t_{OWALn}$ | Asynchronous Load Minimum Pulse Width for the Output/Enable Register | C, C | 0.304 | 0.357 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output/Enable Register | E, E | 0.075 | 0.088 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output/Enable Register | E, E | 0.159 | 0.187 | ns |

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.*

## DDR Module Specification

### *Input DDR Module*

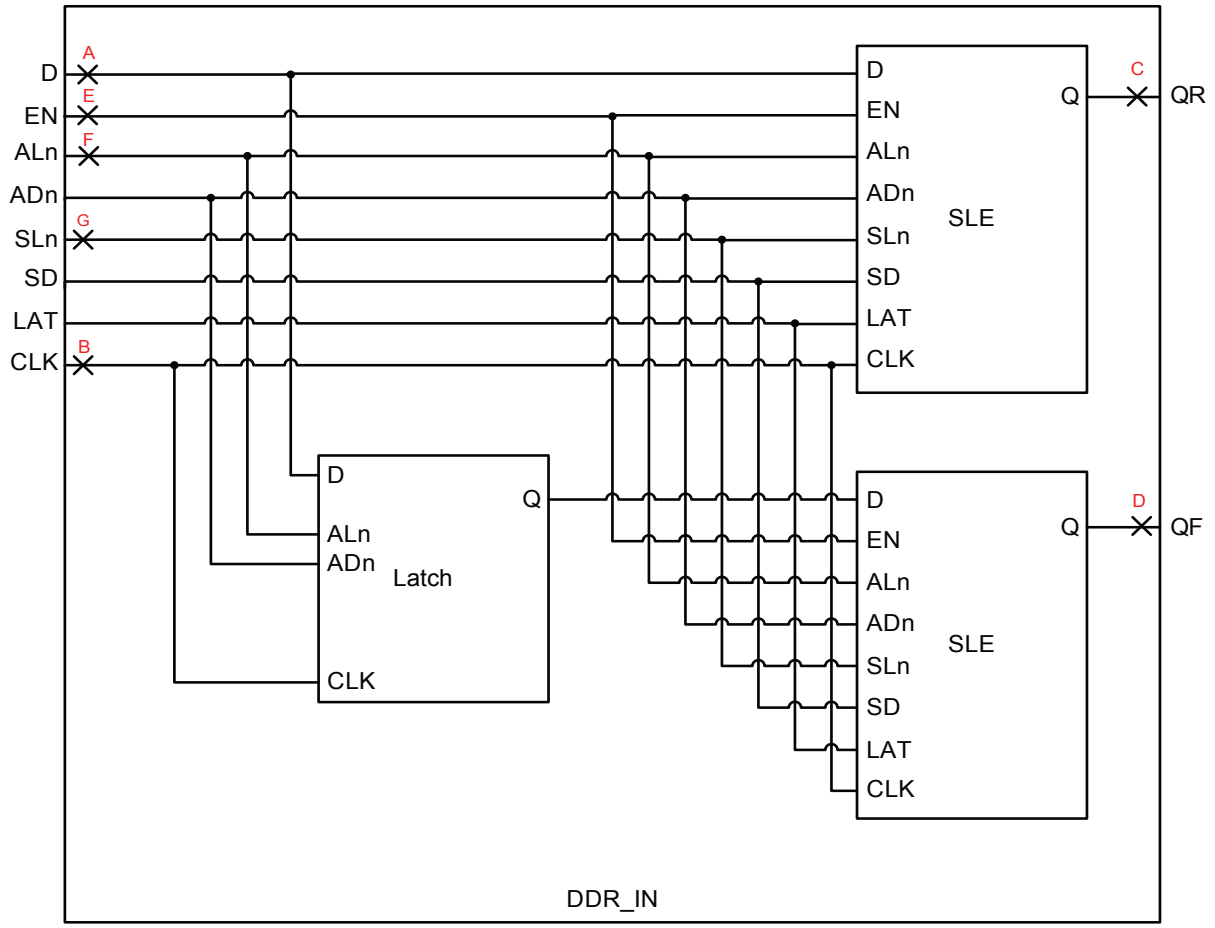



***Figure 7* • Input DDR Module**

## Input DDR Timing Diagram

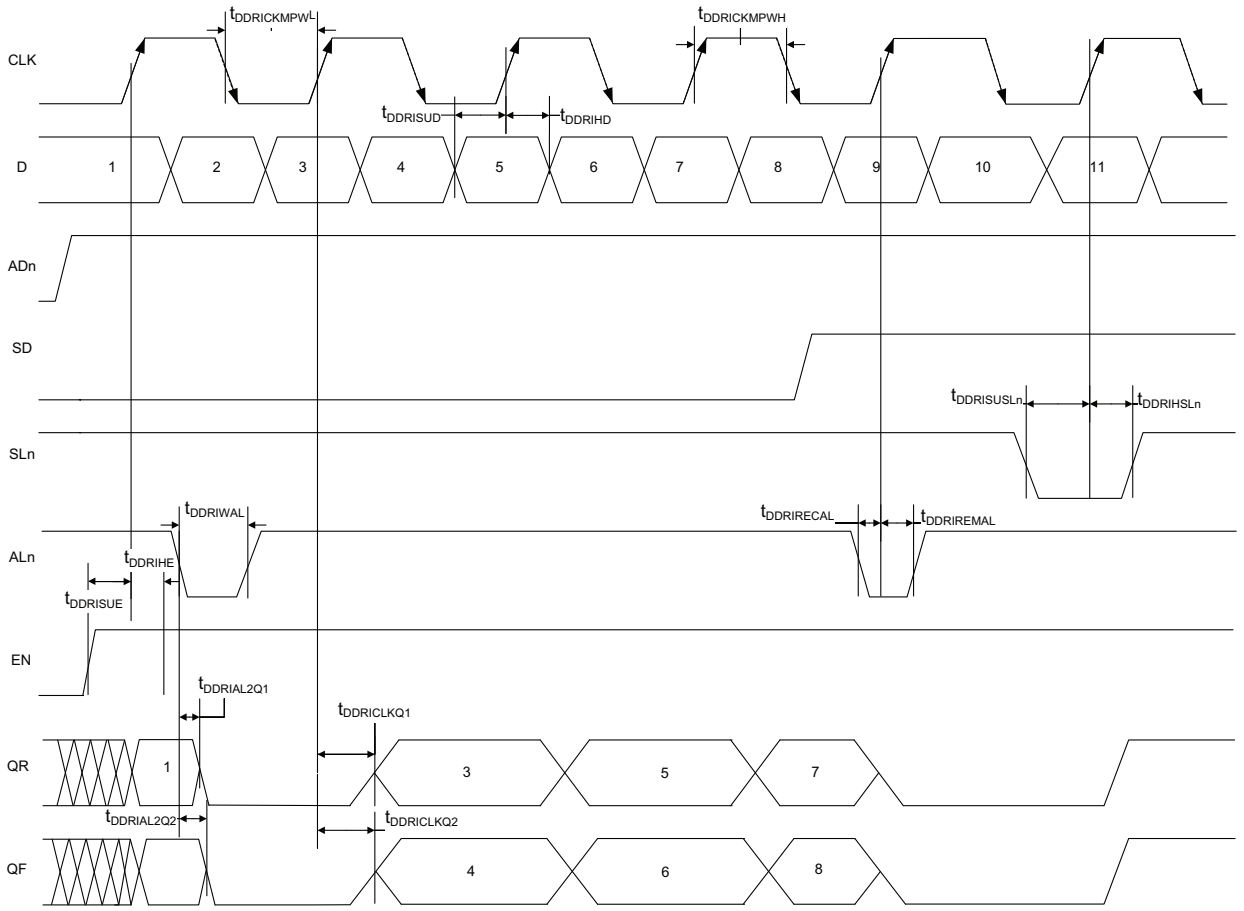



***Figure 8 •*** **Input DDR Timing Diagram**

## Timing Characteristics

**Table 90 • Input DDR Propagation Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | Measuring Nodes (from, to) | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR for Input DDR | B, C | 0.16 | 0.188 | ns |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF for Input DDR | B, D | 0.166 | 0.195 | ns |
| $t_{DDRISUD}$ | Data Setup for Input DDR | A, B | 0.357 | 0.421 | ns |
| $t_{DDRIHD}$ | Data Hold for Input DDR | A, B | 0 | 0 | ns |
| $t_{DDRISUE}$ | Enable Setup for Input DDR | E, B | 0.46 | 0.542 | ns |
| $t_{DDRIHE}$ | Enable Hold for Input DDR | E, B | 0 | 0 | ns |
| $t_{DDRISUSLn}$ | Synchronous Load Setup for Input DDR | G, B | 0.46 | 0.542 | ns |
| $t_{DDRIHSLn}$ | Synchronous Load Hold for Input DDR | G, B | 0 | 0 | ns |
| $t_{DDRIAL2Q1}$ | Asynchronous Load-to-Out QR for Input DDR | F, C | 0.587 | 0.69 | ns |
| $t_{DDRIAL2Q2}$ | Asynchronous Load-to-Out QF for Input DDR | F, D | 0.541 | 0.636 | ns |
| $t_{DDRIREMAL}$ | Asynchronous Load Removal time for Input DDR | F, B | 0 | 0 | ns |
| $t_{DDRIRECAL}$ | Asynchronous Load Recovery time for Input DDR | F, B | 0.074 | 0.087 | ns |
| $t_{DDRIWAL}$ | Asynchronous Load Minimum Pulse Width for Input DDR | F, F | 0.304 | 0.357 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width High for Input DDR | B, B | 0.075 | 0.088 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width Low for Input DDR | B, B | 0.159 | 0.187 | ns |

## Output DDR Module

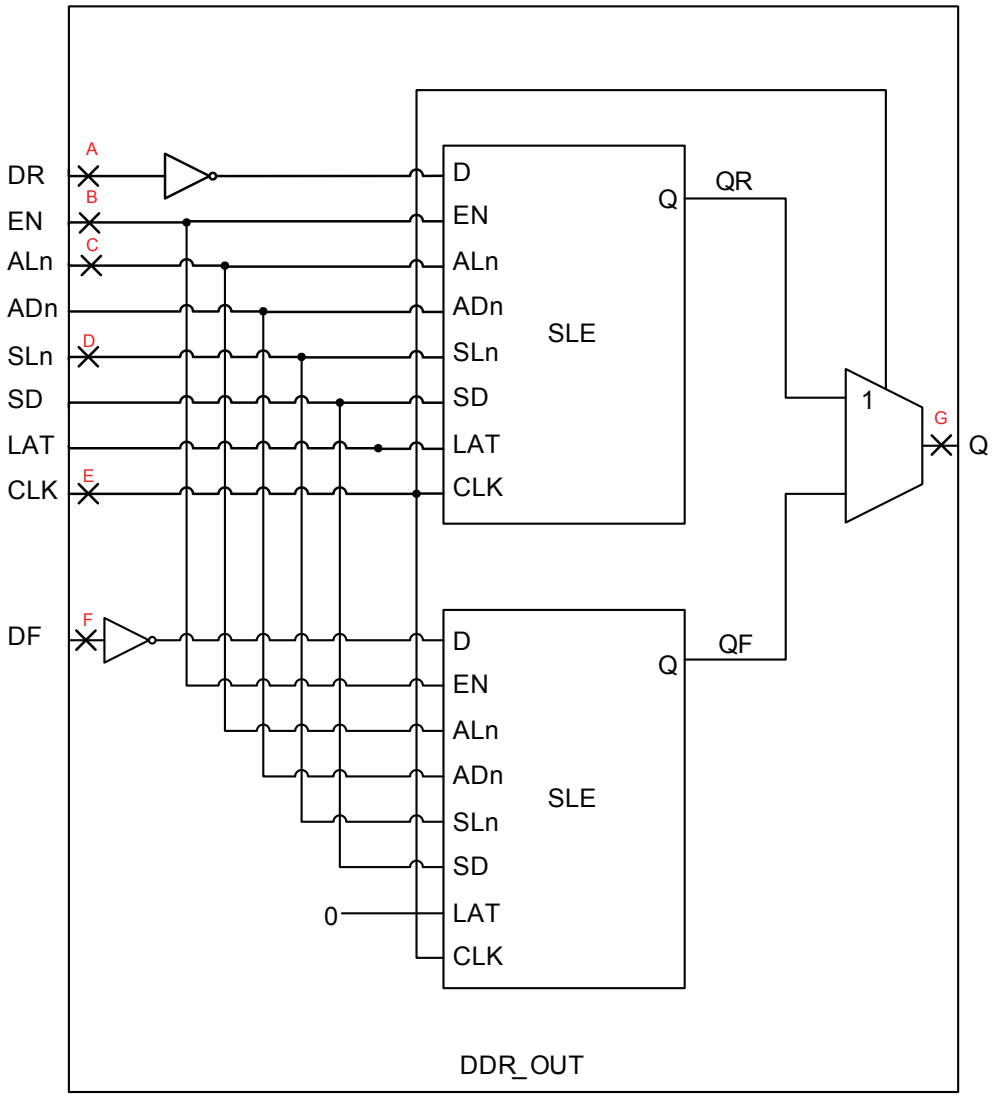



***Figure 9* • Output DDR Module**

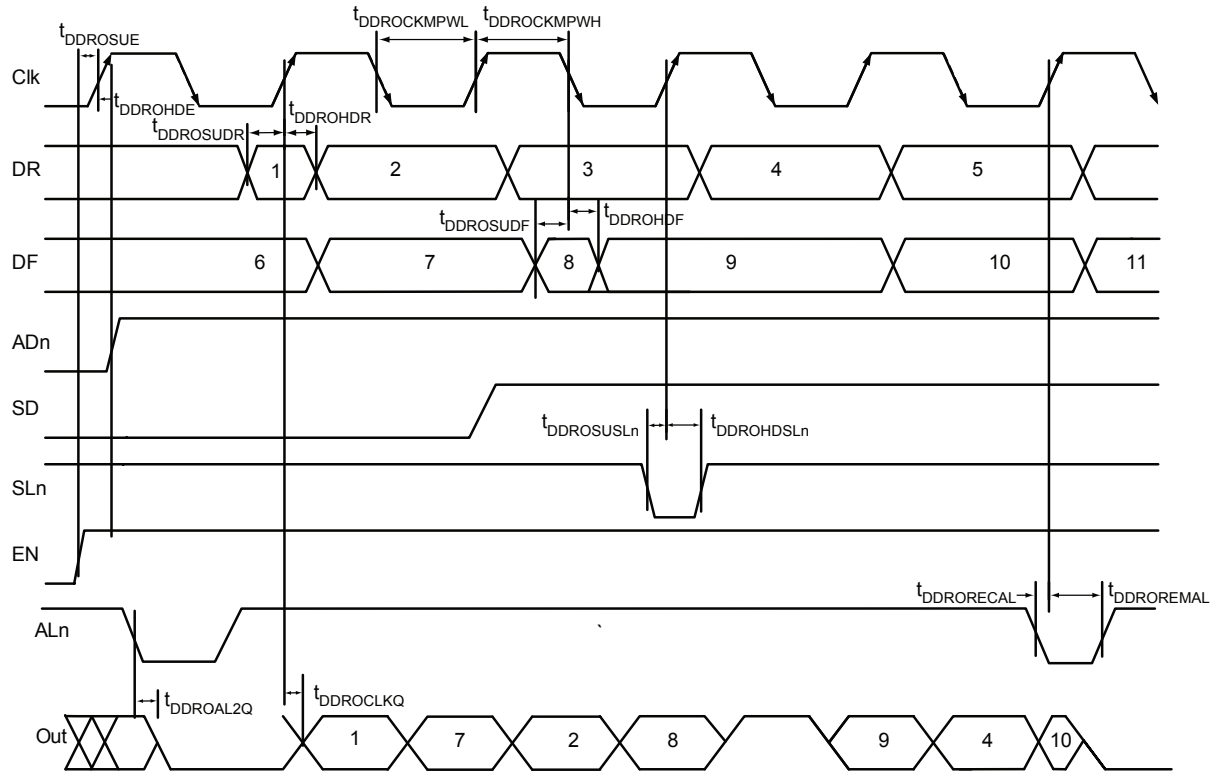



***Figure 10* • Output DDR Timing Diagram**

## Timing Characteristics

**Table 91 • Output DDR Propagation Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | Measuring Nodes (from, to) | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out of DDR for Output DDR | E, G | 0.263 | 0.309 | ns |
| $t_{DDROSUDF}$ | Data_F Data Setup for Output DDR | F, E | 0.143 | 0.168 | ns |
| $t_{DDROSUDR}$ | Data_R Data Setup for Output DDR | A, E | 0.19 | 0.223 | ns |
| $t_{DDROHDF}$ | Data_F Data Hold for Output DDR | F, E | 0 | 0 | ns |
| $t_{DDROHDR}$ | Data_R Data Hold for Output DDR | A, E | 0 | 0 | ns |
| $t_{DDROSUE}$ | Enable Setup for Input DDR | B, E | 0.419 | 0.493 | ns |
| $t_{DDROHE}$ | Enable Hold for Input DDR | B, E | 0 | 0 | ns |
| $t_{DDROSUSLn}$ | Synchronous Load Setup for Input DDR | D, E | 0.196 | 0.231 | ns |
| $t_{DDROHSLn}$ | Synchronous Load Hold for Input DDR | D, E | 0 | 0 | ns |
| $t_{DDROAL2Q}$ | Asynchronous Load-to-Out for Output DDR | C, G | 0.528 | 0.621 | ns |
| $t_{DDROREMAL}$ | Asynchronous Load Removal time for Output DDR | C, E | 0 | 0 | ns |
| $t_{DDRORECAL}$ | Asynchronous Load Recovery time for Output DDR | C, E | 0.034 | 0.04 | ns |
| $t_{DDROWAL}$ | Asynchronous Load Minimum Pulse Width for Output DDR | C, C | 0.304 | 0.357 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | E, E | 0.075 | 0.088 | ns |
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | E, E | 0.159 | 0.187 | ns |

# Logic Element Specifications

## 4-input LUT (LUT-4)

The SmartFusion2 offers a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 Macro Library Guide*.

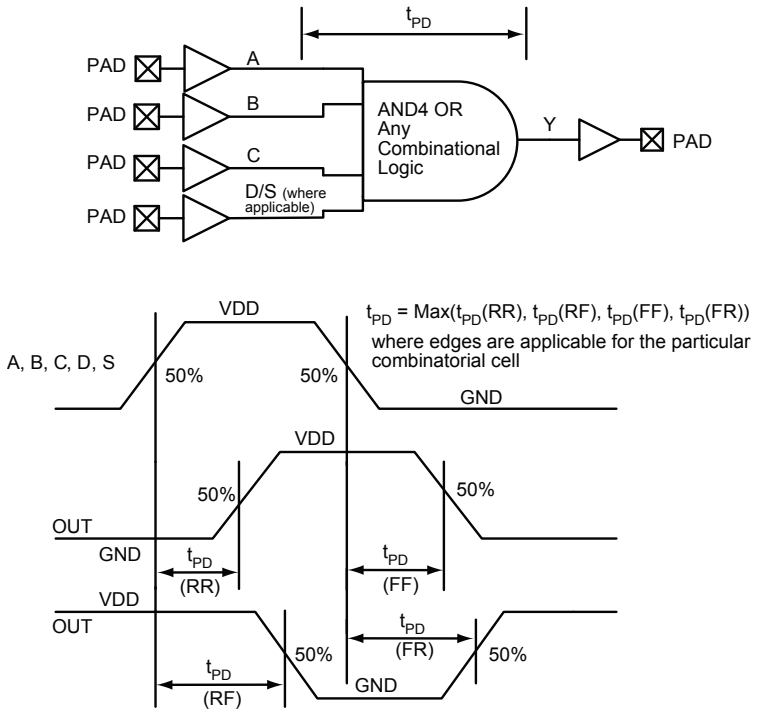



***Figure 11 •*** **LUT-4**

### *Timing Characteristics*

***Table 92 •*** **Combinatorial Cell Propagation Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Combinatorial Cell | Equation | Parameter | –1 | Std. | Units | Notes |
|---|---|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.102 | 0.12 | ns | |
| AND2 | Y = A · B | $t_{PD}$ | 0.179 | 0.211 | ns | |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.144 | 0.169 | ns | |
| OR2 | Y = A + B | $t_{PD}$ | 0.179 | 0.211 | ns | |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.144 | 0.169 | ns | |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.179 | 0.211 | ns | |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.241 | 0.283 | ns | |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.198 | 0.233 | ns | |
| AND4 | Y = A · B · C · D | $t_{PD}$ | 0.371 | 0.436 | ns | |

## Sequential Module

SmartFusion2 offers a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

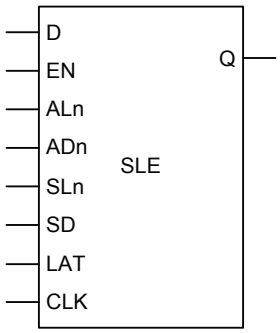



***Figure 12 •*** **Sequential Module**

Figure 13 shows a configuration with SD = 1 (synchronous preset) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

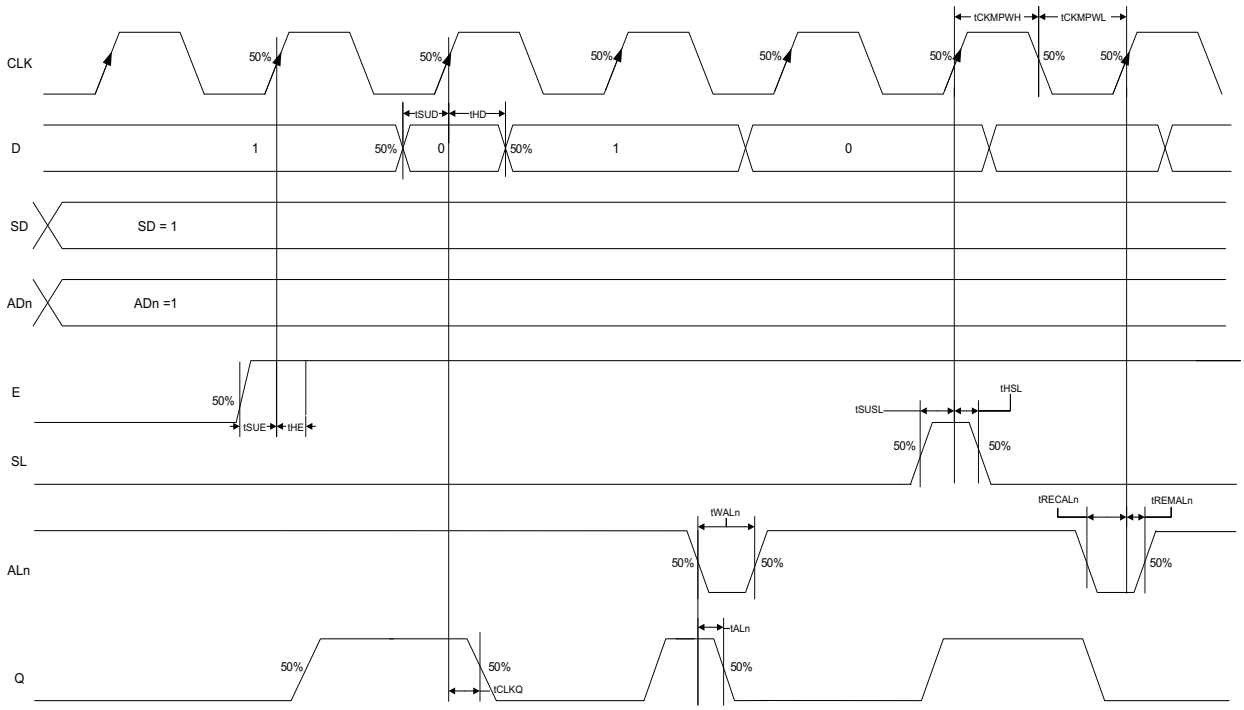



***Figure 13 •*** **Timing Diagram**

## Timing Characteristics

**Table 93 • Register Delays**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | Std. | Units | Notes |
|---|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core register | 0.108 | 0.127 | ns | |
| $t_{SUD}$ | Data Setup Time for the Core register | 0.254 | 0.298 | ns | |
| $t_{HD}$ | Data Hold Time for the Core register | 0 | 0 | ns | |
| $t_{SUE}$ | Enable Setup Time for the Core register | 0.335 | 0.394 | ns | |
| $t_{HE}$ | Enable Hold Time for the Core register | 0 | 0 | ns | |
| $t_{SUSL}$ | Synchronous Load Setup Time for the Core register | 0.335 | 0.394 | ns | |
| $t_{HSL}$ | Synchronous Load Hold Time for the Core register | 0 | 0 | ns | |
| $t_{ALn2Q}$ | Asynchronous Clear-to-Q of the Core register (ADn = 1) | 0.473 | 0.556 | ns | |
| | Asynchronous Preset-to-Q of the Core register (ADn = 0) | 0.451 | 0.531 | ns | |
| $t_{REMALn}$ | Asynchronous Load Removal Time for the Core register | 0 | 0 | ns | |
| $t_{RECALn}$ | Asynchronous Load Recovery Time for the Core register | 0.353 | 0.415 | ns | |
| $t_{WALn}$ | Asynchronous Load Minimum Pulse Width for the Core register | 0.304 | 0.357 | ns | |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core register | 0.075 | 0.088 | ns | |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core register | 0.159 | 0.187 | ns | |

# Global Resource Characteristics

SmartFusion2 devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *SmartFusion2 FPGA Fabric Architecture User Guide* for the positions of various global routing resources. .

***Table 94 •*** **M2S150T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.83 | 0.911 | 0.831 | 0.913 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.457 | 1.588 | 1.715 | 1.869 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.131 | | 0.154 | ns | |

***Table 95 •*** **M2S100T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.83 | 0.911 | 0.831 | 0.913 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.457 | 1.588 | 1.715 | 1.869 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.131 | | 0.154 | ns | |

***Table 96 •*** **M2S090T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.835 | 0.888 | 0.833 | 0.886 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.405 | 1.489 | 1.654 | 1.752 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.084 | | 0.098 | ns | |

***Table 97 •*** **M2S050T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.827 | 0.897 | 0.826 | 0.896 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.419 | 1.53 | 1.671 | 1.8 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.111 | | 0.129 | ns | |

**Table 98 • M2S025T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.747 | 0.799 | 0.745 | 0.797 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.294 | 1.378 | 1.522 | 1.621 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.084 | | 0.099 | ns | |

**Table 99 • M2S010T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.626 | 0.669 | 0.627 | 0.668 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.112 | 1.182 | 1.308 | 1.393 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.07 | | 0.085 | ns | |

**Table 100 • M2S005T Global Resource**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.625 | 0.66 | 0.628 | 0.66 | ns | |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.126 | 1.187 | 1.325 | 1.397 | ns | |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.061 | | 0.072 | ns | |

# FPGA Fabric SRAM

Refer to the *SmartFusion2 FPGA Fabric Architecture User Guide* for more information.

## FPGA Fabric Large SRAM (LSRAM)

***Table 101 •*** **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock Period | 1.882 | – | 2.214 | – | ns |
| $t_{CLKMPWH}$ | Clock Minimum Pulse Width High | 0.781 | – | 0.919 | – | ns |
| $t_{CLKMPWL}$ | Clock Minimum pulse Width Low | 0.302 | – | 0.355 | – | ns |
| $t_{PLCY}$ | Pipelined Clock Period | 1.991 | – | 2.342 | – | ns |
| $t_{PLCLKMPWH}$ | Pipelined Clock Minimum Pulse Width High | 0.785 | – | 0.923 | – | ns |
| $t_{PLCLKMPWL}$ | Pipelined Clock Minimum pulse Width Low | 0.299 | – | 0.352 | – | ns |
| $t_{CLK2Q}$ | Read Access Time with Pipeline Register | – | 0.334 | – | 0.393 | ns |
| | Read Access Time without Pipeline Register | – | 2.273 | – | 2.674 | ns |
| | Access Time with Feed-Through Write Timing | – | 1.529 | – | 1.799 | ns |
| $t_{ADDRSU}$ | Address Setup Time | 0.441 | – | 0.519 | – | ns |
| $t_{ADDRHD}$ | Address Hold Time | 0.274 | – | 0.322 | – | ns |
| $t_{DSU}$ | Data Setup Time | 0.341 | – | 0.401 | – | ns |
| $t_{DHD}$ | Data Hold Time | 0.107 | – | 0.126 | – | ns |
| $t_{BLKSU}$ | Block Select Setup Time | 0.207 | – | 0.244 | – | ns |
| $t_{BLKHD}$ | Block Select Hold Time | 0.216 | – | 0.254 | – | ns |
| $t_{BLK2Q}$ | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 1.529 | – | 1.799 | ns |
| $t_{BLKMPW}$ | Block Select Minimum Pulse Width | 0.186 | – | 0.219 | – | ns |
| $t_{RDESU}$ | Read Enable Setup Time | 0.449 | – | 0.528 | – | ns |
| $t_{RDEHD}$ | Read Enable Hold Time | 0.167 | – | 0.197 | – | ns |
| $t_{RDPLESU}$ | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.248 | – | 0.291 | – | ns |
| $t_{RDPLEHD}$ | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.102 | – | 0.12 | – | ns |
| $t_{R2Q}$ | Asynchronous Reset to Output Propagation Delay | – | 1.506 | | 1.772 | ns |
| $t_{RSTREM}$ | Asynchronous Reset Removal Time | 0.506 | – | 0.595 | – | ns |
| $t_{RSTREC}$ | Asynchronous Reset Recovery Time | 0.004 | – | 0.005 | – | ns |
| $t_{RSTMPW}$ | Asynchronous Reset Minimum Pulse Width | 0.301 | – | 0.354 | – | ns |
| $t_{PLRSTREM}$ | Pipelined Register Asynchronous Reset Removal Time | -0.279 | – | -0.328 | – | ns |
| $t_{PLRSTREC}$ | Pipelined Register Asynchronous Reset Recovery Time | 0.327 | – | 0.385 | – | ns |
| $t_{PLRSTMPW}$ | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.282 | – | 0.332 | – | ns |
| $t_{SRSTSU}$ | Synchronous Reset Setup Time | 0.226 | – | 0.265 | – | ns |
| $t_{SRSTHD}$ | Synchronous Reset Hold Time | 0.036 | – | 0.043 | – | ns |
| $t_{WESU}$ | Write Enable Setup Time (A_WEN, B_WEN = 1) | 0.39 | – | 0.458 | – | ns |
| $t_{WEHD}$ | Write Enable Hold Time (A_WEN, B_WEN = 1) | 0.242 | – | 0.285 | – | ns |

**Table 102 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock period | 1.882 | – | 2.214 | – | ns |
| $t_{CLKMPWH}$ | Clock minimum pulse width High | 0.781 | – | 0.919 | – | ns |
| $t_{CLKMPWL}$ | Clock minimum pulse width Low | 0.302 | – | 0.355 | – | ns |
| $t_{PLCY}$ | Pipelined clock period | 1.991 | – | 2.342 | – | ns |
| $t_{PLCLKMPWH}$ | Pipelined clock minimum pulse width High | 0.785 | – | 0.923 | – | ns |
| $t_{PLCLKMPWL}$ | Pipelined clock minimum pulse width Low | 0.299 | – | 0.352 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.334 | – | 0.393 | ns |
| | Read access time without pipeline register | – | 2.273 | – | 2.674 | ns |
| | Access time with feed-through write timing | – | 1.529 | – | 1.799 | ns |
| $t_{ADDRSU}$ | Address setup time | 0.475 | – | 0.559 | – | ns |
| $t_{ADDRHD}$ | Address hold time | 0.274 | – | 0.322 | – | ns |
| $t_{DSU}$ | Data setup time | 0.336 | – | 0.395 | – | ns |
| $t_{DHD}$ | Data hold time | 0.082 | – | 0.096 | – | ns |
| $t_{BLKSU}$ | Block select setup time | 0.207 | – | 0.244 | – | ns |
| $t_{BLKHD}$ | Block select hold time | 0.216 | – | 0.254 | – | ns |
| $t_{BLK2Q}$ | Block select to out disable time (when pipelined register is disabled) | – | 1.529 | – | 1.799 | ns |
| $t_{BLKMPW}$ | Block select minimum pulse width | 0.186 | – | 0.219 | – | ns |
| $t_{RDESU}$ | Read enable setup time (A_WEN, B_WEN = 0) | 0.485 | – | 0.57 | – | ns |
| $t_{RDEHD}$ | Read enable hold time (A_WEN, B_WEN = 0) | 0.071 | – | 0.083 | – | ns |
| $t_{RDPLESU}$ | Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | 0.248 | – | 0.291 | – | ns |
| $t_{RDPLEHD}$ | Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | 0.102 | – | 0.12 | – | ns |
| $t_{R2Q}$ | Asynchronous reset to output propagation delay | – | 1.514 | – | 1.781 | ns |
| $t_{RSTREM}$ | Asynchronous reset removal time | 0.506 | – | 0.595 | – | ns |
| $t_{RSTREC}$ | Asynchronous reset recovery time | 0.004 | – | 0.005 | – | ns |
| $t_{RSTMPW}$ | Asynchronous reset minimum pulse width | 0.301 | – | 0.354 | – | ns |
| $t_{PLRSTREM}$ | Pipelined register asynchronous reset removal time | -0.279 | – | -0.328 | – | ns |
| $t_{PLRSTREC}$ | Pipelined register asynchronous reset recovery time | 0.327 | – | 0.385 | – | ns |
| $t_{PLRSTMPW}$ | Pipelined register asynchronous reset minimum pulse width | 0.282 | – | 0.332 | – | ns |
| $t_{SRSTSU}$ | Synchronous reset setup time | 0.226 | – | 0.265 | – | ns |
| $t_{SRSTHD}$ | Synchronous reset hold time | 0.036 | – | 0.043 | – | ns |
| $t_{WESU}$ | Write enable setup time (A_WEN, B_WEN = 1) | 0.415 | – | 0.488 | – | ns |
| $t_{WEHD}$ | Write enable hold time (A_WEN, B_WEN = 1) | 0.048 | – | 0.057 | – | ns |

**Table 103 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock period | 1.882 | – | 2.214 | – | ns |
| $t_{CLKMPWH}$ | Clock minimum pulse width High | 0.781 | – | 0.919 | – | ns |
| $t_{CLKMPWL}$ | Clock minimum pulse width Low | 0.302 | – | 0.355 | – | ns |
| $t_{PLCY}$ | Pipelined clock period | 1.991 | – | 2.342 | – | ns |
| $t_{PLCLKMPWH}$ | Pipelined clock minimum pulse width High | 0.785 | – | 0.923 | – | ns |
| $t_{PLCLKMPWL}$ | Pipelined clock minimum pulse width Low | 0.299 | – | 0.352 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.323 | – | 0.38 | ns |
| | Read access time without pipeline register | – | 2.273 | – | 2.673 | ns |
| | Access time with feed-through write timing | – | 1.511 | – | 1.778 | ns |
| $t_{ADDRSU}$ | Address setup time | 0.543 | – | 0.638 | – | ns |
| $t_{ADDRHD}$ | Address hold time | 0.274 | – | 0.322 | – | ns |
| $t_{DSU}$ | Data setup time | 0.334 | – | 0.393 | – | ns |
| $t_{DHD}$ | Data hold time | 0.082 | – | 0.096 | – | ns |
| $t_{BLKSU}$ | Block select setup time | 0.207 | – | 0.244 | – | ns |
| $t_{BLKHD}$ | Block select hold time | 0.216 | – | 0.254 | – | ns |
| $t_{BLK2Q}$ | Block select to out disable time (when pipelined register is disabled) | – | 1.511 | – | 1.778 | ns |
| $t_{BLKMPW}$ | Block select minimum pulse width | 0.186 | – | 0.219 | – | ns |
| $t_{RDESU}$ | Read enable setup time (A_WEN, B_WEN = 0) | 0.516 | – | 0.607 | – | ns |
| $t_{RDEHD}$ | Read enable hold time (A_WEN, B_WEN = 0) | 0.071 | – | 0.083 | – | ns |
| $t_{RDPLESU}$ | Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | 0.248 | – | 0.291 | – | ns |
| $t_{RDPLEHD}$ | Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | 0.102 | – | 0.12 | – | ns |
| $t_{R2Q}$ | Asynchronous reset to output propagation delay | – | 1.507 | – | 1.773 | ns |
| $t_{RSTREM}$ | Asynchronous reset removal time | 0.506 | – | 0.595 | – | ns |
| $t_{RSTREC}$ | Asynchronous reset recovery time | 0.004 | – | 0.005 | – | ns |
| $t_{RSTMPW}$ | Asynchronous reset minimum pulse width | 0.301 | – | 0.354 | – | ns |
| $t_{PLRSTREM}$ | Pipelined register asynchronous reset removal time | -0.279 | – | -0.328 | – | ns |
| $t_{PLRSTREC}$ | Pipelined register asynchronous reset recovery time | 0.327 | – | 0.385 | – | ns |
| $t_{PLRSTMPW}$ | Pipelined register asynchronous reset minimum pulse width | 0.282 | – | 0.332 | – | ns |
| $t_{SRSTSU}$ | Synchronous reset setup time | 0.226 | – | 0.265 | – | ns |
| $t_{SRSTHD}$ | Synchronous reset hold time | 0.036 | – | 0.043 | – | ns |
| $t_{WESU}$ | Write enable setup time (A_WEN, B_WEN = 1) | 0.458 | – | 0.539 | – | ns |
| $t_{WEHD}$ | Write enable hold time (A_WEN, B_WEN = 1) | 0.048 | – | 0.057 | – | ns |

**Table 104 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2 Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock period | 1.882 | – | 2.214 | – | ns |
| $t_{CLKMPWH}$ | Clock minimum pulse width High | 0.781 | – | 0.919 | – | ns |
| $t_{CLKMPWL}$ | Clock minimum pulse width Low | 0.302 | – | 0.355 | – | ns |
| $t_{PLCY}$ | Pipelined clock period | 1.991 | – | 2.342 | – | ns |
| $t_{PLCLKMPWH}$ | Pipelined clock minimum pulse width High | 0.785 | – | 0.923 | – | ns |
| $t_{PLCLKMPWL}$ | Pipelined clock minimum pulse width Low | 0.299 | – | 0.352 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.32 | – | 0.377 | ns |
| | Read access time without pipeline register | – | 2.272 | – | 2.673 | ns |
| | Access time with feed-through write timing | – | 1.511 | – | 1.778 | ns |
| $t_{ADDRSU}$ | Address setup time | 0.612 | – | 0.72 | – | ns |
| $t_{ADDRHD}$ | Address hold time | 0.274 | – | 0.322 | – | ns |
| $t_{DSU}$ | Data setup time | 0.33 | – | 0.388 | – | ns |
| $t_{DHD}$ | Data hold time | 0.082 | – | 0.096 | – | ns |
| $t_{BLKSU}$ | Block select setup time | 0.207 | – | 0.244 | – | ns |
| $t_{BLKHD}$ | Block select hold time | 0.216 | – | 0.254 | – | ns |
| $t_{BLK2Q}$ | Block select to out disable time (when pipelined register is disabled) | – | 1.511 | – | 1.778 | ns |
| $t_{BLKMPW}$ | Block select minimum pulse width | 0.186 | – | 0.219 | – | ns |
| $t_{RDESU}$ | Read enable setup time (A_WEN, B_WEN = 0) | 0.529 | – | 0.622 | – | ns |
| $t_{RDEHD}$ | Read enable hold time (A_WEN, B_WEN = 0) | 0.071 | – | 0.083 | – | ns |
| $t_{RDPLESU}$ | Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | 0.248 | – | 0.291 | – | ns |
| $t_{RDPLEHD}$ | Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | 0.102 | – | 0.12 | – | ns |
| $t_{R2Q}$ | Asynchronous reset to output propagation delay | – | 1.528 | – | 1.797 | ns |
| $t_{RSTREM}$ | Asynchronous reset removal time | 0.506 | – | 0.595 | – | ns |
| $t_{RSTREC}$ | Asynchronous reset recovery time | 0.004 | – | 0.005 | – | ns |
| $t_{RSTMPW}$ | Asynchronous reset minimum pulse width | 0.301 | – | 0.354 | – | ns |
| $t_{PLRSTREM}$ | Pipelined register asynchronous reset removal time | -0.279 | – | -0.328 | – | ns |
| $t_{PLRSTREC}$ | Pipelined register asynchronous reset recovery time | 0.327 | – | 0.385 | – | ns |
| $t_{PLRSTMPW}$ | Pipelined register asynchronous reset minimum pulse width | 0.282 | – | 0.332 | – | ns |
| $t_{SRSTSU}$ | Synchronous reset setup time | 0.226 | – | 0.265 | – | ns |
| $t_{SRSTHD}$ | Synchronous reset hold time | 0.036 | – | 0.043 | – | ns |
| $t_{WESU}$ | Write enable setup time (A_WEN, B_WEN = 1) | 0.488 | – | 0.574 | – | ns |
| $t_{WEHD}$ | Write enable hold time (A_WEN, B_WEN = 1) | 0.048 | – | 0.057 | – | ns |

**Table 105 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock period | 1.882 | – | 2.214 | – | ns |
| $t_{CLKMPWH}$ | Clock minimum pulse width High | 0.781 | – | 0.919 | – | ns |
| $t_{CLKMPWL}$ | Clock minimum pulse width Low | 0.302 | – | 0.355 | – | ns |
| $t_{PLCY}$ | Pipelined clock period | 1.991 | – | 2.342 | – | ns |
| $t_{PLCLKMPWH}$ | Pipelined clock minimum pulse width High | 0.785 | – | 0.923 | – | ns |
| $t_{PLCLKMPWL}$ | Pipelined clock minimum pulse width Low | 0.299 | – | 0.352 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.32 | – | 0.377 | ns |
| | Read access time without pipeline register | – | 2.269 | – | 2.669 | ns |
| | Access time with feed-through write timing | – | 1.51 | – | 1.777 | ns |
| $t_{ADDRSU}$ | Address setup time | 0.626 | – | 0.737 | – | ns |
| $t_{ADDRHD}$ | Address hold time | 0.274 | – | 0.322 | – | ns |
| $t_{DSU}$ | Data setup time | 0.322 | – | 0.378 | – | ns |
| $t_{DHD}$ | Data hold time | 0.082 | – | 0.096 | – | ns |
| $t_{BLKSU}$ | Block select setup time | 0.207 | – | 0.244 | – | ns |
| $t_{BLKHD}$ | Block select hold time | 0.216 | – | 0.254 | – | ns |
| $t_{BLK2Q}$ | Block select to out disable time (when pipelined register is disabled) | – | 1.51 | – | 1.777 | ns |
| $t_{BLKMPW}$ | Block select minimum pulse width | 0.186 | – | 0.219 | – | ns |
| $t_{RDESU}$ | Read enable setup time (A_WEN, B_WEN = 0) | 0.53 | – | 0.624 | – | ns |
| $t_{RDEHD}$ | Read enable hold time (A_WEN, B_WEN = 0) | 0.071 | – | 0.083 | – | ns |
| $t_{RDPLESU}$ | Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | 0.248 | – | 0.291 | – | ns |
| $t_{RDPLEHD}$ | Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | 0.102 | – | 0.12 | – | ns |
| $t_{R2Q}$ | Asynchronous reset to output propagation delay | – | 1.547 | – | 1.82 | ns |
| $t_{RSTREM}$ | Asynchronous reset removal time | 0.506 | – | 0.595 | – | ns |
| $t_{RSTREC}$ | Asynchronous reset recovery time | 0.004 | – | 0.005 | – | ns |
| $t_{RSTMPW}$ | Asynchronous reset minimum pulse width | 0.301 | – | 0.354 | – | ns |
| $t_{PLRSTREM}$ | Pipelined register asynchronous reset removal time | -0.279 | – | -0.328 | – | ns |
| $t_{PLRSTREC}$ | Pipelined register asynchronous reset recovery time | 0.327 | – | 0.385 | – | ns |
| $t_{PLRSTMPW}$ | Pipelined register asynchronous reset minimum pulse width | 0.282 | – | 0.332 | – | ns |
| $t_{SRSTSU}$ | Synchronous reset setup time | 0.226 | – | 0.265 | – | ns |
| $t_{SRSTHD}$ | Synchronous reset hold time | 0.036 | – | 0.043 | – | ns |
| $t_{WESU}$ | Write enable setup time (A_WEN, B_WEN = 1) | 0.454 | – | 0.534 | – | ns |
| $t_{WEHD}$ | Write enable hold time (A_WEN, B_WEN = 1) | 0.048 | – | 0.057 | – | ns |

**Table 106 • RAM1K18 – Two-Port Mode for Depth × Width C0nfiguration 512 × 36**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Clock period | 1.882 | – | 2.214 | – | ns |
| $t_{CLKMPWH}$ | Clock minimum pulse width High | 0.781 | – | 0.919 | – | ns |
| $t_{CLKMPWL}$ | Clock minimum pulse width Low | 0.302 | – | 0.355 | – | ns |
| $t_{PLCY}$ | Pipelined clock period | 1.991 | – | 2.342 | – | ns |
| $t_{PLCLKMPWH}$ | Pipelined clock minimum pulse width High | 0.785 | – | 0.923 | – | ns |
| $t_{PLCLKMPWL}$ | Pipelined clock minimum pulse width Low | 0.299 | – | 0.352 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.334 | – | 0.393 | ns |
| | Read access time without pipeline register | – | 2.25 | – | 2.647 | ns |
| $t_{ADDRSU}$ | Address setup time | 0.313 | – | 0.368 | – | ns |
| $t_{ADDRHD}$ | Address hold time | 0.274 | – | 0.322 | – | ns |
| $t_{DSU}$ | Data setup time | 0.337 | – | 0.396 | – | ns |
| $t_{DHD}$ | Data hold time | 0.111 | – | 0.13 | – | ns |
| $t_{BLKSU}$ | Block select setup time | 0.207 | – | 0.244 | – | ns |
| $t_{BLKHD}$ | Block select hold time | 0.201 | – | 0.237 | – | ns |
| $t_{BLK2Q}$ | Block select to out disable time (when pipelined register is disabled) | – | 2.25 | – | 2.647 | ns |
| $t_{BLKMPW}$ | Block select minimum pulse width | 0.186 | – | 0.219 | – | ns |
| $t_{RDESU}$ | Read enable setup time (A_WEN, B_WEN = 0) | 0.449 | – | 0.528 | – | ns |
| $t_{RDEHD}$ | Read enable hold time (A_WEN, B_WEN = 0) | 0.167 | – | 0.197 | – | ns |
| $t_{RDPLESU}$ | Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN) | 0.248 | – | 0.291 | – | ns |
| $t_{RDPLEHD}$ | Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN) | 0.102 | – | 0.12 | – | ns |
| $t_{R2Q}$ | Asynchronous reset to output propagation delay | – | 1.506 | – | 1.772 | ns |
| $t_{RSTREM}$ | Asynchronous reset removal time | 0.506 | – | 0.595 | – | ns |
| $t_{RSTREC}$ | Asynchronous reset recovery time | 0.004 | – | 0.005 | – | ns |
| $t_{RSTMPW}$ | Asynchronous reset minimum pulse width | 0.301 | – | 0.354 | – | ns |
| $t_{PLRSTREM}$ | Pipelined register asynchronous reset removal time | -0.279 | – | -0.328 | – | ns |
| $t_{PLRSTREC}$ | Pipelined register asynchronous reset recovery time | 0.327 | – | 0.385 | – | ns |
| $t_{PLRSTMPW}$ | Pipelined register asynchronous reset minimum pulse width | 0.282 | – | 0.332 | – | ns |
| $t_{SRSTSU}$ | Synchronous reset setup time | 0.226 | – | 0.265 | – | ns |
| $t_{SRSTHD}$ | Synchronous reset hold time | 0.036 | – | 0.043 | – | ns |
| $t_{WESU}$ | Write enable setup time (A_WEN, B_WEN = 1) | 0.39 | – | 0.458 | – | ns |
| $t_{WEHD}$ | Write enable hold time (A_WEN, B_WEN = 1) | 0.242 | – | 0.285 | – | ns |

## FPGA Fabric Micro SRAM (uSRAM)

***Table 107 •*** **uSRAM (RAM64x18) in 64x18 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock Period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read Access Time with pipeline Register | – | 0.352 | – | 0.414 | ns |
| | Read Access Time without pipeline Register | – | 1.765 | – | 2.076 | ns |
| $t_{ADDRSU}$ | Read Address Setup Time in Synchronous Mode | 0.279 | – | 0.328 | – | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.667 | – | 1.961 | – | ns |
| $t_{ADDRHD}$ | Read Address Hold Time in Synchronous Mode | 0.052 | – | 0.061 | – | ns |
| | Read Address Hold Time in Asynchronous Mode | 0.033 | – | 0.039 | – | ns |
| $t_{RDENSU}$ | Read Enable Setup Time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read Enable Hold Time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read Block Select Setup Time (with pipelined Register Enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read Block Select Hold Time (with pipelined Register Enabled) | 0.001 | – | 0.001 | – | ns |
| $t_{BLK2Q}$ | Read Block Select to Out Disable Time (when pipelined Registered is Disabled) | – | 2.064 | – | 2.429 | ns |
| $t_{RSTREM}$ | Read Asynchronous Reset Removal Time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read Asynchronous Reset Removal Time (Non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read Asynchronous Reset Recovery Time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read Asynchronous Reset Recovery Time (Non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | – | 0.998 | – | 1.174 | ns |
| | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Disabled) | – | 0.897 | – | 1.055 | ns |
| $t_{SRSTSU}$ | Read Synchronous Reset Setup Time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read Synchronous Reset Hold Time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock Period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write Block Setup Time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write Block Hold Time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write Input Data setup Time | 0.016 | – | 0.019 | – | ns |
| $t_{DINCHD}$ | Write Input Data hold Time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write Address Setup Time | 0.012 | – | 0.014 | – | ns |

**Table 107 • uSRAM (RAM64x18) in 64x18 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{ADDRCHD}$ | Write Address Hold Time | -0.04 | – | -0.047 | – | ns |
| $t_{WECSU}$ | Write Enable Setup Time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write Enable Hold Time | -0.029 | – | -0.034 | – | ns |

**Table 108 • uSRAM (RAM64x16) in 64x16 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.352 | – | 0.414 | ns |
| | Read access time without pipeline register | – | 1.765 | – | 2.076 | ns |
| $t_{ADDRSU}$ | Read address setup time in synchronous mode | 0.279 | – | 0.328 | – | ns |
| | Read address setup time in asynchronous mode | 1.667 | – | 1.961 | – | ns |
| $t_{ADDRHD}$ | Read address hold time in synchronous mode | 0.052 | – | 0.061 | – | ns |
| | Read address hold time in asynchronous mode | 0.033 | – | 0.039 | – | ns |
| $t_{RDENSU}$ | Read enable setup time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read enable hold time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read block select setup time (with pipelined register enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read block select hold time (with pipelined register enabled) | 0.001 | – | 0.001 | – | ns |
| $t_{BLK2Q}$ | Read block select to out disable time (when pipelined register is disabled) | – | 2.064 | | 2.429 | ns |
| $t_{RSTREM}$ | Read asynchronous reset removal time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read asynchronous reset removal time (non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read asynchronous reset recovery time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read asynchronous reset recovery time (non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read asynchronous reset to output propagation delay (with pipelined register enabled) | – | 0.992 | – | 1.167 | ns |
| | Read asynchronous reset to output propagation delay (with pipelined register disabled) | – | 0.893 | – | 1.051 | ns |
| $t_{SRSTSU}$ | Read synchronous reset setup time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read synchronous reset hold time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write block setup time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write block hold time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write input data setup time | 0.016 | – | 0.019 | – | ns |
| $t_{DINCHD}$ | Write input data hold time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write address setup time | 0.012 | – | 0.014 | – | ns |
| $t_{ADDRCHD}$ | Write address hold time | -0.04 | – | -0.047 | – | ns |

**Table 108 • uSRAM (RAM64x16) in 64x16 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WECSU}$ | Write enable setup time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write enable hold time | -0.029 | – | -0.034 | – | ns |

**Table 109 • uSRAM (RAM128x9) in 128x9 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.352 | – | 0.414 | ns |
| | Read access time without pipeline register | – | 1.803 | – | 2.121 | ns |
| $t_{ADDRSU}$ | Read address setup time in synchronous mode | 0.279 | – | 0.328 | – | ns |
| | Read address setup time in asynchronous mode | 1.701 | – | 2.002 | – | ns |
| $t_{ADDRHD}$ | Read address hold time in synchronous mode | 0.096 | – | 0.113 | – | ns |
| | Read address hold time in asynchronous mode | 0.078 | – | 0.091 | – | ns |
| $t_{RDENSU}$ | Read enable setup time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read enable hold time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read block select setup time (with pipelined register enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read block select hold time (with pipelined register enabled) | 0.001 | – | 0.001 | – | ns |
| $t_{BLK2Q}$ | Read block select to out disable time (when pipelined register is disabled) | – | 2.101 | – | 2.471 | ns |
| $t_{RSTREM}$ | Read asynchronous reset removal time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read asynchronous reset removal time (non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read asynchronous reset recovery time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read asynchronous reset recovery time (non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read asynchronous reset to output propagation delay (with pipelined register enabled) | – | 0.99 | – | 1.165 | ns |
| | Read asynchronous reset to output propagation delay (with pipelined register disabled) | – | 0.893 | – | 1.051 | ns |
| $t_{SRSTSU}$ | Read synchronous reset setup time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read synchronous reset hold time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write block setup time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write block hold time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write input data setup time | -0.024 | – | -0.028 | – | ns |
| $t_{DINCHD}$ | Write input data hold time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write address setup time | 0.012 | – | 0.014 | – | ns |
| $t_{ADDRCHD}$ | Write address hold time | 0.068 | – | 0.08 | – | ns |

**Table 109 • uSRAM (RAM128x9) in 128x9 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WECSU}$ | Write enable setup time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write enable hold time | -0.029 | – | -0.034 | – | ns |

**Table 110 • uSRAM (RAM128x8) in 128x8 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | | 0.352 | | 0.414 | ns |
| | Read access time without pipeline register | | 1.803 | | 2.121 | ns |
| $t_{ADDRSU}$ | Read address setup time in synchronous mode | 0.279 | – | 0.328 | – | ns |
| | Read address setup time in asynchronous mode | 1.701 | – | 2.002 | – | ns |
| $t_{ADDRHD}$ | Read address hold time in synchronous mode | 0.096 | – | 0.113 | – | ns |
| | Read address hold time in asynchronous mode | 0.078 | – | 0.091 | – | ns |
| $t_{RDENSU}$ | Read enable setup time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read enable hold time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read block select setup time (with pipelined register enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read block select hold time (with pipelined register enabled) | 0.001 | – | 0.001 | – | ns |
| $t_{BLK2Q}$ | Read block select to out disable time (when pipelined register is disabled) | – | 2.101 | – | 2.471 | ns |
| $t_{RSTREM}$ | Read asynchronous reset removal time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read asynchronous reset removal time (non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read asynchronous reset recovery time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read asynchronous reset recovery time (non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read asynchronous reset to output propagation delay (with pipelined register enabled) | – | 0.99 | – | 1.165 | ns |
| | Read asynchronous reset to output propagation delay (with pipelined register disabled) | – | 0.893 | – | 1.051 | ns |
| $t_{SRSTSU}$ | Read synchronous reset setup time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read synchronous reset hold time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write block setup time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write block hold time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write input data setup time | -0.024 | – | -0.028 | – | ns |
| $t_{DINCHD}$ | Write input data hold time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write address setup time | 0.012 | – | 0.014 | – | ns |
| $t_{ADDRCHD}$ | Write address hold time | 0.068 | – | 0.08 | – | ns |

**Table 110 • uSRAM (RAM128x8) in 128x8 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WECSU}$ | Write enable setup time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write enable hold time | -0.029 | – | -0.034 | – | ns |

**Table 111 • uSRAM (RAM256x4) in 256x4 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.352 | – | 0.414 | ns |
| | Read access time without pipeline register | – | 1.837 | – | 2.161 | ns |
| $t_{ADDRSU}$ | Read address setup time in synchronous mode | 0.279 | – | 0.328 | – | ns |
| | Read address setup time in asynchronous mode | 1.721 | – | 2.025 | – | ns |
| $t_{ADDRHD}$ | Read address hold time in synchronous mode | 0.096 | – | 0.113 | – | ns |
| | Read address hold time in asynchronous mode | 0.078 | – | 0.091 | – | ns |
| $t_{RDENSU}$ | Read enable setup time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read enable hold time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read block select setup time (with pipelined register enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read block select hold time (with pipelined register enabled) | 0.001 | | 0.001 | | ns |
| $t_{BLK2Q}$ | Read block select to out disable time (when pipelined register is disabled) | – | 2.136 | – | 2.513 | ns |
| $t_{RSTREM}$ | Read asynchronous reset removal time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read asynchronous reset removal time (non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read asynchronous reset recovery time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read asynchronous reset recovery time (non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read asynchronous reset to output propagation delay (with pipelined register enabled) | – | 0.99 | – | 1.164 | ns |
| | Read asynchronous reset to output propagation delay (with pipelined register disabled) | – | 0.893 | – | 1.05 | ns |
| $t_{SRSTSU}$ | Read synchronous reset setup time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read synchronous reset hold time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write block setup time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write block hold time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write input data setup time | -0.024 | – | -0.028 | – | ns |
| $t_{DINCHD}$ | Write input data hold time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write address setup time | 0.012 | – | 0.014 | – | ns |
| $t_{ADDRCHD}$ | Write address hold time | 0.084 | – | 0.098 | – | ns |

**Table 111 • uSRAM (RAM256x4) in 256x4 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WECSU}$ | Write enable setup time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write enable hold time | -0.029 | – | -0.034 | – | ns |

**Table 112 • uSRAM (RAM512x2) in 512x2 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.352 | – | 0.414 | ns |
| | Read access time without pipeline register | – | 1.857 | – | 2.184 | ns |
| $t_{ADDRSU}$ | Read address setup time in synchronous mode | 0.279 | – | 0.328 | – | ns |
| | Read address setup time in asynchronous mode | 1.757 | – | 2.067 | – | ns |
| $t_{ADDRHD}$ | Read address hold time in synchronous mode | 0.124 | – | 0.146 | – | ns |
| | Read address hold time in asynchronous mode | 0.087 | – | 0.103 | – | ns |
| $t_{RDENSU}$ | Read enable setup time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read enable hold time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read block select setup time (with pipelined register enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read block select hold time (with pipelined register enabled) | 0.001 | – | 0.001 | – | ns |
| $t_{BLK2Q}$ | Read block select to out disable time (when pipelined register is disabled) | – | 2.158 | – | 2.539 | ns |
| $t_{RSTREM}$ | Read asynchronous reset removal time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read asynchronous reset removal time (non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read asynchronous reset recovery time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read asynchronous reset recovery time (non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read asynchronous reset to output propagation delay (with pipelined register enabled) | – | 0.989 | – | 1.164 | ns |
| | Read asynchronous reset to output propagation delay (with pipelined register disabled) | – | 0.89 | – | 1.047 | ns |
| $t_{SRSTSU}$ | Read synchronous reset setup time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read synchronous reset hold time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write block setup time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write block hold time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write input data setup time | -0.024 | – | -0.028 | – | ns |
| $t_{DINCHD}$ | Write input data hold time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write address setup time | 0.012 | – | 0.014 | – | ns |
| $t_{ADDRCHD}$ | Write address hold time | 0.093 | – | 0.109 | – | ns |

**Table 112 • uSRAM (RAM512x2) in 512x2 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WECSU}$ | Write enable setup time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write enable hold time | -0.029 | – | -0.034 | – | ns |

**Table 113 • uSRAM (RAM1024x1) in 1024x1 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{CY}$ | Read clock period | 0.795 | – | 0.935 | – | ns |
| $t_{CLKMPWH}$ | Read clock minimum pulse width High | 0.281 | – | 0.33 | – | ns |
| $t_{CLKMPWL}$ | Read clock minimum pulse width Low | 0.308 | – | 0.362 | – | ns |
| $t_{PLCY}$ | Read pipeline clock period | 1.89 | – | 2.223 | – | ns |
| $t_{PLCLKMPWH}$ | Read pipeline clock minimum pulse width High | 0.246 | – | 0.29 | – | ns |
| $t_{PLCLKMPWL}$ | Read pipeline clock minimum pulse width Low | 0.281 | – | 0.331 | – | ns |
| $t_{CLK2Q}$ | Read access time with pipeline register | – | 0.352 | – | 0.414 | ns |
| | Read access time without pipeline register | – | 1.885 | – | 2.218 | ns |
| $t_{ADDRSU}$ | Read address setup time in synchronous mode | 0.279 | – | 0.328 | – | ns |
| | Read address setup time in asynchronous mode | 1.786 | – | 2.101 | – | ns |
| $t_{ADDRHD}$ | Read address hold time in synchronous mode | 0.124 | – | 0.146 | – | ns |
| | Read address hold time in asynchronous mode | 0.087 | – | 0.103 | – | ns |
| $t_{RDENSU}$ | Read enable setup time | 0.233 | – | 0.274 | – | ns |
| $t_{RDENHD}$ | Read enable hold time | 0.07 | – | 0.082 | – | ns |
| $t_{BLKSU}$ | Read block select setup time (with pipelined register enabled) | 1.806 | – | 2.125 | – | ns |
| $t_{BLKHD}$ | Read block select hold time (with pipelined register enabled) | 0.001 | – | 0.001 | – | ns |
| $t_{BLK2Q}$ | Read block select to out disable time (when pipelined register is disabled) | – | 2.184 | | 2.57 | ns |
| $t_{RSTREM}$ | Read asynchronous reset removal time (pipelined clock) | -0.001 | – | -0.002 | – | ns |
| | Read asynchronous reset removal time (non-pipelined clock) | 0.029 | – | 0.034 | – | ns |
| $t_{RSTREC}$ | Read asynchronous reset recovery time (pipelined clock) | 0.518 | – | 0.61 | – | ns |
| | Read asynchronous reset recovery time (non-pipelined clock) | 0.08 | – | 0.095 | – | ns |
| $t_{R2Q}$ | Read asynchronous reset to output propagation delay (with pipelined register enabled) | – | 0.989 | – | 1.164 | ns |
| | Read asynchronous reset to output propagation delay (with pipelined register disabled) | – | 0.783 | – | 0.921 | ns |
| $t_{SRSTSU}$ | Read synchronous reset setup time | 0.237 | – | 0.279 | – | ns |
| $t_{SRSTHD}$ | Read synchronous reset hold time | 0.07 | – | 0.083 | – | ns |
| $t_{CCY}$ | Write clock period | 1.415 | – | 1.665 | – | ns |
| $t_{CCLKMPWH}$ | Write clock minimum pulse width High | 0.481 | – | 0.566 | – | ns |
| $t_{CCLKMPWL}$ | Write clock minimum pulse width Low | 0.282 | – | 0.332 | – | ns |
| $t_{BLKCSU}$ | Write block setup time | 0.315 | – | 0.371 | – | ns |
| $t_{BLKCHD}$ | Write block hold time | -0.009 | – | -0.011 | – | ns |
| $t_{DINCSU}$ | Write input data setup time | -0.084 | – | -0.099 | – | ns |
| $t_{DINCHD}$ | Write input data hold time | 0.002 | – | 0.003 | – | ns |
| $t_{ADDRCSU}$ | Write address setup time | 0.012 | – | 0.014 | – | ns |
| $t_{ADDRCHD}$ | Write address hold time | 0.093 | – | 0.109 | – | ns |

**Table 113 • uSRAM (RAM1024x1) in 1024x1 Mode**
**Worst Commercial-Case Conditions: $T_J$ = 85°C, VDD = 1.14 V (continued)**

| Parameter | Description | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{WECSU}$ | Write enable setup time | 0.304 | – | 0.358 | – | ns |
| $t_{WECHD}$ | Write enable hold time | -0.029 | – | -0.034 | – | ns |

# On-Chip Oscillators

Table 114 through Table 116 on page 103 describe the electrical characteristics of the available on-chip oscillators in SmartFusion2 devices.

***Table 114 •*** **Electrical Characteristics of the Crystal Oscillator**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| FXTAL | Operating frequency | | – | 32 | – | KHz | |
| ACCXTAL | Accuracy | High Gain Mode (20 MHz) | | | 0.0047 | % | |
| | | Medium Gain Mode (2 MHz) | | | 0.00105 | % | |
| | | Low Gain Mode (32 KHz) | | | 0.000429 | % | |
| CYCXTAL | Output duty cycle | High Gain Mode (20 MHz) | | 1 | 3 | % | |
| | | Medium Gain Mode (2 MHz) | | 1 | 3 | % | |
| | | Low Gain Mode (32 KHz) | | 1 | 3 | % | |
| JITPERXTAL | Output Period Jitter (peak-to-peak) | High Gain Mode (20 MHz) | | 200 | 300 | ps | |
| | | Medium Gain Mode (2 MHz) | | 1 | 5 | ns | |
| | | Low Gain Mode (32 KHz) | | 150 | 300 | ns | |
| JITCYCXTAL | Output Cycle-to-Cycle Jitter (peak-to-peak) | High Gain Mode (20 MHz) | | 200 | 300 | ps | |
| | | Medium Gain Mode (2 MHz) | | 1 | 5 | ns | |
| | | Low Gain Mode (32 KHz) | | 150 | 300 | ns | |
| IDYNXTAL | Operating current | High Gain Mode (20 MHz) | | | 1.5 | mA | |
| | | Medium Gain Mode (2 MHz) | | | 0.3 | mA | |
| | | Low Gain Mode (32 KHz) | | | 0.044 | mA | |
| VIHXTAL | Input logic level High | | 0.9 x VPP | | | V | |
| VILXTAL | Input logic level Low | | | | 0.1 x VPP | V | |
| SUXTAL | Startup time (w.r.t. stable oscillator output) | High Gain Mode (20 MHz) | | | 0.8 | µs | |
| | | Medium Gain Mode (2 MHz) | | | 4.5 | µs | |
| | | Low Gain Mode (32 KHz) | | | 115 | µs | |

**Table 115 • Electrical Characteristics of the 50 MHz RC Oscillator**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| F50RC | Operating frequency | | – | 50 | – | MHz | |
| ACC50RC | Accuracy | | | 1 | 4 | % | |
| CYC50RC | Output duty cycle | | | 1 | 3 | % | |
| JIT50RC | Output jitter | Period jitter | | 200 | 300 | ps | |
| | | Cycle-to-cycle jitter | | 200 | 300 | ps | |
| IDYN50RC | Operating current | | | 6.5 | | mA | |

**Table 116 • Electrical Characteristics of the 1 MHz RC Oscillator**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| F1RC | Operating frequency | | – | 1 | – | MHz | |
| ACC1RC | Accuracy | | | 1 | 3 | % | |
| CYC1RC | Output duty cycle | | | 1 | 3 | % | |
| JIT1RC | Output jitter | Period jitter | | 10 | 20 | ns | |
| | | Cycle-to-cycle jitter | | 10 | 20 | ns | |
| IDYN1RC | Operating current | | | 0.1 | | mA | |
| SU1RC | Startup time | | | | 17 | µs | |

# Clock Conditioning Circuits (CCC)

***Table 117 •*** **SmartFusion2 CCC/PLL Specification**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $f_{IN\_CCC}$ | 1 | | 200 | MHz | |
| Clock conditioning circuitry output frequency $f_{OUT\_CCC}$ | 20 | | 400 | MHz | |
| Delay increments in programmable delay blocks | | 75 | 100 | ps | |
| Number of programmable values in each programmable delay block | | | 64 | | |
| Acquisition time | | 70 | 100 | µs | |
| Output duty cycle | 48 | | 52 | % | |
| **Spread Spectrum Characteristics** | | | | | |
| Modulation frequency range | 25 | 35 | 50 | kHz | |
| Modulation depth range | 0 | | 1.5 | % | |
| Modulation depth control | | 0.5 | | % | |

**Maximum peak-to-peak period jitter**

| Parameter | Conditions/Package Combinations | | | | | Units | Notes |
|---|---|---|---|---|---|---|---|
| CCC output peak-to-peak period jitter FCCC_OUT | | | | | | | |
| | SSO = 0 | 0 < SSO ≤ 2 | SSO ≤ 4 | SSO ≤ 8 | SSO ≤ 16 | | * |
| 20 MHz to 100 MHz | 110 ps < jitter < ± 1% fOUT_CCC | 150 ps < jitter < ± 1% fOUT_CCC | | | | ps | |
| 100 MHz to 400 MHz | 120 ps < jitter < ± 1% fOUT_CCC | 150 ps < jitter < ± 1% fOUT_CCC | | | 170 ps < jitter < ± 1% fOUT_CCC | ps | |

*Note: * SSO Data is based on LVCMOS 2.5 V MSIOD Bank I/Os on the M2S050 FG896 Package.*

# JTAG

***Table 118 •*** **JTAG 1532**
**Worst Industrial-Case Conditions: TJ = 100°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | –1 | Std. | Units | Notes |
|---|---|---|---|---|---|
| $t_{DISU}$ | Test data input setup time | -0.3 | -0.26 | ns | |
| $t_{DIHD}$ | Test data input hold time | 2.08 | 2.45 | ns | |
| $t_{TMSSU}$ | Test mode select setup time | 0.29 | 0.35 | ns | |
| $t_{TMDHD}$ | Test mode select hold time | 0.17 | 0.2 | ns | |
| $t_{TCK2Q}$ | Clock to Q (data out) | 7.86 | 9.25 | ns | |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 8.87 | 10.44 | ns | |
| $F_{TCKMAX}$ | TCK maximum frequency | 25 | 21.25 | MHz | |

*Note: *For specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.*

# Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 14 on page 107.

***Table 119 •*** **SPI Characteristics**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Type | Max | | |
| sp1 | SPI_[0\|1]_CLK minimum period | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | | - | - | 12 | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | | - | - | 24.1 | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | | - | - | 48.2 | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | | - | - | 0.1 | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | | - | - | 0.19 | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | | - | - | 0.39 | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | | - | - | 0.77 | µs | |
| sp2 | SPI_[0\|1]_CLK minimum pulse width high | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | | - | - | 6 | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | | - | - | 12.05 | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | | - | - | 24.1 | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | | - | - | 0.05 | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | | - | - | 0.095 | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | | - | - | 0.195 | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | | - | - | 0.385 | µs | |
| sp3 | SPI_[0\|1]_CLK minimum pulse width low | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | | - | - | 6 | ns | |
| | SPI_[0\|1]_CLK = PCLK/4 | | - | - | 12.05 | ns | |
| | SPI_[0\|1]_CLK = PCLK/8 | | - | - | 24.1 | ns | |
| | SPI_[0\|1]_CLK = PCLK/16 | | - | - | 0.05 | µs | |
| | SPI_[0\|1]_CLK = PCLK/32 | | - | - | 0.095 | µs | |
| | SPI_[0\|1]_CLK = PCLK/64 | | - | - | 0.195 | µs | |
| | SPI_[0\|1]_CLK = PCLK/128 | | - | - | 0.385 | µs | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%-90%) 1 | I/O Configuration: LVCMOS 2.5 V- 8 mA<br>AC Loading: 35 pF<br>Test Conditions: Typical Voltage, 25°C | - | 2.77 | - | ns | 1 |

*Notes:*

1. *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 Microcontroller Subsystem User Guide.*

**Table 119 • SPI Characteristics**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**
**(continued)**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Type | Max | | |
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%-90%) 1 | I/O Configuration: LVCMOS 2.5 V- 8 mA<br>AC Loading: 35 pF<br>Test Conditions: Typical Voltage, 25°C | - | 2.906 | - | ns | 1 |
| sp6 | Data from master (SPI_[0\|1]_DO) setup time | | - | - | 1 | pclk cycles | 2 |
| sp7 | Data from master (SPI_[0\|1]_DO) hold time | | - | - | 1 | pclk cycles | 2 |
| sp8 | SPI_[0\|1]_DI setup time | | - | - | 1 | pclk cycles | 2 |
| sp9 | SPI_[0\|1]_DI hold time | | - | - | 1 | pclk cycles | 2 |

*Notes:*

1. *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 Microcontroller Subsystem User Guide.*

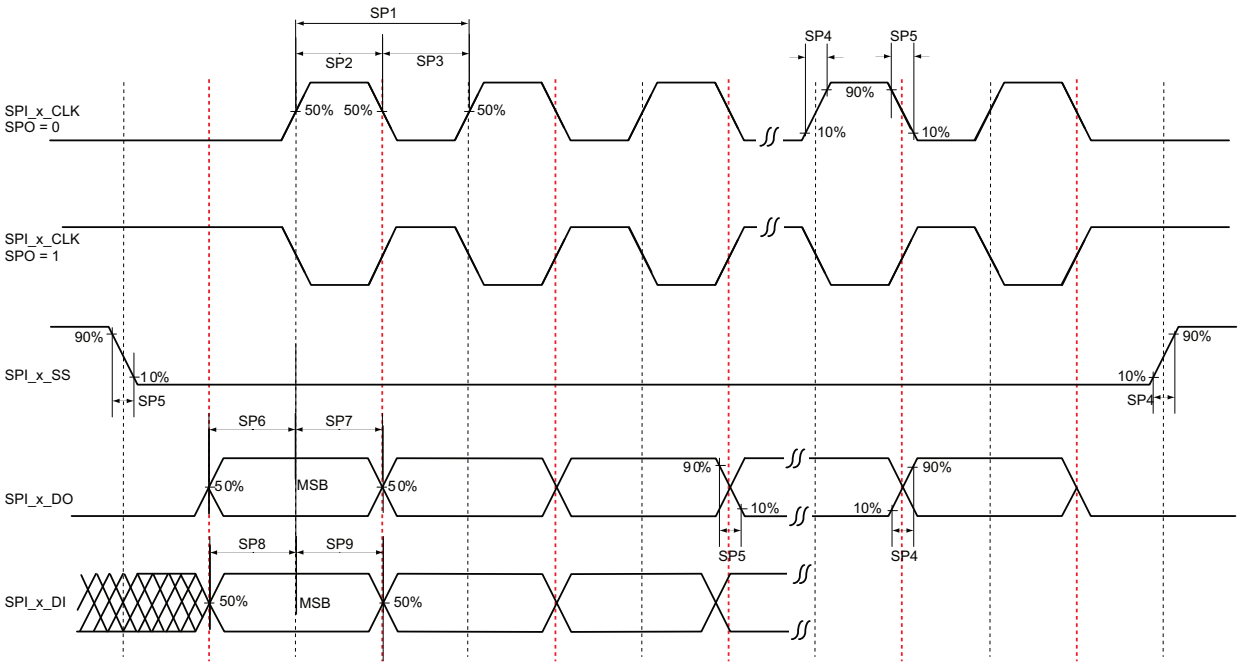



**Figure 14 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

# System Controller SPI Characteristics

.

***Table 120 •*** **System Controller SPI Characteristics**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Type | Max | | |
| sp1 | SC_SPI_SCK minimum period | | - | - | 20 | ns | |
| sp2 | SC_SPI_SCK minimum pulse width high | | - | - | 10 | ns | |
| sp3 | SC_SPI_SCK minimum pulse width low | | - | - | 10 | ns | |
| sp4 | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1 | IO Configuration: LVTTL 3.3V- 20mA<br>AC Loading: 35pF<br>Test Conditions: Typical Voltage, 25C | - | 1.239 | - | ns | 1 |
| sp5 | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1 | IO Configuration: LVTTL 3.3V- 20mA<br>AC Loading: 35pF<br>Test Conditions: Typical Voltage, 25C | - | 1.245 | - | ns | 1 |
| sp6 | Data from master (SC_SPI_SDO) setup time | | - | - | 160 | ns | |
| sp7 | Data from master (SC_SPI_SDO) hold time | | - | - | 160 | ns | |
| sp8 | SC_SPI_SDI setup time | | - | - | 20 | ns | |
| sp9 | SC_SPI_SDI hold time | | - | - | 20 | ns | |

*Notes:*

1. *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx. Please use the supported I/O Configurations for System Controller SPI on Table 121Table 121 • Supported I/O Configurations for System Controller SPI (MSIO Bank Only).*

***Table 121 •*** **Supported I/O Configurations for System Controller SPI (MSIO Bank Only)**

| Voltage Supply | I/O Drive Configuration | Units | Notes |
|---|---|---|---|
| 3.3V | 20 | mA | |
| 2.5V | 16 | mA | |
| 1.8V | 12 | mA | |
| 1.5V | 8 | mA | |
| 1.2V | 4 | mA | |

# Inter-Integrated Circuit ($I^2C$) Characteristics

This section describes the DC and switching of the $I^2C$ interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 15 on page 110.

***Table 122 •*** **$I^2C$ Characteristics**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Definition | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| VIL | Input low voltage | Refer to the "Single-Ended I/O Standards" section on page 22 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive. | –0.3 | – | 0.8 | V | |
| VIH | Input high voltage | Refer to the "Single-Ended I/O Standards" section on page 22 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive. | 2 | – | 3.45 | V | |
| VHYS | Hysteresis of Schmitt triggered inputs for VDDI > 2 V | Refer to Table 13 on page 21 for more information. | 0.05 * VDDI | – | – | V | |
| IIL | Input current high | Refer to the "Single-Ended I/O Standards" section on page 22 for more information. | – | – | 10 | µA | |
| IIH | Input current low | Refer to the "Single-Ended I/O Standards" section on page 22 for more information. | – | – | 10 | µA | |
| VOL | Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V | Refer to the "Single-Ended I/O Standards" section on page 22 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive. | – | – | 0.4 | V | |
| Cin | Pin capacitance | VIN = 0, f = 1.0 MHz | – | – | 10 | pF | |
| $t_{OF}$ | Output fall time from VIHMin to VILMax | VIHmin to VILMax, Cload = 400 pF | – | 21.04 | – | ns | 1 |
| | | VIHmin to VILMax, Cload = 100 pF | – | 5.556 | – | ns | |
| $t_{OR}$ | Output rise time from VILMax to VIHMin | VILMax to VIHmin, Cload = 400pF | – | 19.887 | – | ns | 1 |
| | | VILMax to VIHmin, Cload = 100pF | – | 5.218 | – | ns | |
| Rpull-up | Output buffer maximum pull-down resistance | | – | – | 50 | Ohms | 2, 3 |
| Rpull-down | Output buffer maximum pull-up resistance | | – | – | 131.25 | Ohms | 2, 4 |

*Notes:*

1. *These values are provided for MSIO Bank - LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*

**Table 122 • I²C Characteristics**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V (continued)**

| Parameter | Definition | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| Dmax | Maximum data rate | Fast mode | – | – | 400 | Kbps | |
| | | Standard mode | – | – | 100 | Kbps | |
| $t_{FILT}$ | Pulse width of spikes which must be suppressed by the input filter | Fast mode | – | 50 | – | ns | |

*Notes:*

1. *These values are provided for MSIO Bank - LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*

**Table 123 • I²C Switching Characteristics**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Definition | Conditions | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | | |
| $t_{LOW}$ | Low period of I2C_x_SCL | – | 1 | – | 1 | – | pclk cycles | |
| $t_{HIGH}$ | High period of I2C_x_SCL | – | 1 | – | 1 | – | pclk cycles | |
| $t_{HD;STA}$ | START hold time | – | 1 | – | 1 | – | pclk cycles | |
| $t_{SU;STA}$ | START setup time | – | 1 | – | 1 | – | pclk cycles | |
| $t_{HD;DAT}$ | DATA hold time | – | 1 | – | 1 | – | pclk cycles | |
| $t_{SU;DAT}$ | DATA setup time | – | 1 | – | 1 | – | pclk cycles | |
| $t_{SU;STO}$ | STOP setup time | – | 1 | – | 1 | – | pclk cycles | |

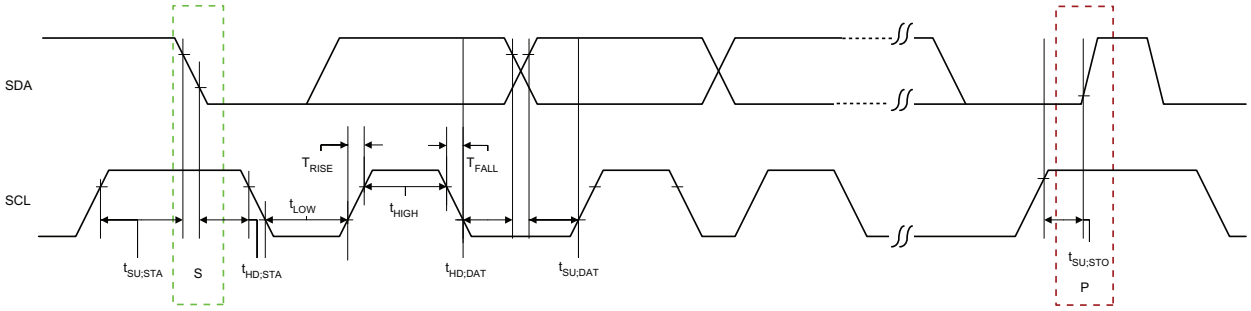



**Figure 15 • I²C Timing Parameter Definition**

# Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each SmartFusion mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

***Table 124 •*** **Mathblocks with All Registers Used**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{MISU}$ | Input, control register setup time | 0.149 | | 0.176 | | ns | |
| $t_{MIHD}$ | Input, control register hold time | 0.08 | | 0.094 | | ns | |
| $t_{MOCDINSU}$ | CDIN input setup time | 1.68 | | 1.976 | | ns | |
| $t_{MOCDINHD}$ | CDIN input hold time | -0.419 | | -0.493 | | ns | |
| $t_{MSRSTENSU}$ | Synchronous reset/enable setup time | 0.185 | | 0.218 | | ns | |
| $t_{MSRSTENHD}$ | Synchronous reset/enable hold time | 0.011 | | 0.013 | | ns | |
| $t_{MARSTREM}$ | Asynchronous reset removal time | 0 | | 0 | | ns | |
| $t_{MARSTREC}$ | Asynchronous reset recovery time | 0.088 | | 0.104 | | ns | |
| $t_{MOCQ}$ | Output register clock to out delay | | 0.232 | | 0.273 | ns | |
| $t_{MCLKMP}$ | CLK minimum period | 2.245 | | 2.641 | | ns | |

***Table 125 •*** **Mathblock with Input Bypassed and Output Registers Used**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{MOSU}$ | Output register setup time | 2.294 | | 2.699 | | ns | |
| $t_{MOHD}$ | Output register hold time | -0.444 | | -0.522 | | ns | |
| $t_{MOCDINSU}$ | CDIN input setup time | 1.68 | | 1.976 | | ns | |
| $t_{MOCDINHD}$ | CDIN input hold time | -0.419 | | -0.493 | | ns | |
| $t_{MSRSTENSU}$ | Synchronous reset/enable setup time | 0.115 | | 0.136 | | ns | |
| $t_{MSRSTENHD}$ | Synchronous reset/enable hold time | 0.011 | | 0.013 | | ns | |
| $t_{MARSTREM}$ | Asynchronous reset removal time | 0 | | 0 | | ns | |
| $t_{MARSTREC}$ | Asynchronous reset recovery time | 0.014 | | 0.017 | | ns | |
| $t_{MOCQ}$ | Output register clock to out delay | | 0.232 | | 0.273 | ns | |
| $t_{MCLKMP}$ | CLK minimum period | 2.179 | | 2.563 | | ns | |

***Table 126 •*** **Mathblock with Input Register Used and Output in Bypass Mode**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{MISU}$ | Input register setup time | 0.149 | | 0.176 | | ns | |
| $t_{MIHD}$ | Input register hold time | 0.08 | | 0.094 | | ns | |
| $t_{MSRSTENSU}$ | Synchronous reset/enable setup time | 0.185 | | 0.218 | | ns | |
| $t_{MSRSTENHD}$ | Synchronous reset/enable hold time | -0.012 | | -0.014 | | ns | |
| $t_{MARSTREM}$ | Asynchronous reset removal time | -0.005 | | -0.005 | | ns | |
| $t_{MARSTREC}$ | Asynchronous reset recovery time | 0.088 | | 0.104 | | ns | |
| $t_{MICQ}$ | Input register clock to output delay | | 2.52 | | 2.964 | ns | |
| $t_{MCDIN2Q}$ | CDIN to output delay | | 1.951 | | 2.295 | ns | |

***Table 127 •*** **Mathblock with Input and Output in Bypass Mode**

| Parameter | Description | –1 | | Std. | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{MIQ}$ | Input to output delay | | 2.568 | | 3.022 | ns | |
| $t_{MCDIN2Q}$ | CDIN to output delay | | 1.951 | | 2.295 | ns | |

***Table 128 •*** **Flash*Freeze Entry and Exit Times**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Symbols | Parameter | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| **TFF_ENTRY** | Entry Time | eNVM and MSS PLL=ON | | | 150 | us | |
| | | eNVM and MSS PLL=OFF | | | 200 | us | |
| **TFF_EXIT** | Exit Time with Respect to MSS PLL Lock | eNVM and MSS PLL=ON during F*F | | | 100 | us | |
| | | eNVM=ON and MSS PLL=OFF during F*F and MSS PLL turned back on at exit | | | 120 | us | |
| | | eNVM and MSS PLL=OFF during F*F and both are turned back on at exit | | | 200 | us | |
| | | eNVM=OFF and MSS PLL=ON during F*F and eNVM turned back on at exit | | | 200 | us | |
| | Exit Time with Respect to Fabric PLL Lock | eNVM and MSS PLL=ON during F*F | | | 1.5 | µs | |
| | | eNVM and MSS PLL=OFF during F*F and both are turned back on at exit | | | 1.5 | µs | |
| | Exit Time with Respect to Fabric buffer output | eNVM and MSS PLL=ON during F*F | | | 15 | us | |
| | | eNVM and MSS PLL=OFF during F*F and both are turned back on at exit | | | 55 | us | |

# PCIe Electrical and Timing AC and DC Characteristics

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The SmartFusion2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

***Table 129 •*** **Transmitter Parameters**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Description | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| VTX-DIFF-PP | Differential swing PCIe Gen 1 and 2 | 0.8 | – | 1.2 | V | |
| VTX-CM-AC-P | Output common mode voltage PCIe Gen 1 | – | – | 20 | mV | |
| VTX-CM-AC-PP | Output common mode voltage PCIe Gen 2 | – | – | 100 | mV | |
| VTX-RISE-FALL | Rise and fall time (20% to 80%) PCIe Gen 1 | 0.125 | – | – | UI | |
| | Rise and fall time (20% to 80%) PCIe Gen 2 | 0.15 | – | – | UI | |
| ZTX-DIFF-DC | Output impedance – differential | 80 | – | 120 | ohm | |
| LTX-SKEW | Lane-to-lane TX skew within a SERDES block PCIe Gen 1 | – | – | 500 ps + 2 UI | ps | |
| | Lane-to-lane TX skew within a SERDES block PCIe Gen 2 | – | – | 500 ps +4 UI | ps | |
| RLTX-DIFF | Return loss differential mode PCIe Gen 1 | –10 | – | – | dB | |
| | Return loss differential mode PCIe Gen 2 | –10 (min.) 0.05 – 1.25 GHz – 8 (min.) 1.25 – 2.5 GHz | | | dB | |
| RLTX-CM | Return loss common mode PCIe Gen 1 and 2 | –6 | – | – | dB | |
| | Transmit PLL lock time from reset | – | – | 10 | µs | |

***Table 130 •*** **Receiver Parameters**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| VRX-DIFF-PP-CC | Input levels PCIe Gen 1 | 0.175 | – | 1.2 | V | |
| | Input levels PCIe Gen 2 | 0.12 | – | 1.2 | V | |
| VRX-CM-DC-P | Input common mode range (DC coupled)<br>Note: PCIe standard mandates AC coupling | NA | NA | NA | - | |
| VRX-CM-AC-P | Input common mode range (AC coupled) | – | – | 150 | mV | |
| VRX-DIFF-PP-CC | Differential input sensitivity PCIe Gen 1 | 0.175 | – | – | mV | |
| | Differential input sensitivity PCIe Gen 2 | 0.12 | – | – | mV | |
| ZRX-DIFF-DC | Differential input termination | 80 | 100 | 120 | Ohms | |
| REXT | External calibration resistor | 1,188 | 1,200 | 1,212 | Ohms | |
| | CDR relock time from reset | – | – | 15 | µs | |
| RLRX-DIFF | Return loss differential mode PCIe Gen 1 | –10 | – | – | dB | |
| | Return loss differential mode PCIe Gen 2 | –10 (min.) 0.05 – 1.25 GHz –8 (min.) 1.25 – 2.5 GHz | | | dB | |
| RLRX-CM | Return loss common mode PCIe Gen 1 and 2 | –6 | – | – | dB | |
| | CID limit (set by 8B/10B coding, not the receiver PLL) | | | 4 | UI | |
| VRX-IDLE-DET-DIFF-PP | Signal detect limit | 65 | | 175 | mV | |

**Table 131 • SERDES Reference Clock AC Specifications**
**Worst-Case Industrial Conditions: $T_J$ = 100°C, VDD = 1.14 V**

| Symbols | Description | Conditions | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| FREFCLK | Reference Clock Frequency | | 100 | | 160 | MHz | |
| TRISE | Reference Clock Rise Time | | 0.6 | | 4 | V/ns | |
| TFALL | Reference Clock Fall Time | | 0.6 | | 4 | V/ns | |
| TCYC | Reference Clock Duty Cycle | | 40 | | 60 | % | |
| Mmrefclk | Reference Clock Mismatch | | -300 | | 300 | ppm | |
| SSCref | Reference Spread Spectrum Clock | | 0 | | 5000 | ppm | |

# Datasheet Information

## List of Changes

The following table lists critical changes that were made in each revision of the datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 5 (January 2014) | Updated the following tables: Table 1 through Table 8, Table 10 through Table 12, Table 14, Table 15, Table 17 through Table 23, Table 25 through Table 127 (SARs 47054, 48244, 49714, 49767, 50214, 51188, 51625, 52203, and 53473).<br>References to MDDR_PLL_xxx are replaced with MSS_MDDR_PLL_xxx (SAR 53294).<br>Removed all references to the datasheet for VDD_2V5 (SAR 53293).<br>Removed HSTL15 and SSTL18 support from MSIO/MSIOD (SAR 52773).<br>Tables 94, 95, 96, 100, 120, and 121 are New | NA |
| Revision 4 (June 2013) | The M2S050T device status was changed from Advance to Preliminary in the "SmartFusion2 Device Status" table (SAR 47026). | 1 |
| | VDD_2V5 and PLL0_PLL1_MDDR_VDDA were added to Table 1 • Absolute Maximum Ratings and Table 2 • Recommended Operating Conditions. The minimum for FDDR_PLL_VDDA was corrected from –0.5 to –0.3 (SARs 47054, 47055, and 48490). | 9, 10 |
| | VDD_2V5, PLL0_PLL1_MDDR_VDDA, and programming junction temperature were added to Table 2 • Recommended Operating Conditions (SARs 45620, 47054, 47055). | 10 |
| | The "Power Supply Sequencing and Power-On Reset (Commercial and Industrial)" section will become part of a user's guide. The sections "I/O Power", "Power Consumption of Various Internal Resources", and "Power Methodology" were moved to the user's guide (SAR 45904). | N/A |
| | Information was added to Table 4 • Package Thermal Resistance (SAR 47026). | 12 |
| | The Power Methodology section was deleted. This information will become part of a new user's guide (SAR 46973). | N/A |
| | Table 5 • Quiescent Supply Current Characteristics and Table 6 • Quiescent Supply Current are new (SARs 45673 and 48135). | 14 |
| | Updated Figure 1 • Timing Model (SAR 47527). | 15 |
| | Values were added to Table 8 • Timing Model Parameters (SAR 47026). | 16 |
| | Values were updated for Table 7 • Average Temperature and Voltage Derating Factors for Fabric Timing Delays (SARs 47026 and 48280). | 15 |
| | Timing tables in the "User I/O Characteristics" section were updated extensively with available data (SAR 47026). | 17 |
| | Updated the Min value of VIH(dc) for the SSTL2 DC Input Voltage Specifications in Table 47 • DDR1/SSTL2 DC Voltage Specification (SAR 48244). | 43 |
| | Diagrams in the "I/O Register Specifications" section are new (SAR 47026). | 66 |
| | A reference to the *SmartFusion2 Macro Library Guide* was added. | 77 |
| | Updated Table 90 • Input DDR Propagation Delays, Table 91 • Output DDR Propagation Delays, Table 92 • Combinatorial Cell Propagation Delays, and Table 93 • Register Delays (SAR 48280). | 73, 76, 77, and 79 |

| Revision | Changes | Page |
|---|---|---|
| Revision 4 (contd.) | Updated Table 114 • Electrical Characteristics of the Crystal Oscillator and Table 115 • Electrical Characteristics of the 50 MHz RC Oscillator (SAR 44895). Table 115 • Electrical Characteristics of the 50 MHz RC Oscillator was renamed to remove the reference to a 25 MHz oscillator (SAR 44859). | 102 and 103 |
| | The "Mathblock Timing Characteristics" section and "PCIe Electrical and Timing AC and DC Characteristics" section are new (SARs 40276) | 111, 113 |
| | Added Table 128 • Flash*Freeze Entry and Exit Times (SAR 46455) and Table 131 • SERDES Reference Clock AC Specifications. | 112 |
| Revision 3 (February 2013) | SmartFusion2 product brief and pin information has been removed from the datasheet and published in separate documents: *SmartFusion2 Product Brief* and *SmartFusion2 Pin Descriptions* (SAR 45184). | N/A |
| Revision 2 (February 2013) | Table 1 • Absolute Maximum Ratings and Table 2 • Recommended Operating Conditions were updated with the new pin names and latest values (SAR 45081). | 9, 10 |
| | The storage temperature minimum value was added to Table 1 • Absolute Maximum Ratings, including a note with references to additional tables (SAR 44887). | 9 |
| | In EQ 1 , $T_J - \theta_A$ was corrected to $T_J - T_A$ (SAR 44109). | 11 |
| | Timing tables were updated with respect to slew and configuration. AC and DC specifications were placed in separate tables. Values were added to replace TBD in a number of tables in the "User I/O Characteristics" section (SAR 44471). | 17 |
| | The termination scheme for the differential I/O test setup in the "Output Buffer and AC Loading" section was corrected (SAR 43591). | 18 |
| | The worst commercial-case conditions for Table 22 • LVCMOS 2.5 V Receiver Characteristics were changed from VDDI = 3.0 V to VDDI = 2.375 V (SAR 44471). | 25 |
| | The following tables were revised to remove typical and minimum Fmax values and change maximum Fmax values (SAR 44471):<br>Table 63 • LVDS DC Voltage Specification<br>Table 77 • Mini-LVDS DC Voltage Specification<br>Table 81 • RSDS DC Voltage Specification | <br>55<br>61<br>63 |
| | Table 102 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 through Table 105 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1 are new (SAR 44471). | 83 to 86 |
| | Table 107 • uSRAM (RAM64x18) in 64x18 Mode through Table 112 • uSRAM (RAM512x2) in 512x2 Mode are new (SAR 44471). | 88 to 98 |
| Revision 1 (January 2013) | Table 1 • Absolute Maximum Ratings is new. In Table 2 • Recommended Operating Conditions, the expression "VDDI0" in the values for VREFx was corrected to "VDDIx." VCCENVM was corrected to VPPNVM (SAR 42461). VDDIx was defined differently for different types of I/O banks (SAR 43850). | 9, 10 |
| | The "Power Supply Sequencing and Power-On Reset (Commercial and Industrial)" section was revised to correct the available ramp rate options from "50 µs, 100 µs, 1 ms, and 100 ms" to "50 µs, 1 ms, 10 ms, and 100 ms." Each selection represents the maximum ramp rate to apply to VDD and VPP. The user can set the ramp rate setting using Libero SOC (SARs 41970, 42401). | 11 |
| | The units for input leakage current (IIL/IIH) were corrected from mA to µA in the DC voltage tables (SAR 43848). | 22 to 35 |
| | A note to reference IBIS models for a detailed I/V curve was added to transmitter drive strength tables for LVTTL/LVCMOS 3.3 V through LVCMOS 1.2 V (SAR 42171). For more information, refer to the *IBIS Models: Background and Usage* application note. | 23 to 35 |

# Datasheet Categories

## Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion2 Device Status" table on page 1 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

## Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

## Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

## Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

## Production

This version contains information that is considered to be final.

# Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

# Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.



51700115-5/01.14