

CRYSTAL OSCILLATOR
SPXO

SG-710 series

- Frequency range : 1.8 MHz to 125 MHz
- Supply voltage : 3.3 V or 5.0 V
- Function : Output enable (OE) PTK,PHK
Standby ($\overline{ST}$) ECK
- Thickness : 1.3 mm Typ.



Actual size

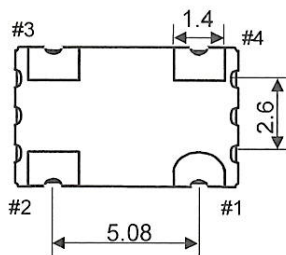
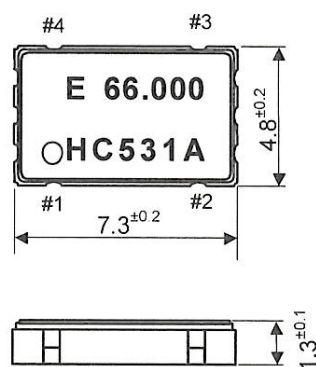


Specifications (characteristics)

Item	Symbol	Specifications			Remarks
		SG-710PTK	SG-710PHK	SG-710ECK	
Output frequency range	f_0	1.8 MHz to 50 MHz	1.8 MHz to 80 MHz	1.8 MHz to 125 MHz	
Supply voltage	V_{CC}	5.0 V ± 0.5 V			3.3 V ± 0.3 V
Temperature range	Storage temperature	-55 °C to +125 °C			Store as bare product after unpacking
	Operating temperature				
Frequency tolerance	$f_{tol}(osc)$	S: $\pm 25 \times 10^{-6}$, B: $\pm 50 \times 10^{-6}$, C: $\pm 100 \times 10^{-6}$ L: $\pm 50 \times 10^{-6}$, M: $\pm 100 \times 10^{-6}$			-10 °C to +70 °C -40 °C to +85 °C
Current consumption	I_{CC}	13 mA Max.	15 mA Max.	8 mA Max.	$f_0 \leq 25$ MHz, No load condition. (ECK: $f_0 \leq 32$ MHz)
		24 mA Max.	26 mA Max.	15 mA Max.	$f_0 \leq 50$ MHz, No load condition
		—	34 mA Max.	18 mA Max.	$f_0 \leq 67$ MHz, No load condition
		—	40 mA Max.	22 mA Max.	$f_0 \leq 80$ MHz, No load condition
		—	—	30 mA Max.	$f_0 \leq 125$ MHz, No load condition
Output disable current	I_{dis}	6 mA Max.	5 mA Max.	—	$f_0 \leq 25$ MHz, OE=GND (PTK, PHK)
		12 mA Max.	10 mA Max.	—	$f_0 \leq 50$ MHz, OE=GND (PTK, PHK)
		—	13 mA Max.	—	$f_0 \leq 67$ MHz, OE=GND (PTK, PHK)
		—	16 mA Max.	—	$f_0 \leq 80$ MHz, OE=GND (PTK, PHK)
Stand-by current	I_{std}	—	—	13 μ A Max.	$\overline{ST}$ =GND(ECK)
Symmetry	SYM	—	45 % to 55 %	45 % to 55 %	1.8 MHz $\leq f_0 \leq 50$ MHz, $L_{CMOS}=15$ pF(ECK), 50 % V_{CC}
		45 % to 55 %	40 % to 60 %	40 % to 60 %	50 MHz $< f_0 \leq 125$ MHz, $L_{CMOS}=15$ pF(ECK), 50 % V_{CC}
High output voltage	V_{OH}	2.4 V Min.	$V_{CC}-0.5$ V Min.	90 % V_{CC} Min.	1.4 V level, $L_{TTL}=10TTL$
Low output voltage	V_{OL}	0.4 V Max.	0.5 V Max.	10 % V_{CC} Max.	
Output load condition(TTL)	L_{TTL}	10 TTL Max.	10 TTL Max.	—	
Output load condition(CMOS)	L_{CMOS}	15 pF Max.	50 pF Max.	15 pF Max.	
Output enable / disable input voltage	V_{IH} V_{IL}	2.0 V Min. 0.8 V Max.	2.0 V Min. 0.8 V Max.	70 % V_{CC} Min. 30 % V_{CC} Max.	OE terminal (PTK, PHK) $\overline{ST}$ terminal (ECK)
Output rise and fall time	t_r / t_f	— 5 ns Max.	5 ns Max. —	6 ns Max. —	CMOS load: 10 % V_{CC} to 90 % V_{CC} level TTL load: 0.4 V to 2.4 V level
Oscillation start up time	t_{osc}	10 ms Max.			Time at minimum supply voltage to be 0 s
Frequency aging	f_{aging}	$\pm 5 \times 10^{-6}$ / year Max.			+25 °C, $V_{CC}=5.0$ V / 3.3 V, First year.

External dimensions

(Unit:mm)



Pin map

Pin	Connection
1	OE or $\overline{ST}$
2	GND
3	OUT
4	V_{CC}

Note.

OE pin (PTK, PHK)

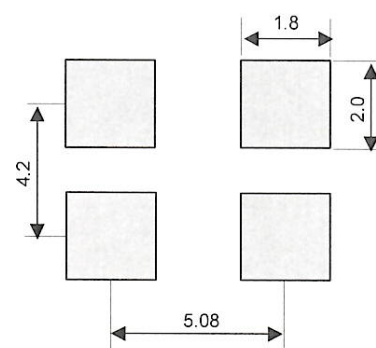
OE pin = HIGH or "open" : Specified frequency output.

OE pin = LOW : Output is high impedance.

 $\overline{ST}$ pin (ECK) $\overline{ST}$ pin = HIGH or "open" : Specified frequency output. $\overline{ST}$ pin = LOW : Output is high impedance, oscillation stops.

Footprint (Recommended)

(Unit:mm)



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