

N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (mA)	Q _g (Typ.)
20	0.396 at V _{GS} = 4.5 V	600	0.75
	0.456 at V _{GS} = 2.5 V	500	
	0.546 at V _{GS} = 1.8 V	350	
	1.100 at V _{GS} = 1.5 V	50	

FEATURES

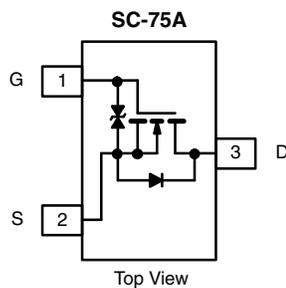
- TrenchFET® Power MOSFET: 1.2 V Rated
- 100 % R_g Tested
- Gate-Source ESD Protected: 1000 V
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load/Power Switching for Portable Devices
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits



Ordering Information:
Si1012CR-T1-GE3 (Lead (Pb)-free and Halogen-free)

Marking Code: K

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	0.63 ^{a, b}
		T _A = 70 °C	0.5 ^{a, b}
Pulsed Drain Current (t = 300 μs)	I _{DM}	2	A
Continuous Source-Drain Diode Current	I _S	0.2 ^{a, b}	A
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	0.24 ^{a, b}
		T _A = 70 °C	0.15 ^{a, b}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	t ≤ 5 s	R _{thJA}	440	530	°C/W
	Steady State		540	650	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
b. t = 5 s.

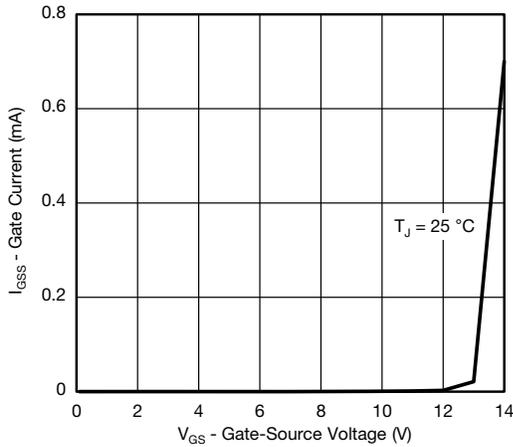
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		17		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 1.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 30	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	2			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 0.6\text{ A}$		0.330	0.396	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 0.3\text{ A}$		0.380	0.456	
		$V_{GS} = 1.8\text{ V}, I_D = 0.3\text{ A}$		0.420	0.546	
		$V_{GS} = 1.5\text{ V}, I_D = 0.05\text{ A}$		0.720	1.100	
Forward Transconductance	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 0.5\text{ A}$		7.5		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		43		pF
Output Capacitance	C_{oss}			14		
Reverse Transfer Capacitance	C_{rss}			8		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 0.6\text{ A}$		1.3	2	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 0.6\text{ A}$		0.75	1.2	
Gate-Source Charge	Q_{gs}			0.15		
Gate-Drain Charge	Q_{gd}			0.13		
Gate Resistance	R_g	$f = 1\text{ MHz}$	2.4	12.2	24.4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 20\text{ }\Omega$ $I_D = 0.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		11	20	ns
Rise Time	t_r			16	24	
Turn-Off Delay Time	$t_{d(off)}$			26	39	
Fall Time	t_f			11	20	
Drain-Source Body Diode Characteristics						
Pulse Diode Forward Current ^a	I_{SM}				2	A
Body Diode Voltage	V_{SD}	$I_S = 0.5\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 0.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		10	15	ns
Body Diode Reverse Recovery Charge	Q_{rr}			2	4	nC
Reverse Recovery Fall Time	t_a			5		ns
Reverse Recovery Rise Time	t_b			5		

Notes:

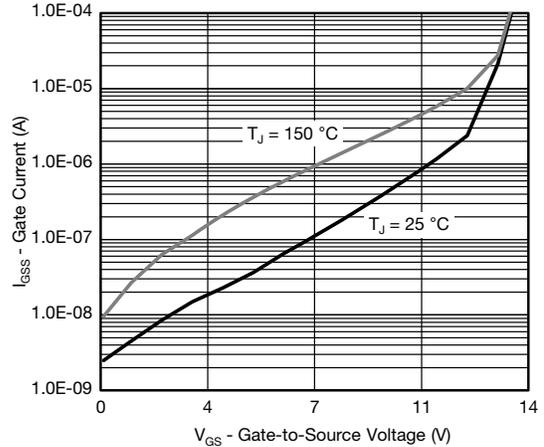
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

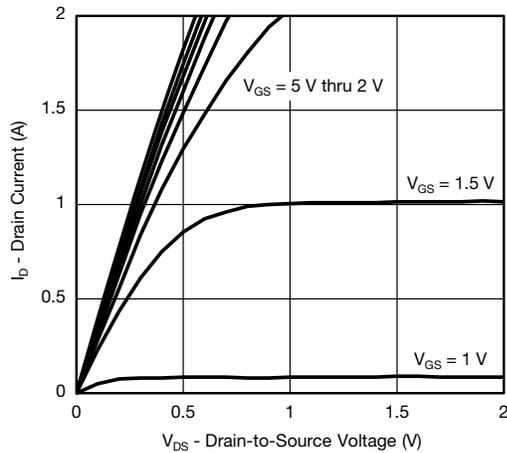
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



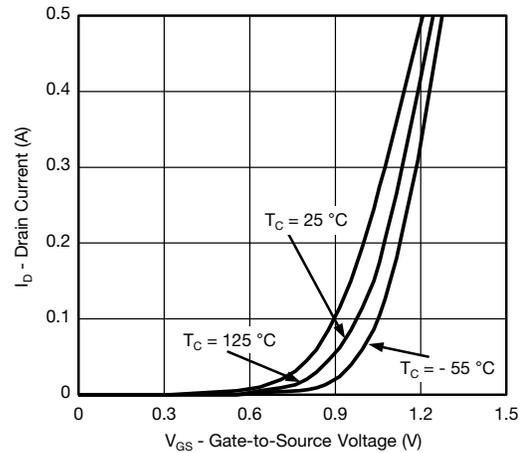
Gate Current vs. Gate-Source Voltage



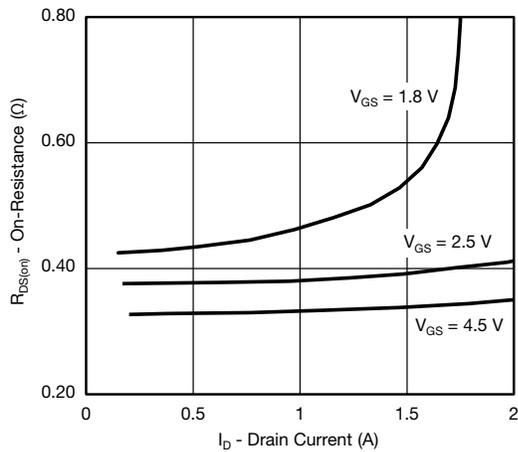
Gate Current vs. Gate-Source Voltage



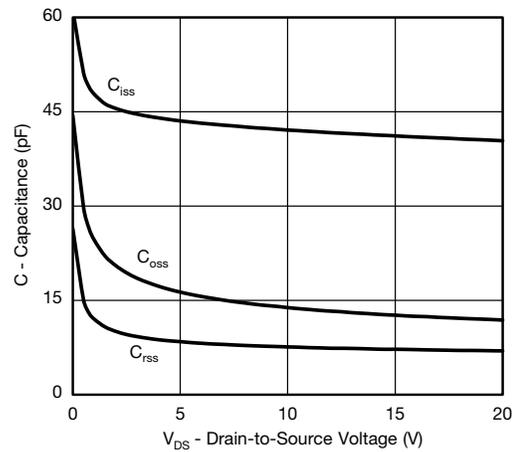
Output Characteristics



Transfer Characteristics

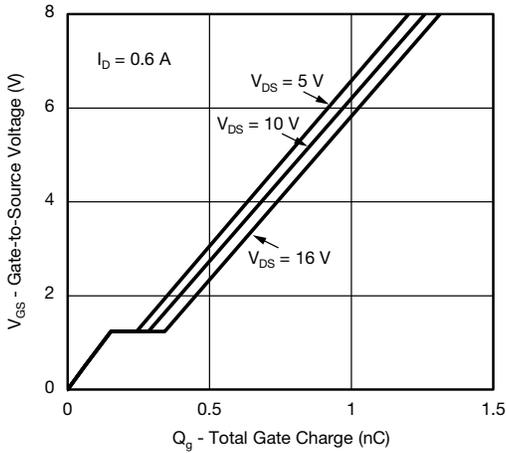


On-Resistance vs. Drain Current

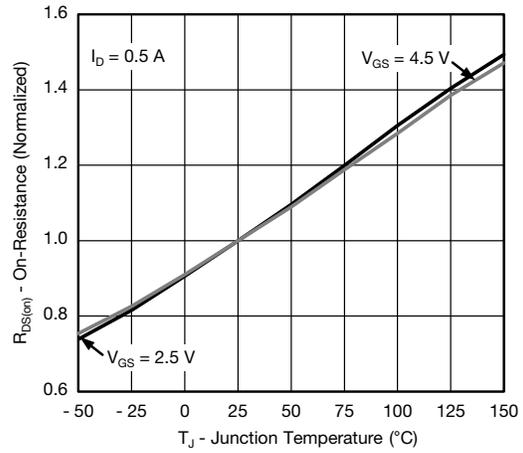


Capacitance

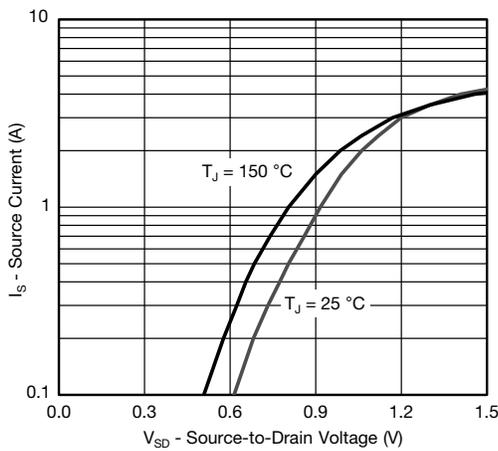
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



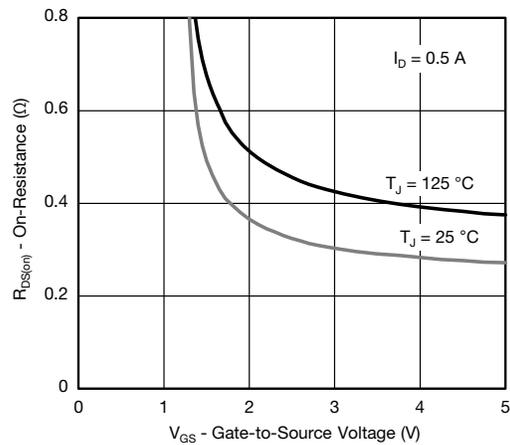
Gate Charge



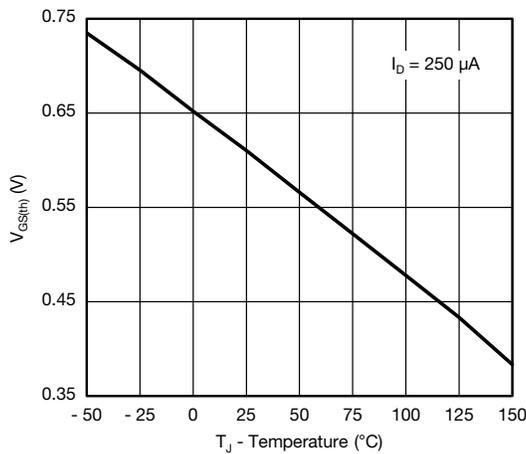
On-Resistance vs. Junction Temperature



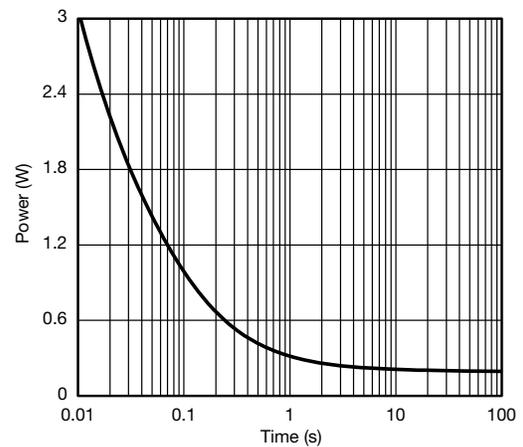
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

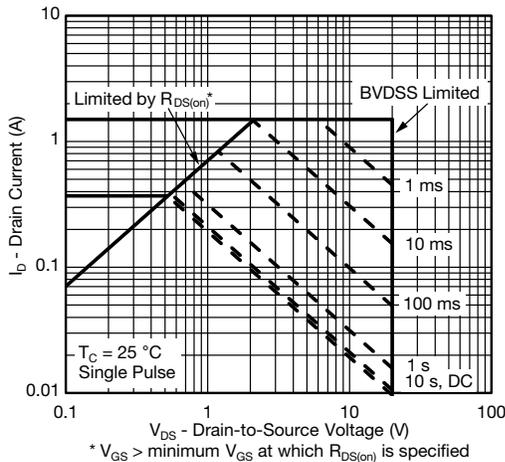


Threshold Voltage

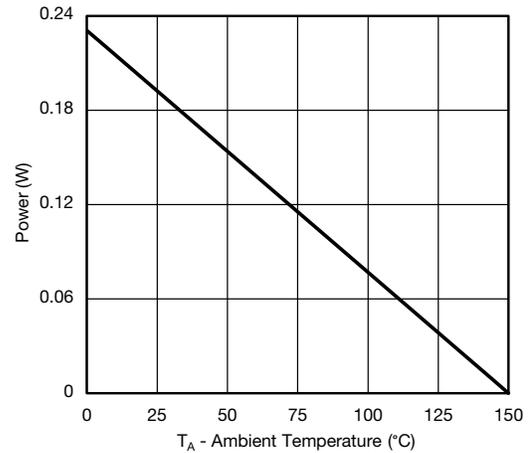


Single Pulse Power, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

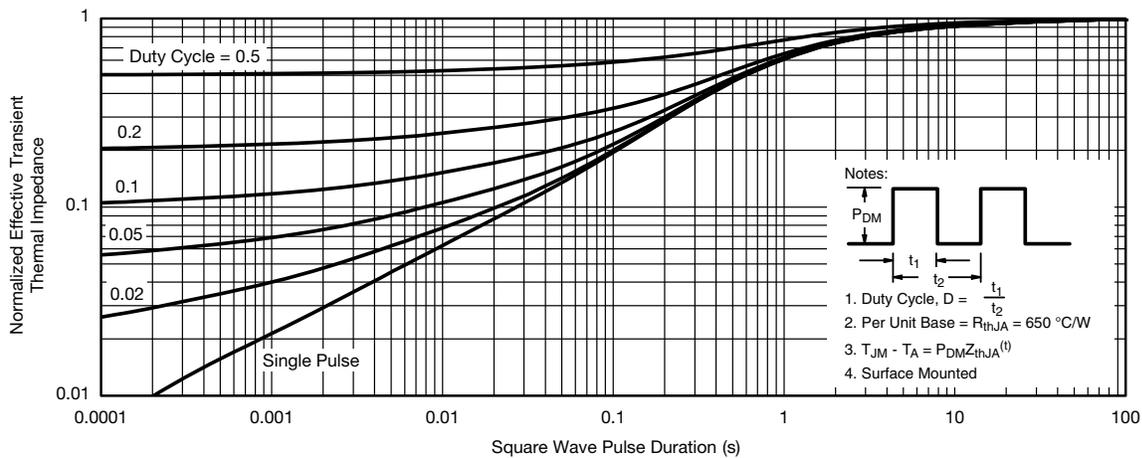


Safe Operating Area, Junction-to-Ambient



Power Derating, Junction-to-Ambient

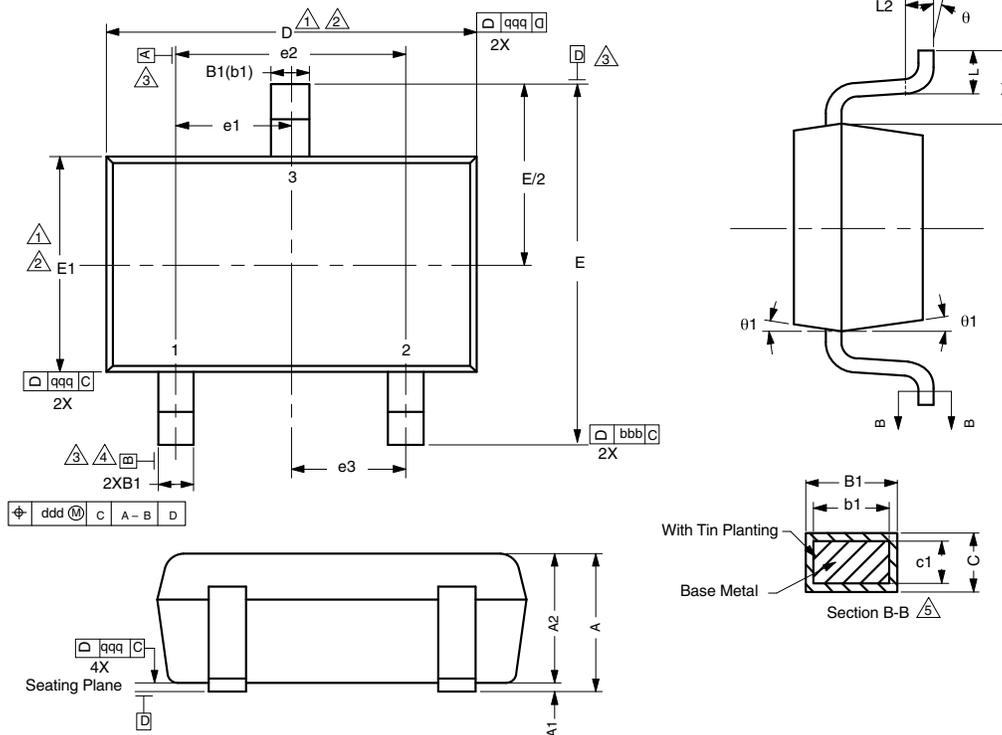
* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67519.

SC-75A: 3-LEADS



Notes

Dimensions in millimeters will govern.

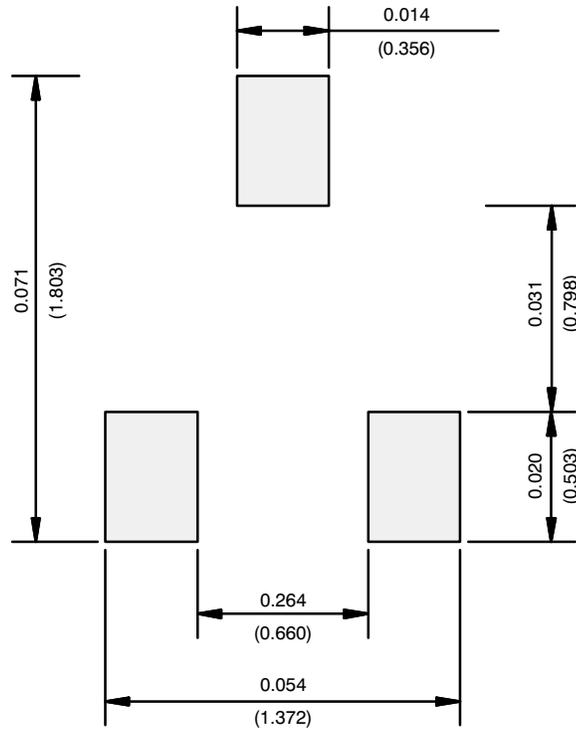
1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. Datums A, B and D to be determined 0.10 mm from the lead tip.
4. Terminal positions are shown for reference only.
5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	-	0.80	
A ₁	0.00	-	0.10	
A ₂	0.65	0.70	0.80	
B ₁	0.19	-	0.24	5
b ₁	0.17	-	0.21	
c	0.13	-	0.15	5
c ₁	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E ₁	0.66	0.76	0.86	1, 2
e ₁	0.50 BSC			
e ₂	1.00 BSC			
e ₃	0.50 BSC			
L	0.15	0.205	0.30	
L ₁	0.40 REF			
L ₂	0.15 BSC			
θ	0°	-	8°	
θ ₁	4°	-	10°	

ECN: E11-2210-Rev. D, 08-Aug-11
DWG: 5868

RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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