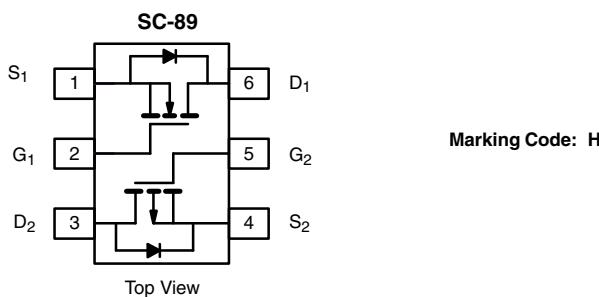


Complementary N- and P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (mA)
N-Channel	60	1.40 at V _{GS} = 10 V	500
		3 at V _{GS} = 4.5 V	200
P-Channel	- 60	4 at V _{GS} = - 10 V	- 500
		8 at V _{GS} = - 4.5 V	- 25



Ordering Information: Si1029X-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Very Small Footprint
- High-Side Switching
- Low On-Resistance: N-Channel, 1.40 Ω
P-Channel, 4 Ω
- Low Threshold: ± 2 V (typ.)
- Fast Switching Speed: 15 ns (typ.)
- Gate-Source ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits

APPLICATIONS

- Replace Digital Transistor, Level-Shifter
- Battery Operated Systems
- Power Supply Converter Circuits

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter	Symbol	N-Channel		P-Channel		Unit
		5 s	Steady State	5 s	Steady State	
Drain-Source Voltage	V _{DS}	60		- 60		V
Gate-Source Voltage	V _{GS}	± 20				
Continuous Drain Current (T _J = 150 °C) ^a	I _D	320	305	- 200	- 190	mA
		230	220	- 145	- 135	
Pulsed Drain Current ^b	I _{DM}	650		- 650		mA
Continuous Source Current (Diode Conduction) ^a	I _S	450	380	- 450	- 380	
Maximum Power Dissipation ^a	P _D	280	250	280	250	mW
		145	130	145	130	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000				V

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 10 \mu\text{A}$	N-Ch	60			V
		$V_{GS} = 0 \text{ V}$, $I_D = -10 \mu\text{A}$	P-Ch	-60			
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	N-Ch	1		2.5	
		$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	P-Ch	-1		-3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 5 \text{ V}$	N-Ch			± 50	nA
		$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 10 \text{ V}$	P-Ch			± 100	
		$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$	N-Ch			± 150	
		$V_{DS} = -50 \text{ V}$, $V_{GS} = 0 \text{ V}$	P-Ch			± 200	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 85^\circ\text{C}$	N-Ch			10	
		$V_{DS} = -50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 85^\circ\text{C}$	P-Ch			-25	
		$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 85^\circ\text{C}$	N-Ch			100	
		$V_{DS} = -50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 85^\circ\text{C}$	P-Ch			-250	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} = 10 \text{ V}$, $V_{GS} = 4.5 \text{ V}$	N-Ch	500			mA
		$V_{DS} = -10 \text{ V}$, $V_{GS} = -4.5 \text{ V}$	P-Ch	-50			
		$V_{DS} = 7.5 \text{ V}$, $V_{GS} = -4.5 \text{ V}$	N-Ch	800			
		$V_{DS} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$	P-Ch	-600			
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$, $I_D = 200 \text{ mA}$	N-Ch			3	Ω
		$V_{GS} = -4.5 \text{ V}$, $I_D = -25 \text{ mA}$	P-Ch			8	
		$V_{GS} = 10 \text{ V}$, $I_D = 500 \text{ mA}$	N-Ch			1.40	
		$V_{GS} = -10 \text{ V}$, $I_D = -500 \text{ mA}$	P-Ch			4	
		$V_{GS} = 10 \text{ V}$, $I_D = 500 \text{ mA}$, $T_J = 125^\circ\text{C}$	N-Ch			2.50	
		$V_{GS} = -10 \text{ V}$, $I_D = -500 \text{ mA}$, $T_J = 125^\circ\text{C}$	P-Ch			6	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}$, $I_D = 200 \text{ mA}$	N-Ch		200		ms
		$V_{DS} = -10 \text{ V}$, $I_D = -100 \text{ mA}$	P-Ch		100		
Diode Forward Voltage ^a	V_{SD}	$I_S = 200 \text{ mA}$, $V_{GS} = 0 \text{ V}$	N-Ch			1.4	V
		$I_S = -200 \text{ mA}$, $V_{GS} = 0 \text{ V}$	P-Ch			-1.4	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 250 \text{ mA}$	N-Ch		750		pC
Gate-Source Charge	Q_{gs}		P-Ch		1700		
Gate-Drain Charge	Q_{gd}		N-Ch		75		
Gate-Drain Charge	Q_{gd}		P-Ch		260		
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	N-Ch		225		pF
Output Capacitance	C_{oss}		P-Ch		460		
Reverse Transfer Capacitance	C_{rss}		N-Ch		30		
Reverse Transfer Capacitance	C_{rss}		P-Ch		23		
Turn-On Time ^c	t_{ON}	N-Channel $V_{DD} = 30 \text{ V}$, $R_L = 150 \Omega$ $I_D \geq 200 \text{ mA}$, $V_{GEN} = 10 \text{ V}$, $R_g = 10 \Omega$	N-Ch		6		ns
Turn-On Time ^c	t_{OFF}		P-Ch		10		
Turn-Off Time ^c	t_{OFF}		N-Ch		3		
Turn-Off Time ^c	t_{OFF}		P-Ch		5		

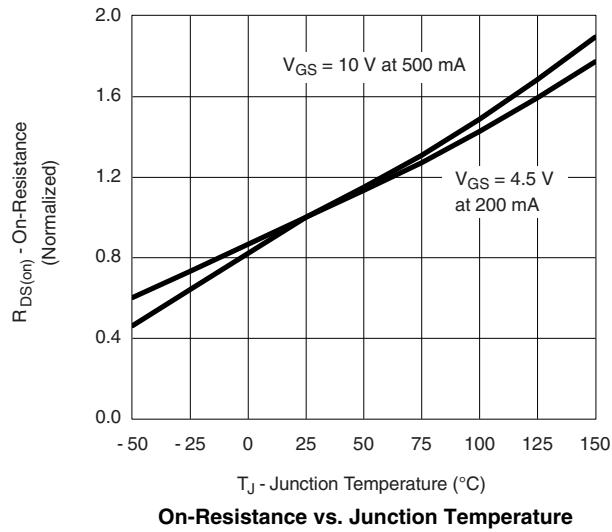
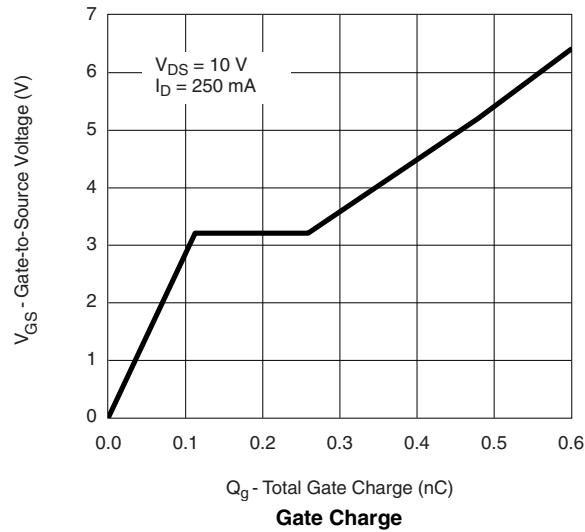
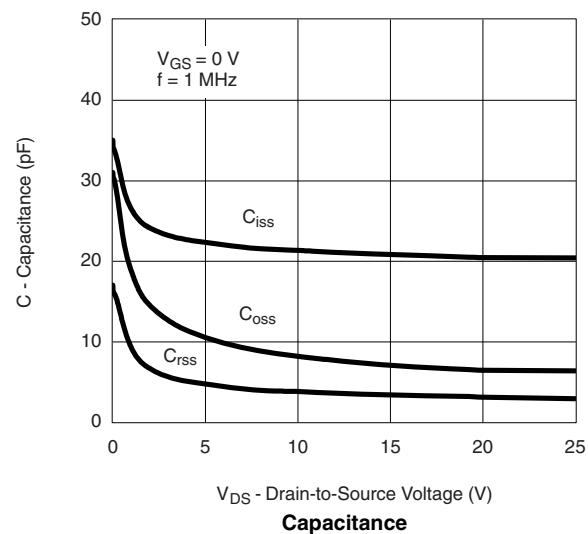
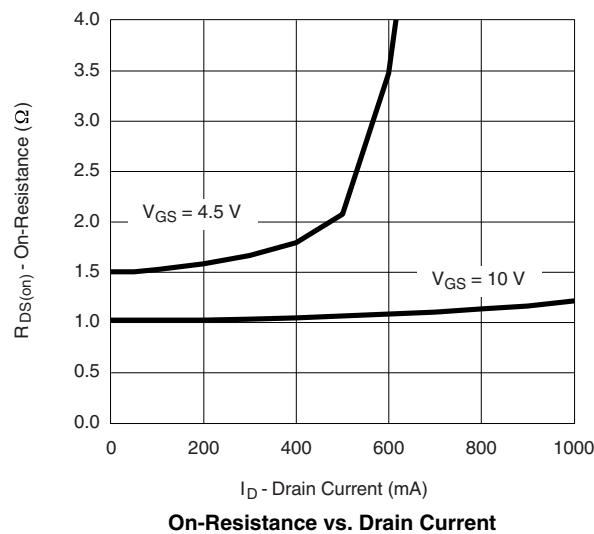
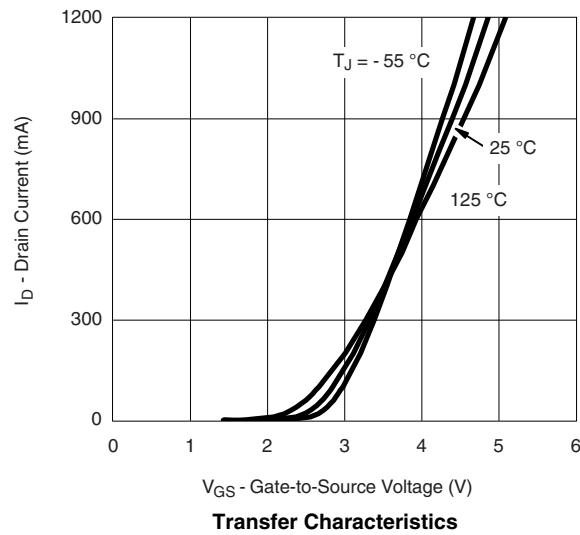
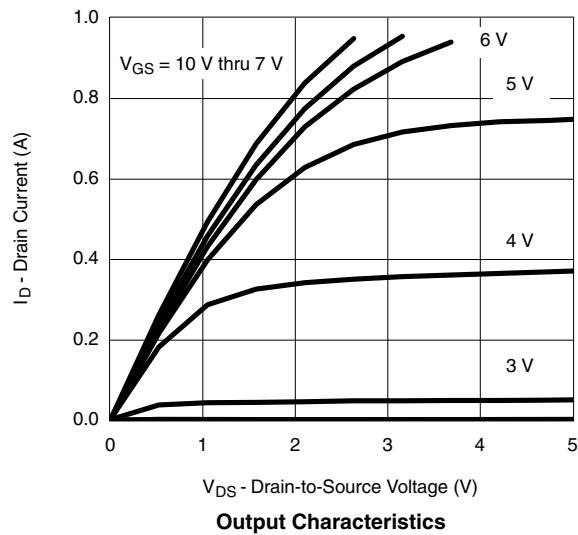
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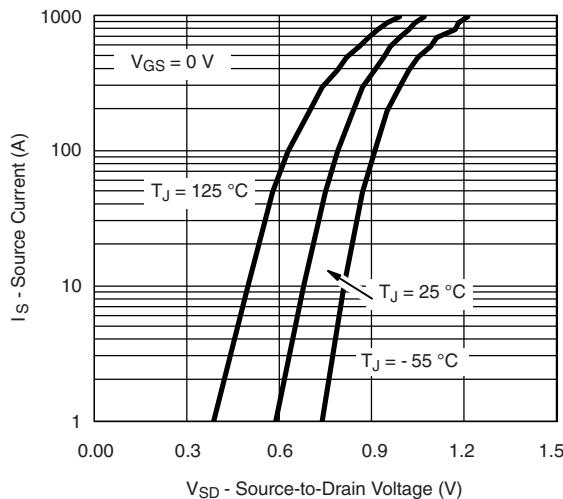
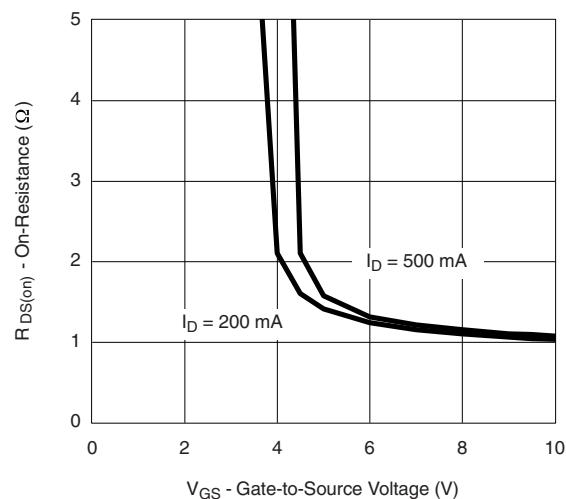
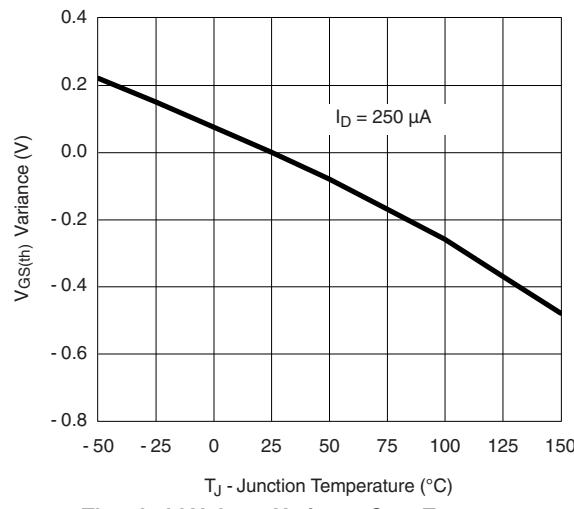
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

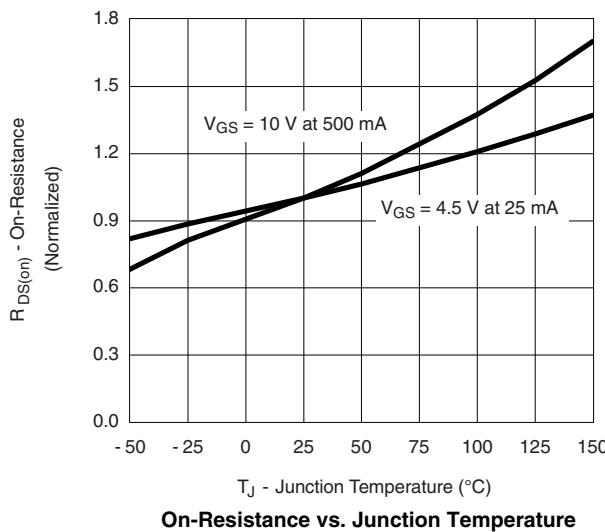
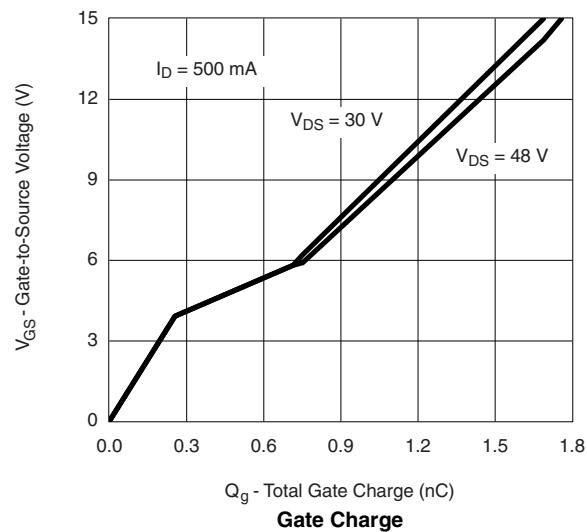
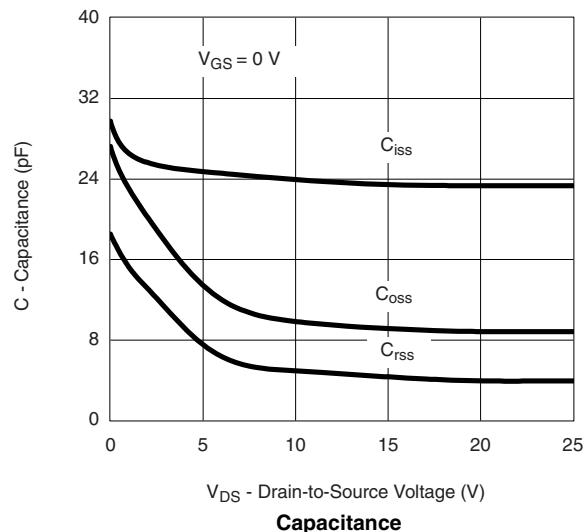
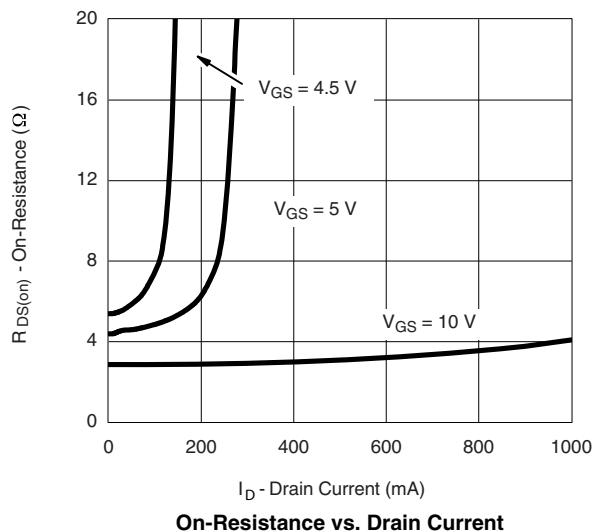
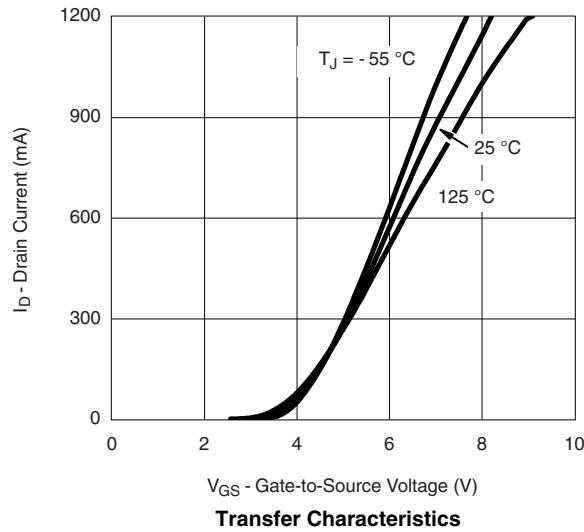
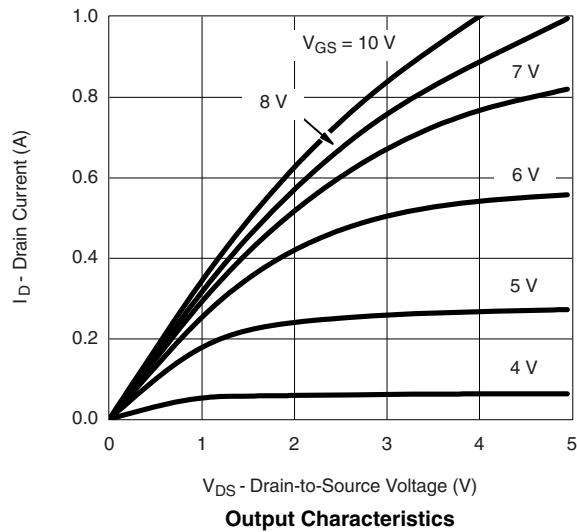
b. Guaranteed by design, not subject to production testing.

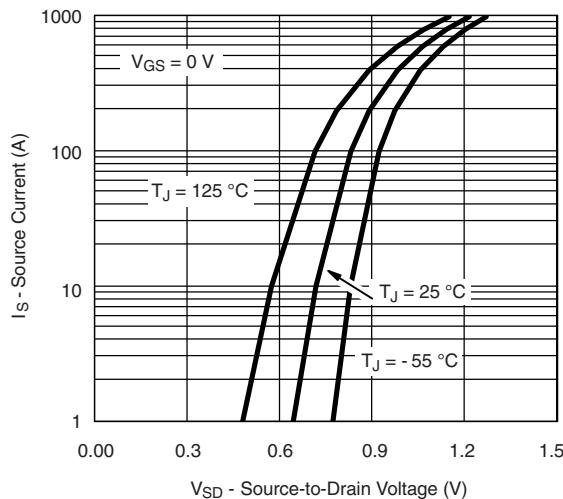
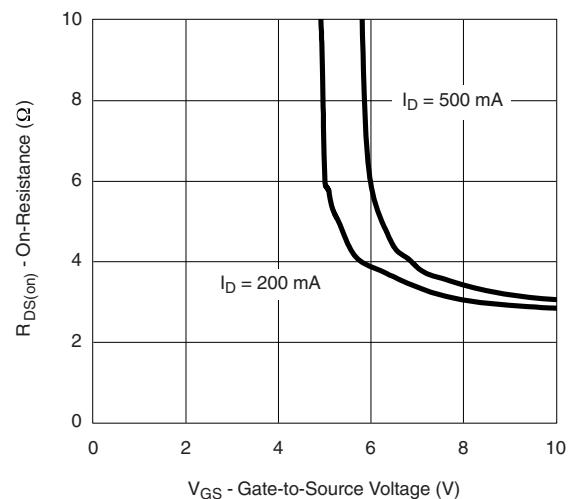
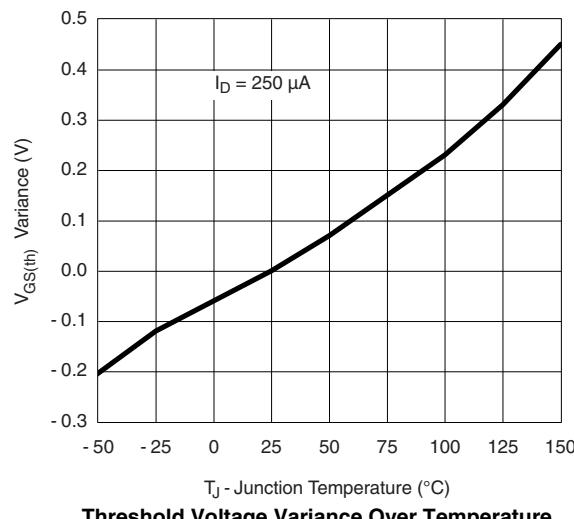
c. Switching time is essentially independent of operating temperature.

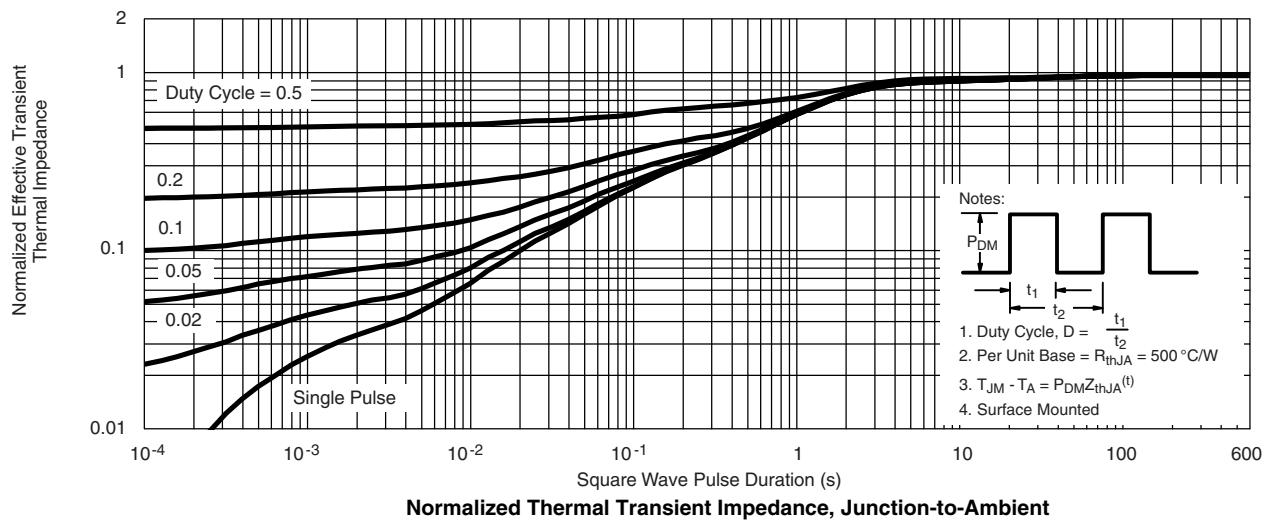
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)


N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage Variance Over Temperature**

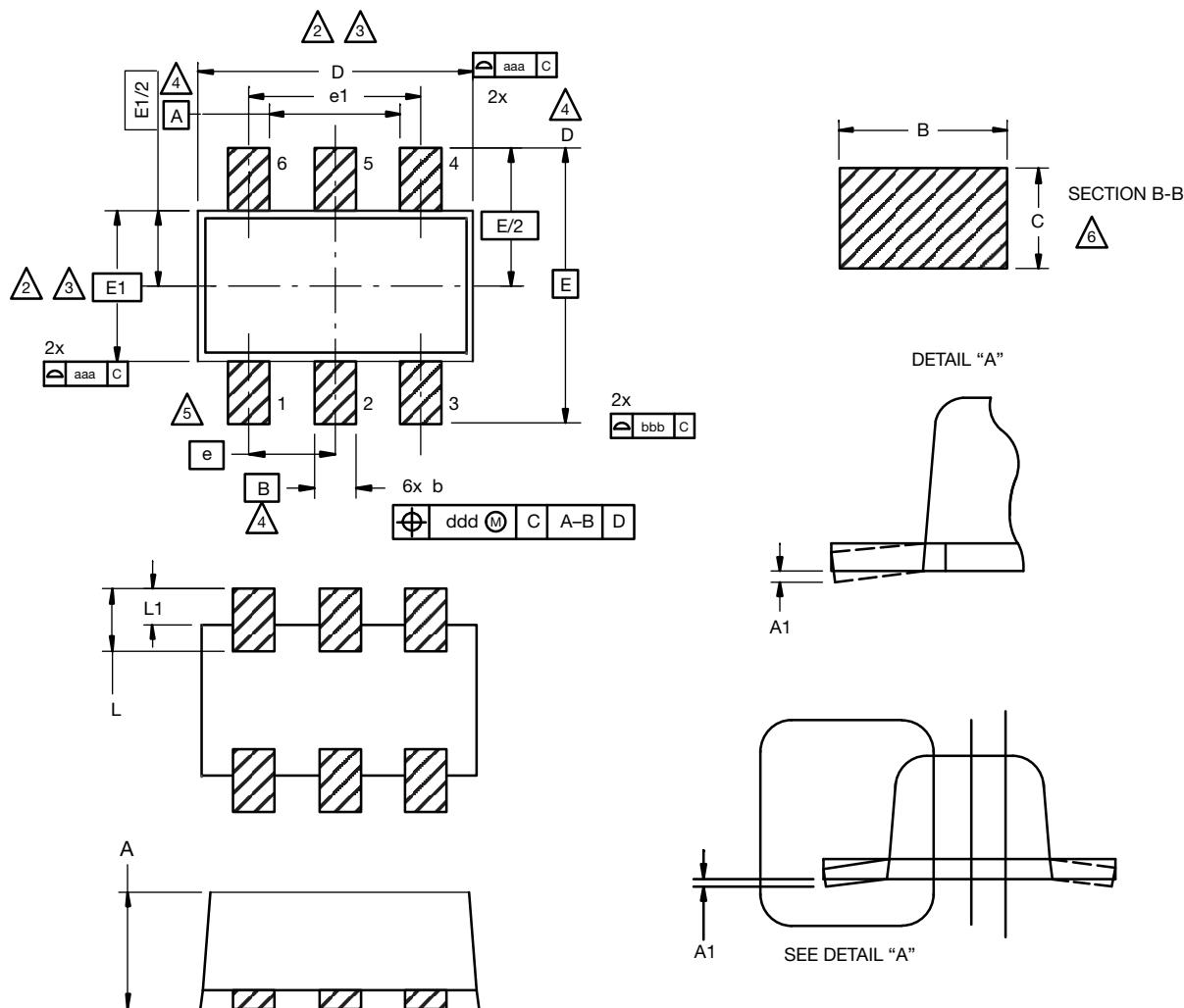
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)


P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage Variance Over Temperature**

N- OR P-CHANNEL TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)


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SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

 Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

 Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

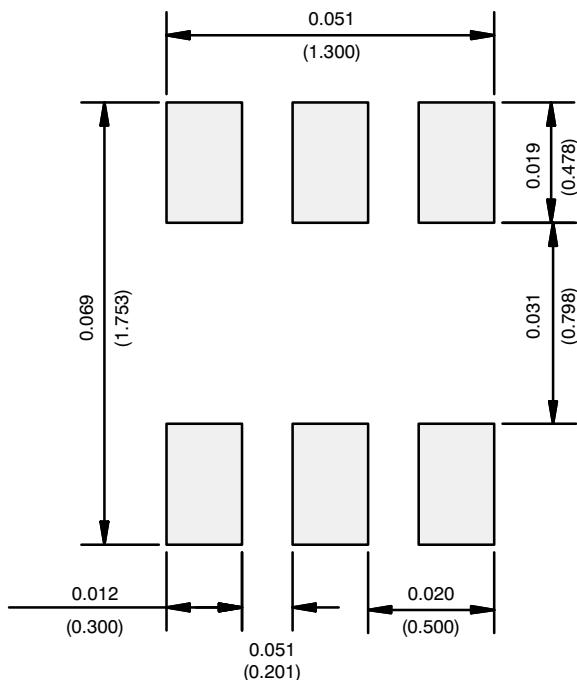
 Datums A, B and D to be determined 0.10 mm from the lead tip.

 Terminal numbers are shown for reference only.

 These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

C14-0439-Rev. C, 11-Aug-14
DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

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