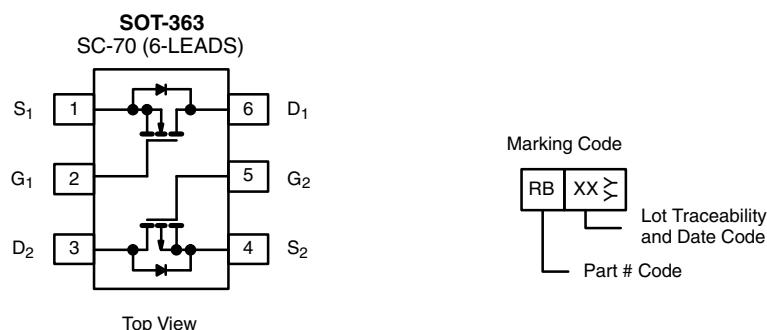


Complementary Low-Threshold MOSFET Pair

PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.385 at $V_{GS} = 4.5$ V	0.70
		0.630 at $V_{GS} = 2.5$ V	0.54
P-Channel	- 8	0.600 at $V_{GS} = - 4.5$ V	- 0.60
		0.850 at $V_{GS} = - 2.5$ V	- 0.50
		1.200 at $V_{GS} = - 1.8$ V	- 0.42

FEATURES

- TrenchFET® Power MOSFET
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



Ordering Information: Si1555DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)						
Parameter	Symbol	N-Channel		P-Channel		Unit
		5 s	Steady State	5 s	Steady State	
Drain-Source Voltage	V_{DS}		20		- 8	V
Gate-Source Voltage	V_{GS}		± 12		± 8	
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D ($T_A = 25$ °C)	± 0.70	± 0.66	- 0.60	- 0.57	A
	I_D ($T_A = 85$ °C)	± 0.50	± 0.48	- 0.43	- 0.41	
Pulsed Drain Current	I_{DM}	± 1				A
Continuous Source Current (Diode Conduction) ^a	I_S	0.25	0.23	- 0.25	- 0.23	
Maximum Power Dissipation ^a	P_D ($T_A = 25$ °C)	0.30	0.27	0.30	0.27	W
	P_D ($T_A = 85$ °C)	0.16	0.14	0.16	0.14	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical		Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ s	R_{thJA}	360	415	°C/W
	Steady State		400	460	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	300	350	

Note:

a. Surface mounted on 1" x 1" FR4 board.

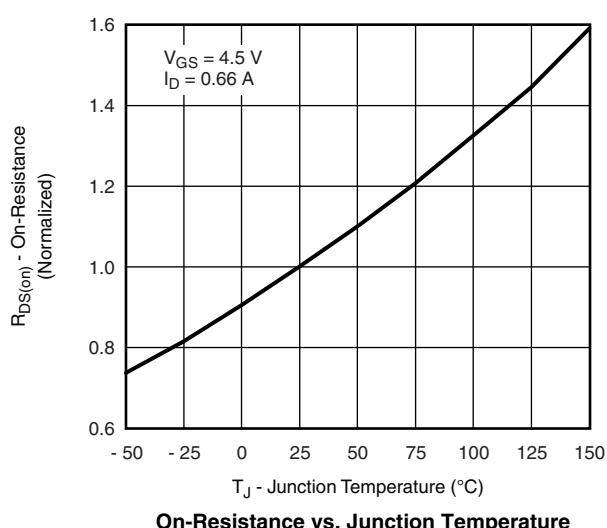
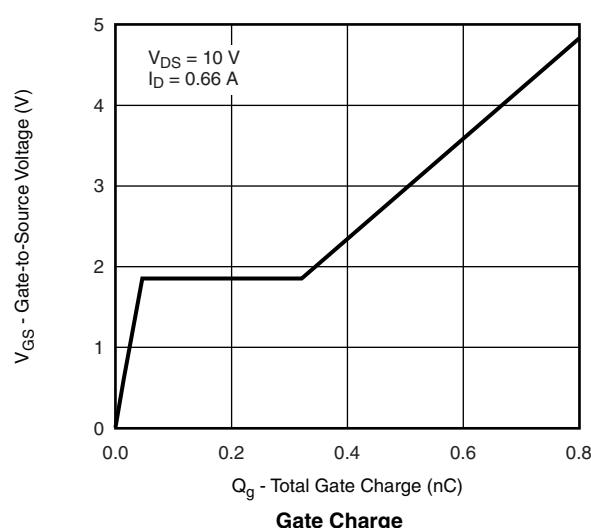
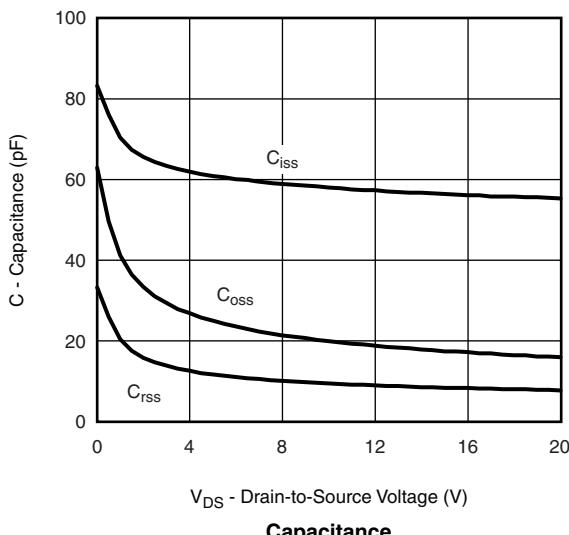
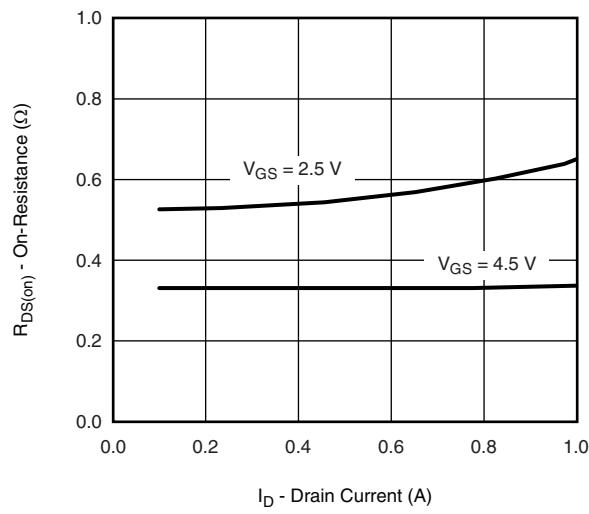
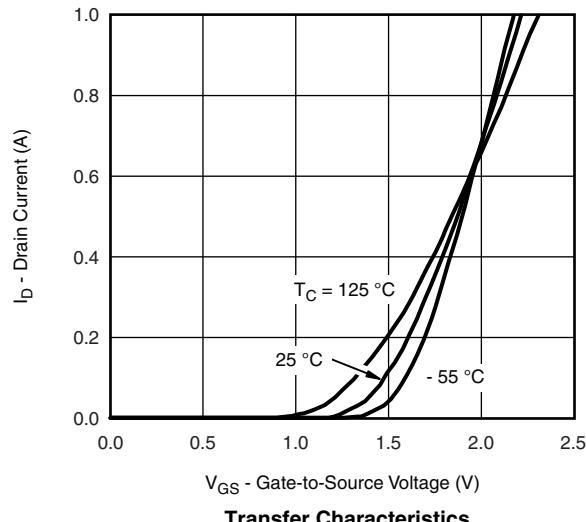
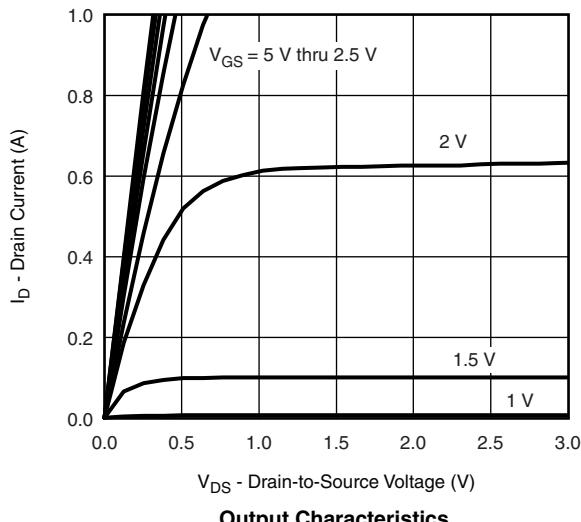
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	0.6		1.4
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-0.45		-1
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	N-Ch			± 100
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	P-Ch			± 100
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch			1
		$V_{DS} = -8 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch			-1
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$	N-Ch			5
		$V_{DS} = -8 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$	P-Ch			-5
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	1		
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	-1		
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}, I_D = 0.66 \text{ A}$	N-Ch		0.320	0.385
		$V_{GS} = -4.5 \text{ V}, I_D = -0.57 \text{ A}$	P-Ch		0.510	0.600
		$V_{GS} = 2.5 \text{ V}, I_D = 0.40 \text{ A}$	N-Ch		0.560	0.630
		$V_{GS} = -2.5 \text{ V}, I_D = -0.48 \text{ A}$	P-Ch		0.720	0.850
		$V_{GS} = -1.8 \text{ V}, I_D = -0.20 \text{ A}$	P-Ch		1.000	1.200
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 0.66 \text{ A}$	N-Ch		1.5	
		$V_{DS} = -4 \text{ V}, I_D = -0.57 \text{ A}$	P-Ch		1.2	
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.23 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch		0.8	1.2
		$I_S = -0.23 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch		-0.8	-1.2
Dynamic^b						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 0.66 \text{ A}$ P-Channel $V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -0.57 \text{ A}$	N-Ch		0.8	1.2
Gate-Source Charge	Q_{gs}		P-Ch		1.5	2.3
Gate-Drain Charge	Q_{gd}		N-Ch		0.06	
Rise Time	t_r	N-Channel $V_{DD} = 10 \text{ V}, R_L = 20 \Omega$ $I_D \approx 0.5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 6 \Omega$ P-Channel $V_{DD} = -4 \text{ V}, R_L = 8 \Omega$ $I_D \approx -0.5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 6 \Omega$	P-Ch		0.17	
Turn-On Delay Time	$t_{d(on)}$		N-Ch		0.30	
Fall Time	t_f		P-Ch		0.16	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		10	20
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 0.23 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $I_F = -0.23 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$	P-Ch		6	12
			N-Ch		16	30
			P-Ch		25	50
			N-Ch		10	20
			P-Ch		10	20
			N-Ch		10	20
			P-Ch		10	20
			N-Ch		20	40
			P-Ch		20	40

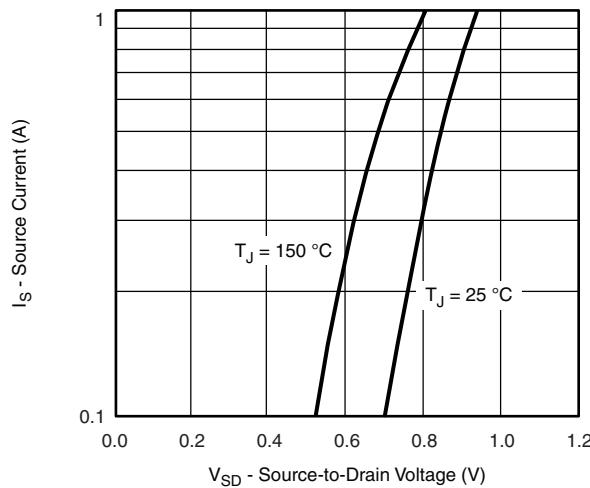
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

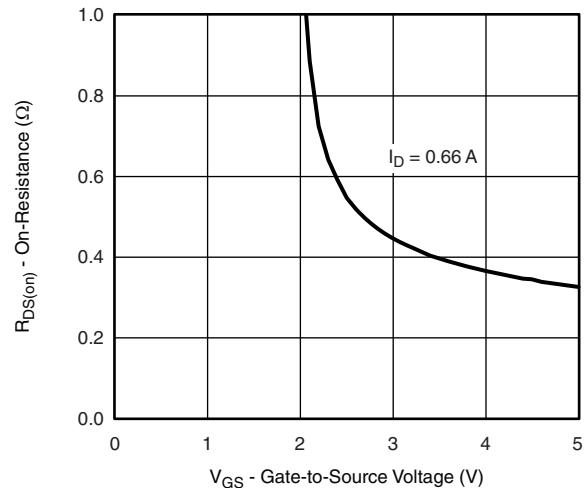
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


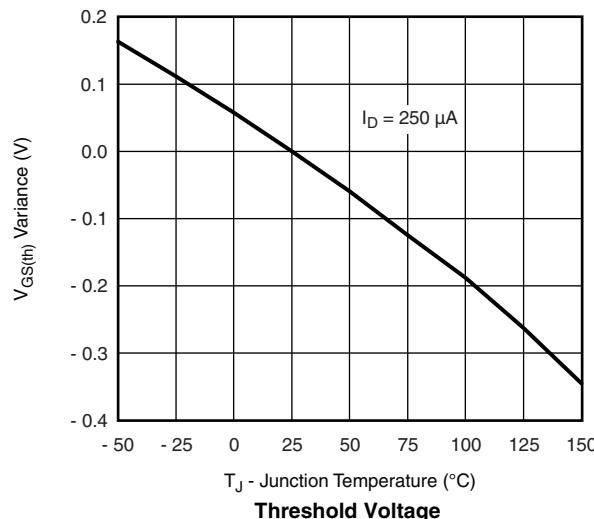
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



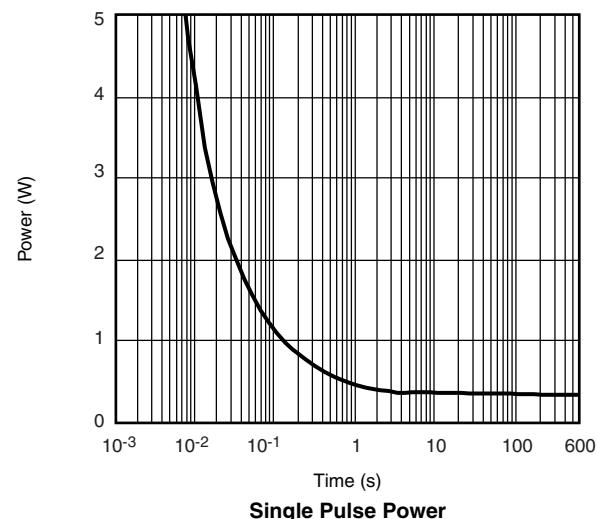
Source-Drain Diode Forward Voltage



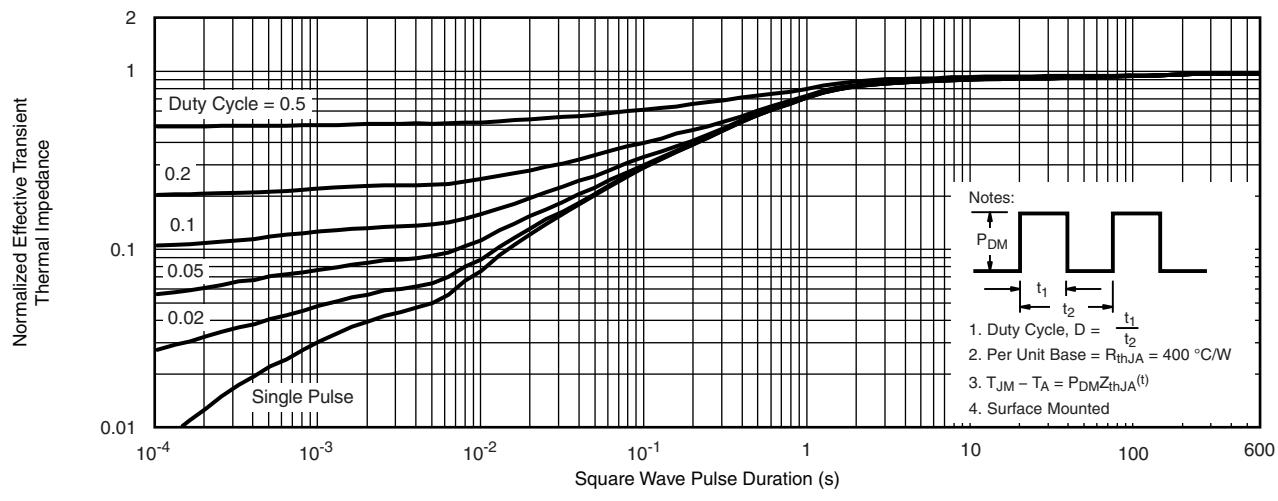
On-Resistance vs. Gate-to-Source Voltage



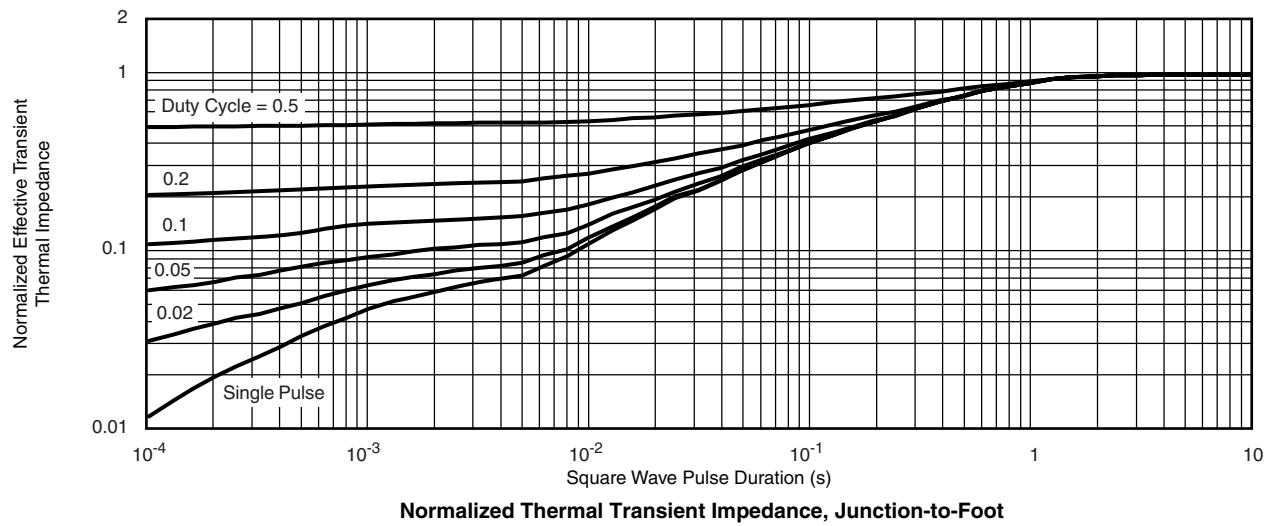
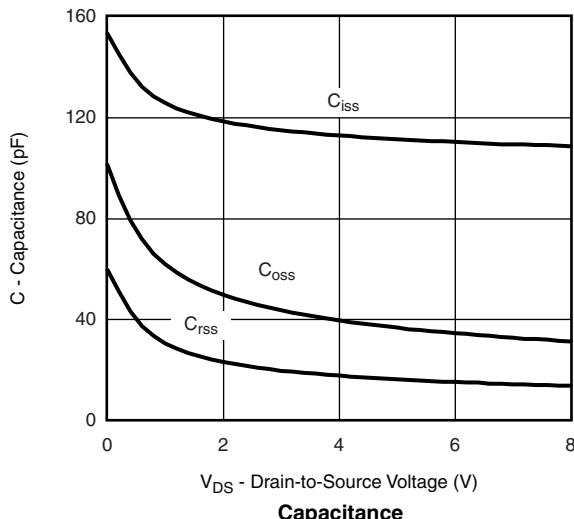
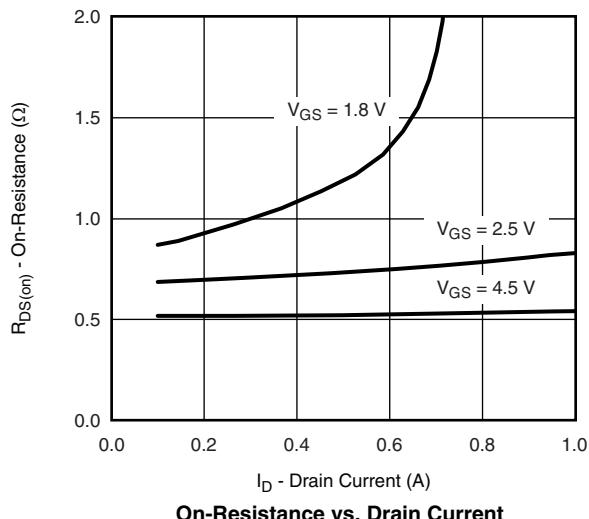
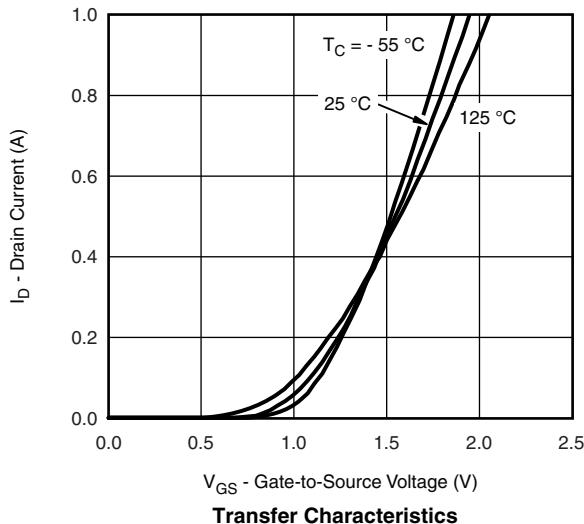
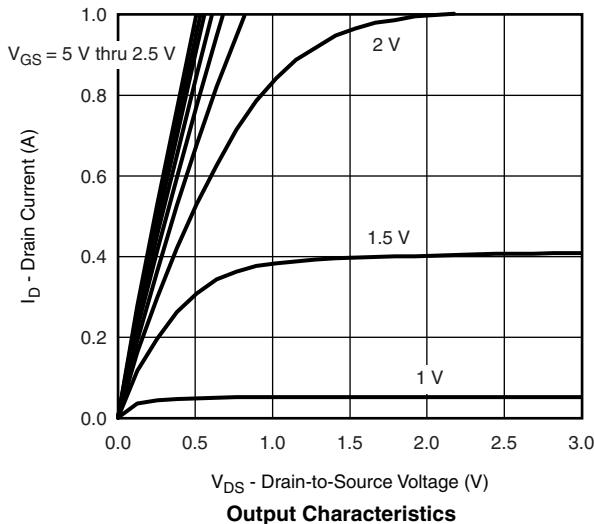
Threshold Voltage



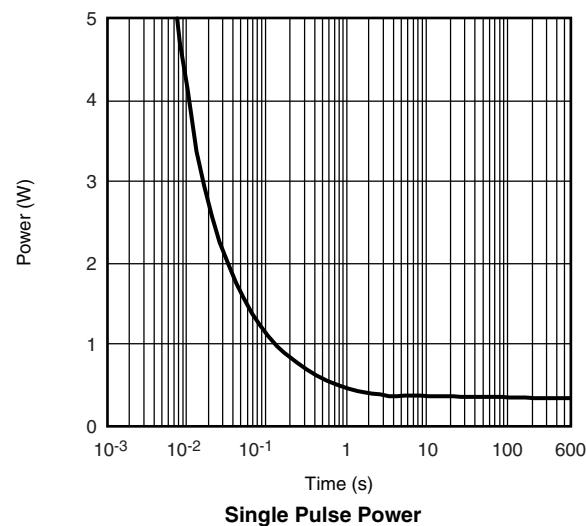
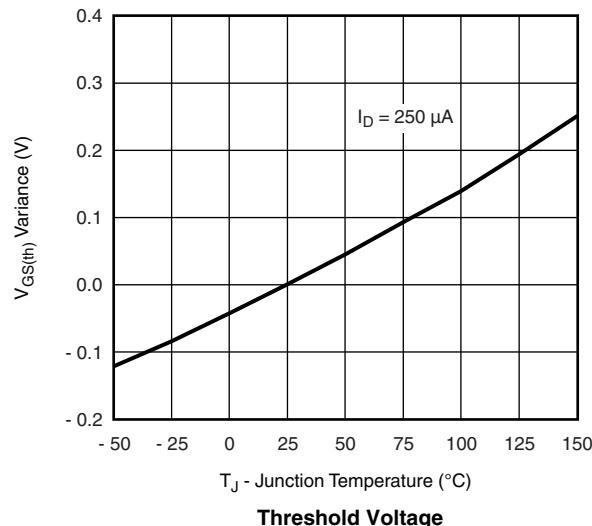
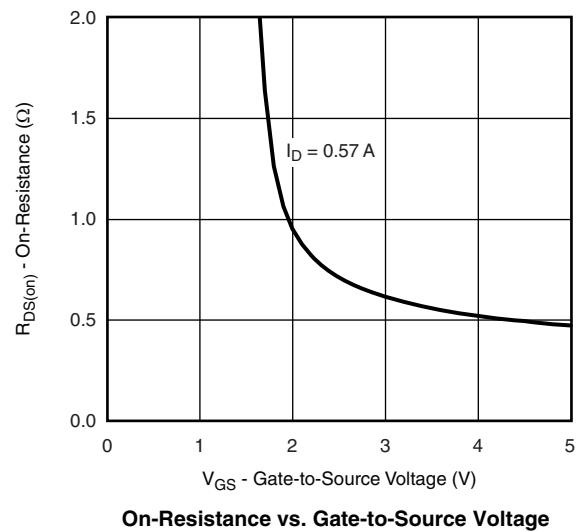
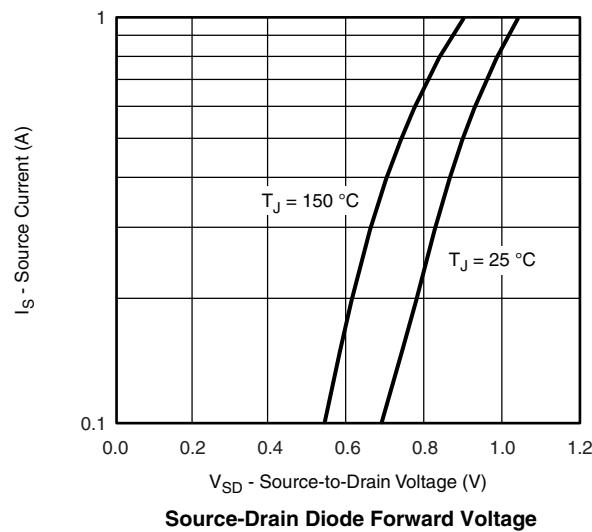
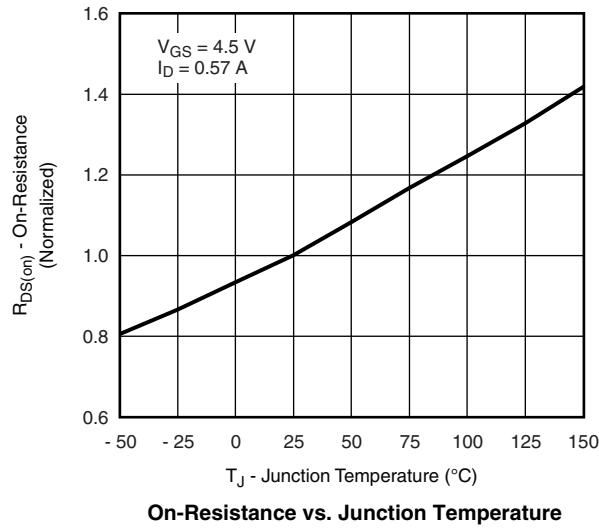
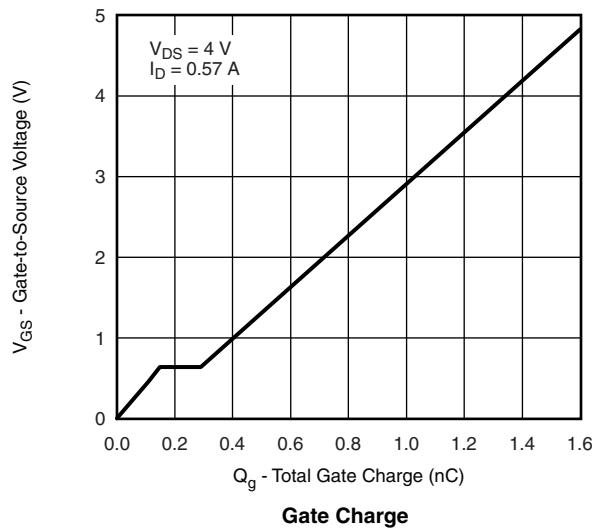
Single Pulse Power

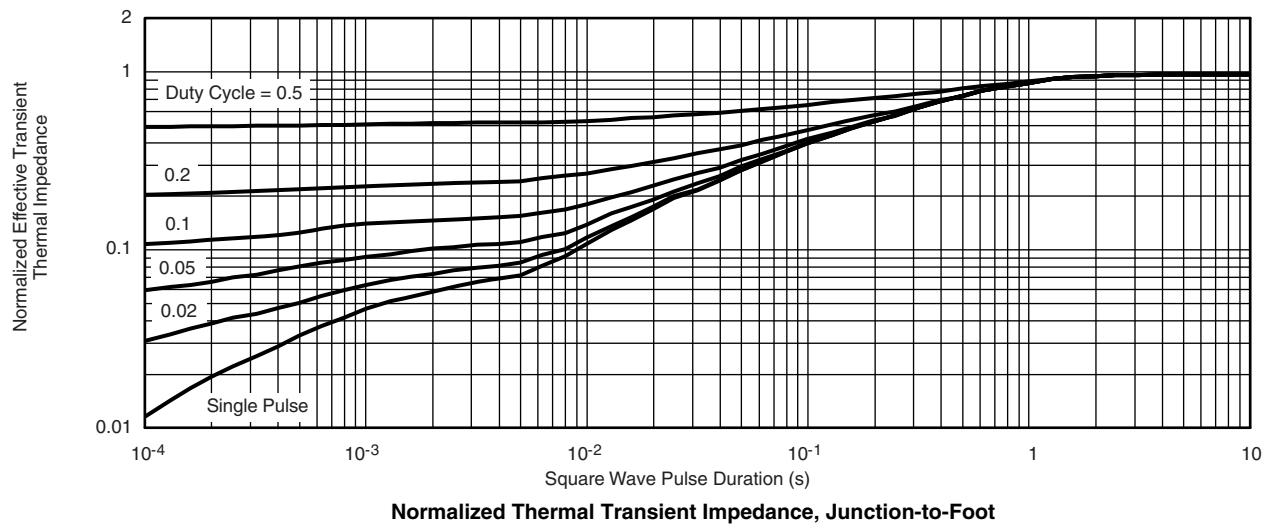
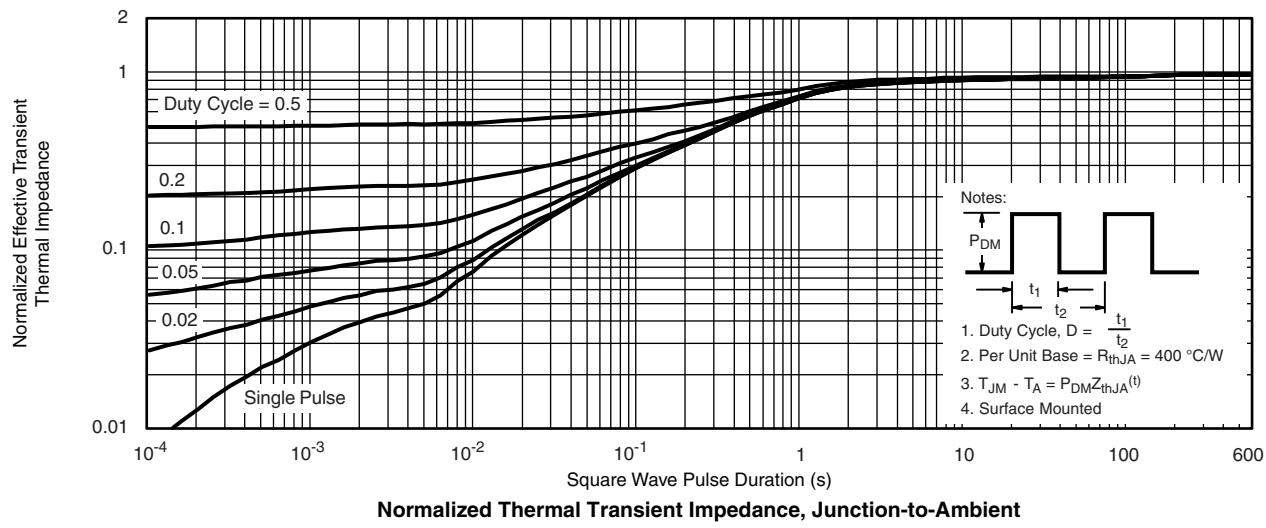


Normalized Thermal Transient Impedance, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


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