

# V.90, V.34, V.32BIS, V.22BIS ISOMODEM® WITH GLOBAL DAA

#### **Features**

- This data sheet applies to Si2457/34/ Integrated DAA 15/04 Revision D
- Data modem formats
  - ITU-T. Bell
  - 300 bps up to 56 kbps
  - V.21,V.22, V.29 Fast Connect
  - V.44, V.42, V.42bis, MNP2-5
  - Automatic rate negotiation
- Type I and II caller ID decode
- No external ROM or RAM required
- UART, SPI, or parallel interface
- Flexible clock options
  - Low-cost 32.768 kHz oscillator
  - 4.915 MHz oscillator
  - 27 MHz clock input

- - Over 6000 V capacitive isolation
  - Parallel phone detect
  - · Globally-compliant line interface
  - Overcurrent detection
- AT command set support
- SMS / MMS support
- Firmware upgradeable
- EEPROM interface
- Lead-free, RoHS-compliant packages
- Commercial or industrial temperature range
- DTMF detection/generation

### **Ordering Information**

This data sheet is valid only for those chipset combinations listed on page 50.

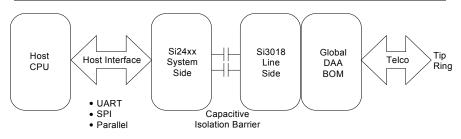
### **Applications**

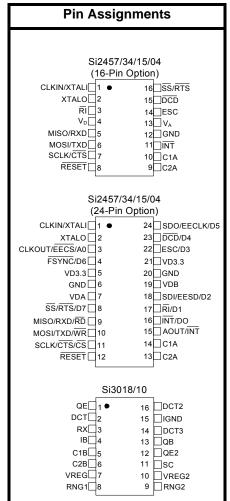
- Set-top boxes
- Point-of-sale terminals
- Text / video telephones
- Digital video recorder
- Digital televisions
- Remote monitoring

### **Description**

The ISOmodem<sup>®</sup> family of products is a complete modem ranging in speed from 56.000 bps to 2400 bps. Offered as a chipset with the Si2457, Si2434. Si2415, or Si2404 system-side device and the Si3018/10 line-side device, the ISOmodem utilizes Silicon Laboratories' patented direct access arrangement (DAA) technology to provide a programmable telephone line interface with an unparalleled level of integration. These compact solutions eliminate the need for a separate DSP, modem controller, codec, transformer, relay, opto-isolators, clocking crystal, and 2-4 wire hybrid. Available with a system-side packaging option of either a 16-pin SOIC or a 24-pin TSSOP, these devices are ideal for embedded modem applications due to their flexibility, small footprint, and minimal external component count.

### System Block Diagram







2

# TABLE OF CONTENTS

Se	<u>ection</u>	<u>Page</u>
1.	Electrical Specifications	4
2.	Typical Application Schematic	11
	Bill of Materials: Si2457/34/15/04 Chipset	
4.	Functional Description	17
	4.1. Host Interface	17
	4.2. Command Mode	18
	4.3. Data Mode	18
	4.4. Fast Connect	18
	4.5. V.80 Synchronous Access Mode	18
	4.6. Clocking	18
	4.7. Low-Power Modes	18
	4.8. Data Compression	18
	4.9. Error Correction	
	4.10. Wire Mode	18
	4.11. Caller ID Operation	19
	4.12. Parallel Phone Detection	
	4.13. Overcurrent Detection	
	4.14. Global Operation	
	4.15. Firmware Upgrades	
	4.16. DTMF Detection / Generation	
	4.17. SMS/MMS Support	
	4.18. Codec Interface (24-Pin Version Only)	
	4.19. EEPROM Interface (24-Pin Version Only)	
	4.20. AT Commands	
	4.21. Extended AT Commands	
5.	S-Registers	
	User-Access Registers (U-Registers)	
	Pin Descriptions: Si2457/34/15/04 (16-Pin Option)	
	Pin Descriptions: Si2457/34/15/04 (24-Pin Option)	
	Pin Descriptions: Si3018/10	
	). Ordering Guide	
	. Package Markings (Top Markings)	
	11.1. Si2457-D-FT Top Marking	
	11.2. Si2457-D-FS Top Marking	
	11.3. Si2434-D-FT Top Marking	
	11.4. Si2434-D-FS Top Marking	
	11.5. Si2415-D-FT Top Marking	
	11.6. Si2415-D-FS Top Marking	
	11.7. Si2404-D-FT Top Marking	
	11.8. Si2404-D-FS Top Marking	
	11.9. Si3010-F-FS Top Marking	
	11.10. Si3018-F-FS Top Marking	
12	2. Package Outline: 24-Pin TSSOP	
	3. 24-Pin TSSOP Land Pattern	
	l. Package Outline: 16-Pin SOIC	
	5. 16-Pin SOIC Land Pattern	
	ocument Change List	
	ontact Information	



### 1. Electrical Specifications

**Table 1. Recommended Operating Conditions** 

Parameter <sup>1</sup>	Symbol	Test Condition	Min <sup>2</sup>	Тур	Max <sup>2</sup>	Unit
Ambient Temperature	T <sub>A</sub>	F-grade G-grade	0 -40	25 25	70 85	°C
Si2457/34/15/04 Supply Voltage, Digital <sup>3</sup>	V <sub>D</sub>		3.0	3.3	3.6	V

#### Notes:

- **1.** The Si2457/34/15/04 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2457/34/15/04 and any Si3018 are used. See "2. Typical Application Schematic" on page 11.
- **2.** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
- 3. The digital supply, VD, operates from 3.0 to 3.6 V.

### **Table 2. Loop Characteristics**

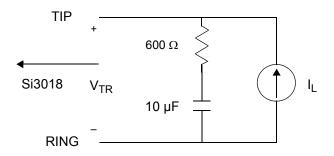
(V<sub>D</sub> = 3.0 to 3.6 V,  $T_A$  = 0 to 70 °C for F-grade,  $T_A$  = –40 to 85 °C for G-grade)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ILIM <sup>1</sup> = 0 DCV = 00, MINI = 11, DCR = 0	_	_	6.0	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9	_	_	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	_	_	7.5	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	_	_	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0		_	7.5	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40	_	_	V
DC Termination Voltage	V <sub>TR</sub>	I <sub>L</sub> = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0		_	40	V
On-Hook Leakage Current	I <sub>LK</sub>	V <sub>TR</sub> = -48 V	_		5	μΑ
Operating Loop Current	I <sub>LP</sub>	MINI = 00, ILIM = 0	10		120	mA
Operating Loop Current	I <sub>LP</sub>	MINI = 00, ILIM = 1	10		60	mA
DC Ring Current		DC current flowing through ring detection circuitry	_	1.5	3	μA
Ring Detect Voltage <sup>2</sup>	$V_{RD}$	RT = 0	12	15	18	$V_{RMS}$
Ring Detect Voltage <sup>2</sup>	$V_{RD}$	RT = 1	18	21	25	V <sub>RMS</sub>
Ring Frequency	F <sub>R</sub>		15	_	68	Hz
Ringer Equivalence Number	REN				0.2	

#### Notes:

- 1. ILIM = U67, bit 9; DCV = U67, bits 3:2; MINI = U67, bits 13:12; DCR = U67, bit 7; RT = U67, bit 0.
- **2.** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.





**Figure 1. Test Circuit for Loop Characteristics** 

Table 3. DC Characteristics,  $V_D = 3.0$  to 3.6 V

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \,^{\circ}\text{C} \text{ for F-grade}, T_A = -40 \text{ to } 85 \,^{\circ}\text{C} \text{ for G-grade})$ 

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit					
High Level Input Voltage	V <sub>IH</sub>		2.0	_	_	V					
Low Level Input Voltage	V <sub>IL</sub>			_	0.8	V					
High Level Output Voltage	V <sub>OH</sub>	I <sub>O</sub> = -2 mA	2.4	_	_	V					
Low Level Output Voltage	V <sub>OL</sub>	I <sub>O</sub> = 2 mA	_	_	0.35	V					
Input Leakage Current	IL		-10	_	10	μA					
Pullup Resistance Pins	R <sub>PU</sub>		50	125	200	kΩ					
Total Supply Current <sup>*</sup>	I <sub>D</sub>		_	17	35	mA					
Total Supply Current, Wake on Ring <sup>*</sup>	I <sub>D</sub>			4.4	_	mA					
Total Supply Current, Powerdown*	I <sub>D</sub>	PDN = 1	_	80	_	μA					
*Note: All inputs at 0 or V <sub>D</sub> . All inputs held	static except	clock and all outputs un	loaded (Sta	tic I <sub>OUT</sub> = 0	*Note: All inputs at 0 or V <sub>D</sub> . All inputs held static except clock and all outputs unloaded (Static I <sub>OUT</sub> = 0 mA).						



# Si2457/34/15/04

### **Table 4. AC Characteristics**

( $V_D$  = 3.0 to 3.6 V, TA = 0 to 70 °C for F-grade, Fs = 8 kHz,  $T_A$  = -40 to 85 °C for G-grade)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Sample Rate	Fs		_	8	_	kHz
Clock Input Frequency	F <sub>XTL</sub>	default	_	4.9152	_	MHz
Clock Input Frequency	F <sub>XTL</sub>	27 MHz Mode <sup>1</sup>	_	27	_	MHz
Clock Input Frequency	F <sub>XTL</sub>	32 kHz Mode <sup>1</sup>	_	32.768	_	kHz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	_	5	_	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	_	200	_	Hz
Transmit Full Scale Level <sup>2</sup>	V <sub>FS</sub>		_	1.1	_	V <sub>PEAK</sub>
Receive Full Scale Level <sup>2,3</sup>	V <sub>FS</sub>		_	1.1		V <sub>PEAK</sub>
Dynamic Range <sup>4</sup>	DR	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I <sub>L</sub> = 100 mA	—	80	_	dB
Dynamic Range <sup>4</sup>	DR	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I <sub>L</sub> = 20 mA	_	80	_	dB
Dynamic Range <sup>4</sup>	DR	ILIM = 1, DCV = 11, MINI = 00 DCR = 0, I <sub>L</sub> = 50 mA	_	80	_	dB
Transmit Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 0, DCV = 11, MINI = 00 DCR = 0, I <sub>L</sub> = 100 mA	_	<b>–72</b>	_	dB
Transmit Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I <sub>L</sub> = 20 mA	_	<b>–78</b>	_	dB
Receive Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 0, DCV = 00, MINI = 11 DCR = 0, I <sub>L</sub> = 20 mA	_	<b>–78</b>	_	dB
Receive Total Harmonic Distortion <sup>5</sup>	THD	ILIM = 1,DCV = 11, MINI=00 DCR = 0, I <sub>L</sub> = 50 mA	_	<b>–78</b>	_	dB
Dynamic Range (Caller ID Mode)	DR <sub>CID</sub>	VIN = 1 kHz, –13 dBm	_	50	_	dB

#### Notes:

- 1. Refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for configuring clock input reset strapping.
- 2. Measured at TIP and RING with 600  $\Omega$  termination at 1 kHz, as shown in Figure 1 on page 5.
- 3. Receive full scale level produces –0.9 dBFS at DTX.
- 4. DR = 20 x log |Vin| + 20 x log (rms signal/rms noise). Applies to both transmit and receive paths. Vin = 1 kHz, -3 dBFS.
- **5.** Vin = 1 kHz, -3 dBFS. THD = 20 x log (rms distortion/rms signal).



**Table 5. Absolute Maximum Ratings** 

Parameter	Symbol	Value	Unit
DC Supply Voltage	V <sub>D</sub>	4.1	V
Input Current, Si2457/34/15/04 Digital Input Pins	I <sub>IN</sub>	±10	mA
Digital Input Voltage	V <sub>IND</sub>	-0.3 to (V <sub>D</sub> + 0.3)	V
CLKIN/XTALI Input Voltage	$V_{XIND}$	-0.3 to (V <sub>D</sub> + 0.3)	V
Operating Temperature Range	T <sub>A</sub>	-10 to 100	°C
Storage Temperature Range	T <sub>STG</sub>	-40 to 150	°C

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Table 6. Switching Characteristics<sup>1</sup>

 $(V_D = 3.0 \text{ to } 3.6 \text{ V}, T_A = 0 \text{ to } 70 \,^{\circ}\text{C} \text{ for F-grade}, T_A = -40 \text{ to } 85 \,^{\circ}\text{C} \text{ for G-grade})$ 

Parameter	Symbol	Min	Тур	Max	Unit
UART Timing Parameters	,		1		
Baud Rate Accuracy	t <sub>BD</sub>	-1	_	1	%
Reset Timing Parameters	·				
RESET ↓ to RESET ↑	t <sub>RS</sub>	5.0 <sup>2</sup>	_	_	ms
RESET ↑ to 1st AT Command	t <sub>AT</sub>	300	_	_	ms
Parallel Timing Parameters	·				
Address Setup	t <sub>AS</sub>	15	_	_	ns
Address Hold	t <sub>AH</sub>	0	_	_	ns
WR Low Pulse Width	t <sub>WL</sub>	50	_	_	ns
Write Data Setup Time	t <sub>WDSU</sub>	20	_	_	ns
Write Cycle Time	t <sub>WC</sub>	120	_	_	ns
Chip Select Setup	t <sub>CSS</sub>	10	_	_	ns
Chip Select Hold	t <sub>CSH</sub>	0	_	_	ns
RD Low Pulse Width	t <sub>RL</sub>	50	_	_	ns
RD Low to Data Driven Time	t <sub>RLDD</sub>	_	_	20	ns
Data Hold	t <sub>DH</sub>	10	_	_	ns
RD High to Hi-Z Time	t <sub>DZ</sub>	_	_	30	ns

#### Notes:

- All timing is referenced to the 50% level of the waveform. Input test levels are V<sub>IH</sub> = V<sub>D</sub> 0.4 V, V<sub>IL</sub> = 0.4 V.
   With 32.768 kHz clocking, allow 500 ms for the reset low-to-high minimum pulse on power-up and wake-from-powerdown conditions.



Table 6. Switching Characteristics (Continued) ( $V_D$  = 3.0 to 3.6 V,  $T_A$  = 0 to 70 °C for F-grade,  $T_A$  = -40 to 85 °C for G-grade)

Parameter	Symbol	Min	Тур	Max	Unit
Read Cycle Time	t <sub>RC</sub>	120	_	_	ns
Write to Read Cycle Time	t <sub>WRC</sub>	120	_		ns
Serial Peripheral Interface (SPI) Timing Pa	rameters				
SS Falling to First SCLK Edge	t <sub>SE</sub>	41	_	_	ns
Last SCLK Edge to SS Rising	t <sub>SD</sub>	41	_	_	ns
SS Rising to MISO High-Z	t <sub>SDZ</sub>	_	_	93	ns
SCLK High Time	t <sub>CKH</sub>	102	_	_	ns
SCLK Low Time	t <sub>CKL</sub>	102	_	_	ns
MOSI Valid to SCLK Sample Edge	t <sub>SIS</sub>	41	_	_	ns
SCLK Sample Edge to MOSI Change	t <sub>SIH</sub>	41	_	_	ns
SCLK Shift Edge to MISO Change	t <sub>SOH</sub>	_	_	93	ns
SCLK cycle time	t <sub>SCK</sub>	224	_	_	ns
Inactive time between SS actives	t <sub>NSS_INACT</sub>	81	_	_	ns

#### Notes:

- All timing is referenced to the 50% level of the waveform. Input test levels are V<sub>IH</sub> = V<sub>D</sub> 0.4 V, V<sub>IL</sub> = 0.4 V.
   With 32.768 kHz clocking, allow 500 ms for the reset low-to-high minimum pulse on power-up and wake-from-powerdown conditions.

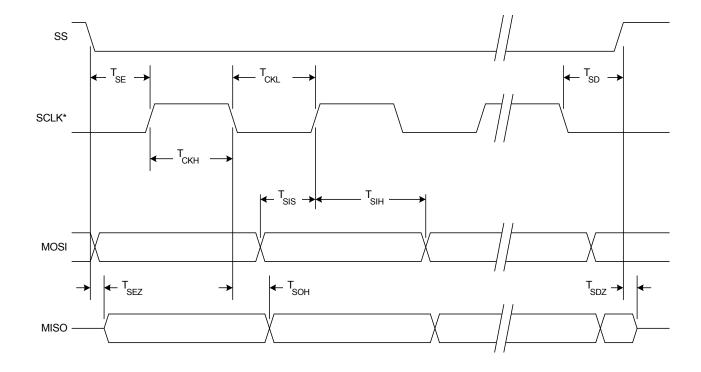


Figure 2. SPI Slave Timing

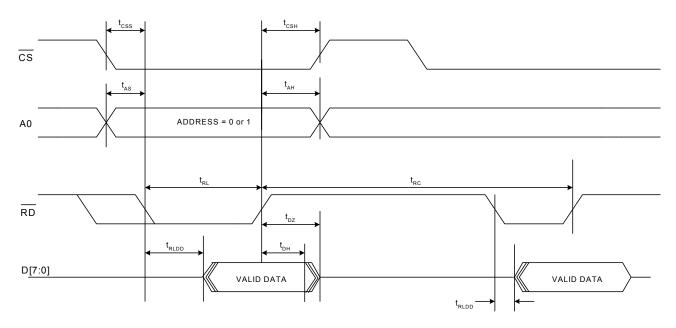
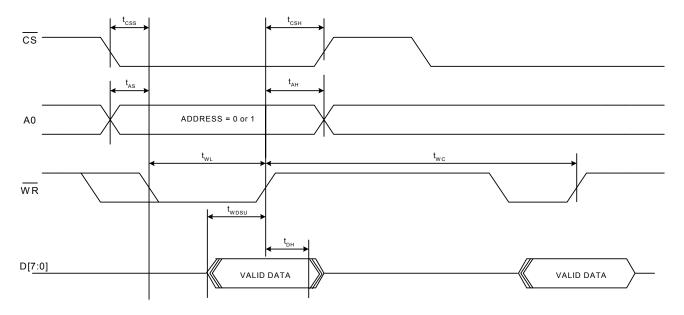


Figure 3. Parallel Interface Read Timing



**Figure 4. Parallel Interface Write Timing** 



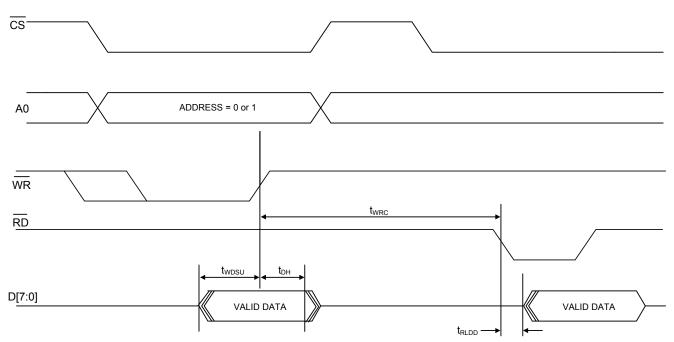


Figure 5. Parallel Interface Write Followed by Read Timing

# 2. Typical Application Schematic

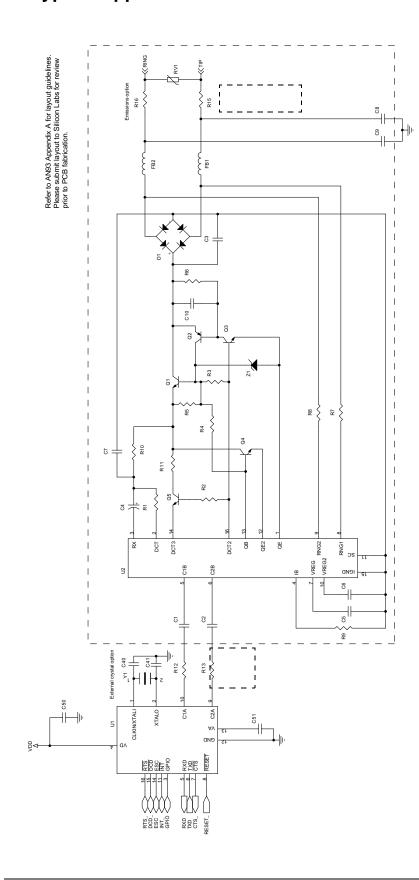


Figure 6. Typical Si2457/34/15/04 Schematic with 16-pin System-Side Option



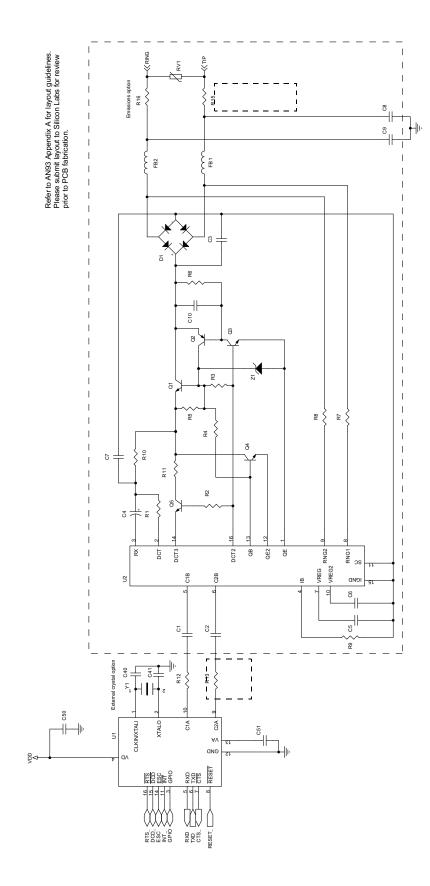


Figure 7. Typical Si2457/34/15/04 Schematic with 24-pin System-Side Option

### 3. Bill of Materials: Si2457/34/15/04 Chipset

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6, C50, C52 <sup>1</sup>	0.1 μF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 μF, 16 V, X7R, ±20%	Venkel, SMEC
C40	32.768 kHz: 18 pF, 16 V, NPO, ±5%	Venkel, SMEC
C40 C41	4.9152 MHz: 33 pF, 16 V, NPO, ±5%	VEHINEI, SIVIEC
041	27 MHz: Not Populated	
C51, C53 <sup>1</sup>	0.22 μF, 16 V, X7R, ±20%	Venkel, SMEC
D1, D2 <sup>2</sup>	Dual Diode, 225 mA, 300 V, CMPD2004S	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM21AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonio
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonio
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonio
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonio
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonio
R7, R8	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonio
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonio
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonio
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonio
R12, R13	56 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonio
R15, R16 <sup>3</sup>	0 Ω, 1/16 W	Venkel, SMEC, Panasonio
U1	Si2457/34/15/04	Silicon Labs
U2	Si3018/10	Silicon Labs
	32.768 kHz, 12 pF, 100 ppm, 35 kΩ max ESR	ECS Inc., Siward
Y1 <sup>4</sup>	4.9152 MHz, 20 pF, 100 ppm, 150 Ω ESR	EGS IIIG., SIWAIU
	27 MHz (from external clock)	
Z1	Zener Diode, 43 V, 1/2 W, BZT84C43	On Semi

#### Notes:

- 1. C52 and C53 should not be populated with the Si2457/34/15/04 16-pin package option.
- 2. Several diode bridge configurations are acceptable. For example, a single DF04S or four 1N4004 diodes may be used.
- 3. Murata BLM21AG601SN1 may be substituted for R15–R16 (0  $\Omega$ ) to decrease emissions.
- **4.** To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading.



**Table 7. Protocol Characteristics** 

ltem	Specification		
Data Rate			
56 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
54.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
53.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
52 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
50.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
49.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
48 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
46.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
45.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
44 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
42.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
41.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
40 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
38.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
37.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
36 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
34.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
33.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
32 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
30.666 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
29.333 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
28 kbps <sup>1</sup>	ITU-T V.90 <sup>1</sup>		
33.6 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
31.2 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
28.8 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
26.4 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
24.0 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
21.6 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
19.2 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
16.8 kbps <sup>2</sup>	ITU-T V.34 <sup>2</sup>		
14.4 kbps <sup>3</sup>	ITU-T V.34 or V.32bis <sup>3</sup>		
12.0 kbps <sup>3</sup>	ITU-T V.34 or V.32bis <sup>3</sup>		
9600 bps <sup>3</sup>	ITU-T V.34, V.32bis, or V.29 <sup>3</sup>		
7200 bps <sup>3</sup>	ITU-T V.34 or V.32bis <sup>3</sup>		
4800 bps <sup>3</sup>	ITU-T V.34 or V.32bis <sup>3</sup>		
2400 bps	ITU-T V.34 or V.22bis <sup>3</sup>		
1200 bps	ITU-T V.22bis, V.23, or Bell 212A		
300 bps	ITU-T V.21		
300 bps	Bell 103		
Notes:	25100		

- 1. Supported on Si2457 only.
- 2. Supported on Si2457 and Si2434 only.
- 3. Supported on Si2457, Si2434, and Si2415 only.



**Table 7. Protocol Characteristics (Continued)** 

Item	Specification
Data Format	
Bit asynchronous	Selectable 8, 9, 10, or 11 bits per character, which includes the start, stop, and parity bits
Compatibility	ITU-T V.90 <sup>1</sup> , V.34 <sup>2</sup> , V.32bis, V.32, V.23, V.22bis, V.22, V.21, Bell 212A, and Bell 103
Operating Mode	
Switched network	Two-wire full duplex
Data Modulation	
28 to 56 kbps <sup>1</sup>	V.90 as specified by ITU-T
2.4 to 33.6 kbps <sup>2</sup>	V.34 as specified by ITU-T
14.4 kbps <sup>3</sup>	128-level TCM/2400 Baud ±0.01%
12.0 kbps <sup>3</sup>	64-level TCM/2400 Baud ±0.01%
9600 bps <sup>3</sup>	32-level TCM/2400 Baud ±0.01%
9600 bps <sup>3</sup>	16-level QAM/2400 Baud ±0.01%
9600 bps <sup>3</sup>	V.29 QAM as specified by ITU-T
7200 bps <sup>3</sup>	16-level TCM/2400 Baud ±0.01%
4800 bps <sup>3</sup>	4-level QAM/2400 Baud ±0.01%
2400 bps	16-level QAM/600 Baud ±0.01%
1200 bps	4-level PSK/600 Baud ±0.01%
300 bps	FSK 300 Baud ±0.01%
Answer Tone	
ITU-T V.32bis, V.32, V.22bis, V.22, and V.21	2100 Hz ±3 Hz
modes	
Bell 212A and 103 modes	2225 Hz ±3 Hz
Transmit Carrier	
V.90 <sup>1</sup>	As specified by ITU-T
V.34 <sup>2</sup>	As specified by ITU-T
ITU-T V.32bis <sup>3</sup>	1800 Hz ±0.01%
ITU-T V.32 <sup>3</sup>	1800 Hz ±0.01%
ITU-T V.29 <sup>3</sup>	1700 Hz±1 Hz
ITU-T V.22, V.22bis/Bell 212A	1200 Hz ±0.5 Hz
Originate mode	2400 Hz ±1 Hz
Answer mode	
ITU-T V.21	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)
Originate mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)
Answer mode	
Bell 103	Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)
Originate mode	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)
Answer mode	
Output Level	
Permissive—Switched network	–9 dBm maximum
Notes:	

- **1.** Supported on Si2457 only.
- 2. Supported on Si2457 and Si2434 only.
- 3. Supported on Si2457, Si2434, and Si2415 only.



**Table 7. Protocol Characteristics (Continued)** 

Item	Specification			
Receive Carrier				
ITU-T V.90 <sup>1</sup>	As specified by ITU-T			
ITU-T V.34 <sup>2</sup>	As specified by ITU-T			
ITU-T V.32bis <sup>3</sup>	1800 Hz ±7 Hz			
ITU-T V.32 <sup>3</sup>	1800 Hz ±7 Hz			
ITU-T V.29 <sup>3</sup>	1700 Hz ±7 Hz			
ITU-T V.22, V.22bis/Bell 212A	2400 Hz ±7 Hz			
Originate mode	1200 Hz ±7 Hz			
Answer mode	_			
ITU-T V.21	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)			
Originate mode	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)			
Answer mode				
Bell 103	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)			
Originate mode	Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)			
Answer mode				
Carrier Detect (level for ITU-T V.22bis, V.22, V.21,	Acquisition (-43 dBm)			
212, 103) in Switched Network	Release (–48 dBm)			
Hysteresis	2 dBm minimum			
<b>Note:</b> ITU-T V.90 <sup>1</sup> , V.34 <sup>2</sup> , V.32/V.32bis <sup>3</sup> are echo cance connection. They also provide for self-training determined by the connection of the connectio	ling protocols that use signal quality as criteria for maintaining ection to force disconnect.			
DTE Interface	EIA/TIA-232-E (ITU-T V.24/V.28/ISO 2110)			
Line Equalization	Automatic Adaptive			
Connection Options	Loss of Carrier in ITU-T V.22bis and lower			
Phone Types	500 (rotary dial), 2500 (DTMF dial)			
Dialing	Pulse and Tone			
DTMF Output Level	Per TIA-968-B			
Pulse Dial Ratio	Make/Break: 39/61%			
Ring Cadence	Per T1.401.02-2000			
Call Progress Monitor	BUSY			
	CONNECT (rate)			
	NO ANSWER			
	NO CARRIER			
	NO DIALTONE			
	OK			
	RING			
	RINGING			
Notes:				

- **1.** Supported on Si2457 only.
- 2. Supported on Si2457 and Si2434 only.
- **3.** Supported on Si2457, Si2434, and Si2415 only.



## 4. Functional Description

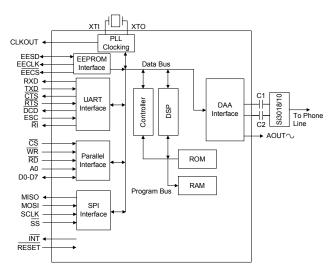


Figure 8. Functional Block Diagram

The Si2457/34/15/04 ISOmodem<sup>®</sup> is a complete embedded modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two small packages, this solution includes a DSP data pump, modem controller, on-chip RAM and ROM, codec, DAA, analog output, and 27 MHz clock input.

The Si2457/34/15/04 accepts standard modem AT commands and provides connect rates up to 56/33.6/14.4/2.4 kbps full-duplex over the Public Switched Telephone Network (PSTN). The Si2457/34/15/04 features a complete set of modem protocols including all ITU-T standard formats up to V.90.

To provide the most flexibility, the Si2457/34/15/04 ISOmodem system-side device is offered in either a 24-pin TSSOP or a 16-pin SOIC package. The 16-pin version is footprint-compatible with the Si2401 ISOmodem and is recommended for most applications. The 16-pin version does not support the parallel, EEPROM or voice codec interface. If these features are required, customers should use the 24-pin version.

The ISOmodem provides numerous additional features for embedded modem applications. The modem includes full type I and type II caller ID detection and decoding for global standards. Call progress monitoring is supported through standard result codes. The modem is also programmable to meet global settings. Because the Si2457/34/15/04 ISOmodem integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2457/34/15/04 solution includes a silicon DAA using Silicon Laboratories' proprietary third-generation DAA technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the Si2457/34/15/04 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, surge immunity, and safety requirements.

The Si2457/34/15/04 allows for rapid integration into existing modem applications by providing a serial interface that can directly communicate to either a microcontroller via a UART interface or a PC via an RS-232 port. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software.

#### 4.1. Host Interface

The Si2457/34/15/04 interfaces to the host processor through either an asynchronous serial interface, a synchronous Serial Peripheral Interface (SPI), or a parallel interface. The default is asynchronous serial communication. Selection of either SPI or parallel interface is done on power-up with reset strapping. Please refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for details.

#### 4.1.1. Asynchronous Serial Interface

The Si2457/34/15/04 supports asynchronous serial communication with data terminal equipment (DTE) at rates up to 307.2 kbps with the standard serial UART format. Upon powerup, the UART baud rate is automatically detected using the autobaud feature.

#### 4.1.2. Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) provides a flexible, full-duplex synchronous serial bus for host processor and Si2457/34/15/04 ISOmodem communication. When the Si2457/34/15/04 is powered up with SPI mode enabled the modem becomes an SPI slave, and the pins are configured to SS (slave select input, active low), MOSI (serial data input to modem), MISO (serial data output from modem) and SCLK (serial data clock input). Each SPI operation consists of a control-and-address byte and a data byte.

### 4.1.3. Parallel Interface (24-Pin Version Only)

The Si2457/34/15/04 can also communicate via a parallel interface when using the 24-pin version. The parallel interface is an 8-bit data bus with a single bit address to memory mapped registers.



#### 4.2. Command Mode

Upon reset, the ISOmodem<sup>®</sup> is in command mode and accepts "AT" commands. An outgoing modem call can be made using the "ATDT#" (tone dial) or "ATDP#" (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes detailed in Table 12 on page 38 and enters data mode.

#### 4.3. Data Mode

The Si2457/34/15/04 ISOmodem is in data mode while it has a telephone line connection to another modem or is in the process of establishing a connection.

Data protocols are available to provide error correction to improve reliability (V.42 and MNP2-4) and data compression to increase throughput (V.44, V.42bis and MNP5).

Each connection between two modems in data mode begins with a handshaking sequence. During this sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem during the negotiation process.

### 4.4. Fast Connect

The Si2457/34/15/04 supports a fast connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes can be enabled for V.21, V.22, Bell103, and V.29 modulations. See AN93 for details.

#### 4.5. V.80 Synchronous Access Mode

The Si2457/34/15/04 supports a V.80 synchronous access mode of operation, which operates with an asynchronous DTE and a synchronous DCE. See "AN93: ISOmodem® Chipset Family Designer's Guide".

### 4.6. Clocking

The Si2457/34/15/04 contains an on-chip phase-locked loop (PLL) and clock generator to derive all necessary internal system clocks from a single clock input. A 32.768 kHz or 4.9152 MHz crystal can be used across XTALI and XTALO pins to form the master clock (±100 ppm max, ±25 ppm recommended) for the ISOmodem. The 32.768 kHz option can provide lower BOM costs and smaller footprint. Alternatively, a clock input of 27 MHz, 4.9152 MHz, or 32.768 kHz can be provided to XTALI if that clock source is available in the system. A 4.9152 MHz clock input is the default clock option. Other clock options are selected at power-up through reset strapping. Refer to AN93 for details.

#### 4.7. Low-Power Modes

The Si2457/34/15/04 provides multiple low power modes. Using the S24 S-register, the Si2457/34/15/04 can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the last DTE activity, after the transmit FIFO is empty, and after the last data are received from the remote modem.

Additionally, the Si2457/34/15/04 can be placed in wake-on-ring-mode using the command, AT&Z. In either mode, the ISOmodem remains in the sleep state until one of the following occurs:

- A 1-to-0 transition on TXD (UART mode).
- A 1-to-0 transition on SS (SPI mode).
- A 1-to-0 transition on CS (parallel mode).
- An incoming ring is detected.
- A parallel telephone is picked up.
- Line polarity reversal

The Si2457/34/15/04 may also be placed in a complete powerdown mode. Once the Si2457/34/15/04 completely powers down, it can only be powered back on via the RESET pin.

### 4.8. Data Compression

The modem can achieve DTE (host-to-ISOmodem) speeds greater than the maximum DCE (modem-to-modem) speed through the use of a data compression protocol. The compression protocols available are the ITU-T V.42bis and MNP5 protocols. Data compression attempts to increase throughput by compressing the data before actually sending it. Thus, the modem is able to transmit more data in a given period of time.

#### 4.9. Error Correction

The Si2457/34/15/04 ISOmodem can employ error correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The Si2457/34/15/04 supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled by default.

#### 4.10. Wire Mode

Wire mode is used to communicate with standard non-error correcting modems. When optioned with \N3, the Si2457/34/15/04 falls back to wire mode if it fails in an attempt to negotiate a V.42 link with the remote modem. Error correction and data compression are not active in wire mode.



### 4.11. Caller ID Operation

The Si2457/34/15/04 supports full type I and type II caller ID detection and decode. Caller ID is supported for the US Bellcore, European ETSI, UK, and Japanese protocols and is enabled via the +VCID, +VCDT, and +PCW commands.

### 4.12. Parallel Phone Detection

The ISOmodem<sup>®</sup> is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the ISOmodem is using the phone line.

#### 4.12.1. On-Hook Line-in-use Detection

When the ISOmodem is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the ISOmodem to monitor the TIP-RING dc voltage with the line voltage sense (LVS) register (U6C, bits 15:8).

The LVS bits have a resolution of 1 V per bit with an accuracy of approximately ±10%. Bits 0 through 6 of this 8-bit signed twos complement number indicate the value of the line voltage, and the sign bit (bit 7) indicates the polarity of TIP and RING. The ISOmodem can also monitor the TIP-RING dc voltage using the LVCS register (U79, bits 4:0). See Figure 9 on page 19. See also the %Vn commands for automatic line-in-use detection.

#### 4.12.2. Off-Hook Intrusion Detection

When the ISOmodem is off-hook, an algorithm is implemented in the ISOmodem to automatically monitor the TIP-RING loop current via the LVCS register. During the off-hook state, the LVCS register switches from representing the TIP-RING voltage to representing the TIP-RING current. See Figure 10 on page 20. Upon detecting an intrusion, the ISOmodem alerts the host of the condition via the INT pin.

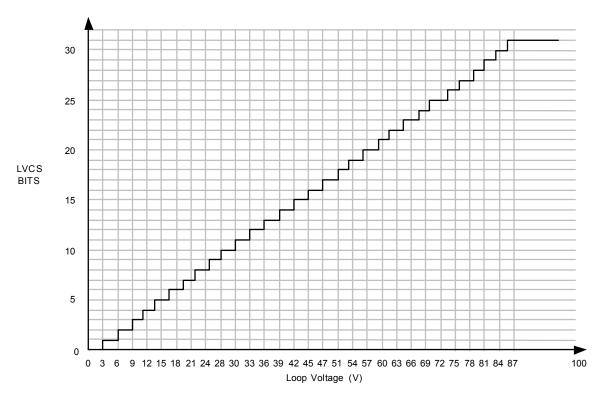


Figure 9. Loop Voltage



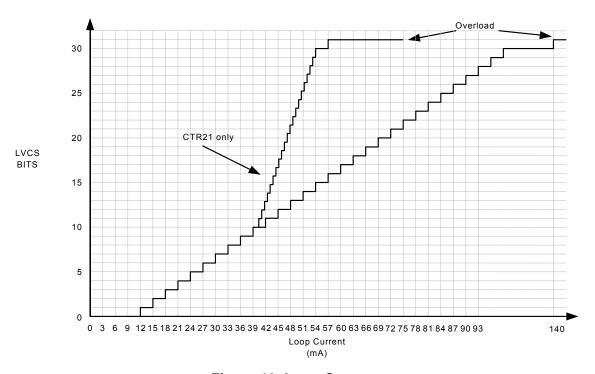


Figure 10. Loop Current



#### 4.13. Overcurrent Detection

The Si2457/34/15/04 includes an overcurrent detection feature that measures the loop current at a programmable time after the Si2457/34/15/04 goes off-hook. This allows the Si2457/34/15/04 to detect if it is connected to an improper telephone line. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured. See "AN93: ISOmodem® Chipset Family Designer's Guide" for details.

### 4.14. Global Operation

The Si2457/34/15/04 chipset contains an integrated silicon direct access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. "AN93: Modem Designer's Guide" gives the DAA register settings required to meet international PTT standards.

Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone. See AN93 for complete details.

### 4.15. Firmware Upgrades

The Si2457/34/15/04 contains an on-chip program ROM that includes the firmware required for the features listed in this data sheet. In addition, the Si2457/34/15/04 contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field. See AN93 for complete details.

#### 4.16. DTMF Detection / Generation

The Si2457/34/15/04 provides comprehensive DTMF tone generation and detection. The ISOmodem can generate single tones or DTMF tones using the +VTS command. DTMF tones may also be generated during dialing using the "ATDT" command. DTMF detection is only available in voice mode (+FCLASS = 8). DTMF digits are reported from the modem to the host using <DLE> shielding.

### 4.17. SMS/MMS Support

Short Message Service (SMS) is a service that allows text messages to be sent and received from one telephone to another via an SMS service center. Multimedia Messaging Service (MMS) extends the core SMS capability to send messages that include multimedia content. The Fax ISOmodem provides an interface that offers a great deal of flexibility in handling multiple SMS standards. This flexibility is possible because most of the differences between standards are handled by the host using the raw data itself. The Si2457/34/15/04 performs the necessary modulation/demodulation of the data and provides two options for message packet structure (Protocol 1 and Protocol 2, as defined in ETSI ES 201 912). The rest of the data link layer and transfer layer are defined by the host system.

The content of the message is entirely up to the host including any checksum or CRC. ETSI ES 201 912 describes two standard data and transfer layers that are commonly used. SMS typically relies on caller identification information to determine if the call should be answered using an SMS device or not.

See "6.4. SMS Support" in AN93 for more information on how to configure the modem for SMS support.

### 4.18. Codec Interface (24-Pin Version Only)

In order to support a full range of voice and data applications, the Si2457/34/15/04 includes an optional serial interface that connects to an external voice codec (Si3000). See AN93 for complete details.

# 4.19. EEPROM Interface (24-Pin Version Only)

The Si2457/34/15/04 supports an optional serial peripheral interface (SPI) bus serial EEPROM Mode 3 with a 16-bit (8–64 kbit range) address. Upon powerup, if a pulldown resistor  $\leq\!10~k\Omega$  is placed between D6 and GND, the ISOmodem attempts to detect an EEPROM. The EEPROM is intended first for setting custom defaults, second for automatically loading firmware upgrades, and third to allow for user-defined AT command macros for use in custom AT commands or country codes. See AN93 for complete details.

#### 4.20. AT Commands

At powerup, the Si2457/34/15/04 is in the AT command mode. In command mode, the modem monitors the input (serial or parallel) checking constantly for a valid command (AT commands are described in Table 8.)



Table 8. Basic AT Command Set (Command Defaults in Bold)

Command		Action
\$	Display AT command mode setti	ngs.
Α	Answer incoming call	
A/	Re-execute last command. This is the only command not preceded by "AT" or followed by a <cr>.</cr>	
Dn	Dial The dial command, followed by 1 number:  Modifier ! or & , or < ; @  G	Function  Flash hook switch for FHT (U4F) ms (default: 500 ms)  Pause before continuing for S8 seconds (default: 2 seconds)  Return to AT command mode  Wait for silence.  Polarity reversal detect. By placing the "G" character in the dial string (i.e. ATDTG1), the Si2457/34/15/04 will monitor the telephone line for polarity reversals. If a busy tone is detected, the Si2457/34/15/04 will report "POLARITY REVERSAL" if a polarity reversal was detected or "NO POLARITY REVERSAL" if a polarity reversal was not detected. In each case, the result code is followed by "OK". If the S7 timeout occurs before a busy tone is detected, the Si2457/34/15/04 will report "NO CARRIER". Polarity reversal monitoring begins after the last digit is dialed and ends when the busy tone is detected or S7 timeout occurs.  Note: It is not possible to establish a modem connection when using this command.
	L	Redial last number.  Pulse (rotary) dialing—pulse digits: 0, 1, 2, 3, 4, 5, 6, 7,
	Р	8, 9
	Т	Tone (DTMF) dialing—DTMF digits: *, #, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.
	W	Wait for dial tone before continuing for S14 seconds (default: 12 seconds). Blind dialing modes X0, X1 and X3 do not affect the W command.  If the DOP bit (U7A, bit 7) is set, the "ATDTW" command will cause the ISOmodem® to pause dialing and either report an "OK" if a dialtone is detected or "NO DIALTONE" if a dial tone is not detected.
En	Local DTE echo	
E0	Disable	
E1	Enable	
Hn	Hook switch.	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
H0	Go on-hook (hang up modem).
H1	Go off-hook.
In	Identification and checksum.
10	Display Si2457/34/15/04 revision code. B: Revision B C: Revision C, etc.
I1	Display Si2457/34/15/04 firmware revision code (numeric).
13	Display line-side revision code.  18C = Si3018 revision C
16	Display the ISOmodem <sup>®</sup> model number.  "2404" = Si2404  "2415" = Si2415  "2434" = Si2434  "2457" = Si2457
17	Diagnostic results 1. See "AN93: ISOModem® Chipset Family Designer's Guide" for details.
18	Diagnostic results 2. See AN93 for details.
Ln	Speaker volume operation
L1	Low speaker volume
L2	Medium speaker volume
L3	High speaker volume
Mn	Speaker operation (via AOUT).
МО	Speaker is always off.
M1	Speaker is on while dialing and handshaking; off in data mode.
M2	Speaker is always on.
M3	Speaker is off while dialing, on during handshaking and retraining.
On	Return to data mode from Command mode operation.
00	Return to data mode.
01	Return to data mode and perform a full retrain (at any speed except 300 bps).
O2	Return to data mode and perform rate renegotiation.
Qn	Response mode.
Q0	Enable result codes (see Table 12 on page 38)
Q1	Disable result codes (enable quiet mode).
R	Initiate V.23 reversal.
Sn	S-register operation (see Table 13 on page 41).
S\$	List contents of all S registers.
Sn?	Display contents of S-register n.



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
Sn=x	Set S-register n to value x (where n and x are decimal values).
Vn	Result code type (see Table 12 on page 38).
V0	Numeric result codes.
V1	Verbal result codes
Xn	Call Progress Monitor (CPM)—This command controls which CPM signals are monitored and reported to the host from the Si2457/34/15/04. (See Table 12 on page 38.)
X0	Basic results; disable CPM—Blind dial (does not wait for dial tone). CONNECT message does not include speed.
X1	Extended results; disable CPM—Blind dial. CONNECT message includes speed.
X2	Extended results and detect dial tone only—Add dial tone detection to X1 mode. Does not blind dial.
X3	Extended results and detect busy only—Add busy tone detection to X1 mode.
X4	Extended results, full CPM—Full CPM enabled, CONNECT message includes speed.
X5	Extended results—Full CPM enabled including ringback detection. Adds ringback detection to X4 mode.
Yn	Long space disconnect—Modem hangs up after 1.5 seconds or more of continuous space while on-line.
Υ0	Disable.
Y1	Enable.
Z	Hard Reset—This command is functionally equivalent to pulsing the RESET pin low. (See t <sub>AT</sub> in Table 6 on page 7.)
:E	Read from serial EEPROM.
:I	Interrupt Read—This command causes the ISOmodem <sup>®</sup> to report the lower 8 bits of the interrupt register I/O Control 0 (U70). The CID, OCD, PPD, and RI bits also are cleared, and the INT pin (INT bit in parallel mode) is deactivated on this read.
:M	Write to serial EEPROM.
:Р	Program RAM Write—This command is used to upload firmware supplied by Silicon Labs to the Si2457/34/15/04. The format for this command is AT:Paaaa,xxxx,yyyy, where aaaa is the first address in hexadecimal and xxxx,yyyy, is data in hexadecimal. Only one :P command is allowed per AT command line. No other commands can be concatenated in the :P command line. This command is <i>only</i> for use with special files provided by Silicon Laboratories. Do not attempt to use this command for any other purpose.
:R	User-Access Register Read—This command allows the user to read from the user-access registers (see "6. User-Access Registers (U-Registers)" on page 44). The format is "AT:Raa", where:  aa = user-access address in hexadecimal.  The "AT:R" command causes all the U- registers to be displayed.



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action	
:U	User-Access Register Write—This command allows the user to write to the 16-bit user-access registers. (See page page 44.) The format is "AT:Uaa,xxxx,yyyy,zzzz," where aa = user-access address in hexadecimal.  xxxx = Data in hexadecimal to be written to location aa.  yyyy = Data in hexadecimal to be written to location (aa + 1).  zzzz = Data in hexadecimal to be written to location (aa + 2).  etc.	
+DR=X	Data compression reporting.  X Mode  O Disabled  1 Enabled  If enabled, the intermediate result code is transmitted at the point after error control negotiation. The format of this result code is as follows:  Result code Mode  +DR:NONE Data compression is not in use  +DR:V42B Rec. V.42bis is in use in both directions  +DR:V42B RD Rec. V.42bis is in use in receive direction only  +DR:V42B TD Rec. V.42bis is in use in transmit directions only	
+DS Options +DS = A +DS = A,B +DS = A,B,C +DS = A,B,C,D	Controls V.42bis data compression function.  A Direction  0 No compression  1 Transmit only  2 Receive only  3 Both Directions  B Compression_negotiation  0 Do not disconnect if V.42 is not negotiated.  1 Disconnect is V.42 is not negotiated.  C Maximum dictionary size  512  D Maximum string size  6 to 250 (28 default)	
+ES Options +ES = A +ES = A,,C	<ul> <li>Enable synchronous access mode.</li> <li>A Specifies the mode of operation when initiating a modem connection.</li> <li>D Disable synchronous assess mode.</li> <li>6 Enable synchronous access mode when connection is completed and data state is entered.</li> <li>B Specifies fallback mode of operation.</li> <li>This parameter should not be used.</li> <li>C Specifies the mode of operation when answer a modem connection.</li> <li>D Disable synchronous assess mode.</li> <li>8 Enable synchronous access mode when connection is completed and data state is entered.</li> </ul>	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
+ESA Options +ESA = A +ESA = A,B +ESA = A,B,C +ESA = A,B,C,E +ESA = A,B,C,E,F G	Synchronous access mode control options  A Specifies action taken if an underrun condition occurs during transparent sub-mode.  0 Modem transmits 8-bit SYN sequences on idle.  B Specifies action taken if an underrun condition occurs after a flag during framed sub-mode  0 Modem transmits 8-bit HDLC flags on idle.  C Specifies action taken if an underrun or overrun condition occurs after a non-flag during framed sub-mode.  0 Modem transmits abort on underrun in middle of frame.  1 Modem transmits flag on underrun in middle of frame and notifies host of underrun or overrun.  D Specifies V.34 half duplex operation.  This parameter should not be used.  E Specifies CRC polynomial used while in framed sub-mode.  0 CRC generation checking disable.  1 16-bit CRC generation and checking is performed by the modem.  F Specifies NRZI encoding and decoding.  0 NRZI encoding and decoding disabled.  G Specifies SYN.  255
+FCLASS = X	Class 1 Mode Enable for V.29 fast connect.  X
+FRM = X	Class 1 Receive Carrier for V.29 fast connect.  X Mode  Transmit V.21 (980 Hz) tone for longer than 100 ms, then send answer tone (2100/2225 Hz) for 200 ms.  V.29 short synchronous.  V.29 full synchronous.
+FTM = X	Class 1 Transmit Carrier for V.29 fast connect.  X



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Country settings - Automatically configure all registers for a particular country  Country  Japan  Australia  Austria  FBelgium  Belgium  Bulgaria	ountry.
0 Japan 9 Australia A Austria F Belgium 16 Brazil 1B Bulgaria	
0 Japan 9 Australia A Austria F Belgium 16 Brazil 1B Bulgaria	
A Austria F Belgium 16 Brazil 1B Bulgaria	
F Belgium 16 Brazil 1B Bulgaria	
16 Brazil 1B Bulgaria	
1B Bulgaria	
20 Canada	
26 China	
27 Columbia	
2E Czech Republic	
31 Denmark	
35 Ecuador	
3C Finland	
3D France	
42 Germany	
46 Greece	
50 Hong Kong	
51 Hungary	
53 India	
57 Ireland	
58 Israel	
+GCI = X 59 Italy	
61 South Korea	
69 Luxembourg 6C Malaysia	
6C Malaysia 73 Mexico	
75 Mexico 7B Netherlands	
7E New Zealand	
82 Norway	
87 Paraguay	
89 Philippines	
8A Poland	
8B Portugal	
9C Singapore	
9F South Africa	
A0 Spain	
A5 Sweden	
A6 Switzerland	
B8 Russia	
B4 United Kingdom	
B5 United States	
FE Taiwan	
Note: U-registers are configured to Silicon Laboratories' recommended values	. The +GCI command
resets the U-registers and the S7 and S6 S-registers to default values be	efore setting country-
specific values. Changes may be made by writing individual registers after	
command. Refer to "AN93: ISOModem® Chipset Family Designer's Guid	de" for details.
+GCI? List current country code setting (response is: + GCI: <setting>)</setting>	
+GCI = ? List all possible country code settings.	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action	
+IFC Options +IFC = A +IFC = A,B	Specifies the flow control to be implemented.  A Specifies the flow control method used by the host to control data from the modem  0 None  1 Local XON/OFF flow control. Does not pass XON/XOFF character to the remote modem.  2 Hardware flow control (RTS)  B Specifies the flow control method used by the modem to control data from the host 0 None  1 Local XON/OFF flow control.  2 Hardware flow control (CTS).	
+ITF Options +ITF = A +ITF = A,B +ITF = A,B,C	Transmit flow control threshold.  A Threshold above which the modem will generate a flow off signal <0 to 511> bytes  B Threshold below which the modem will generate a flow on signal <0 to 511> bytes  C Polling interval for <em><bnum> indicator 0 to 300 in 10 msec units.</bnum></em>	
+MR = X	Modulation reporting control.  X Mode  O Disabled  1 Enabled  If enabled, the intermediate result code is transmitted at the point during connect negotiation.  The format of this result code is as follows:  +MCR: <carrier> e.g. +MCR: V32B  +MRR: <rate> e.g. +MRR: 14400</rate></carrier>	
+MS Options +MS = A +MS = A,B +MS = A,B,C +MS = A,B,C,D +MS = A,B,C,D,E +MS = A,B,C,D,E,F	Modulation Selection.  A Preferred modem carrier V21 ITU-T V.21 V22 ITU-T V.22 V22B ITU-T V.22bis (default for Si2404) V32 ITU-T V.32 V32B ITU-T V.32bis (default for Si2415) V34 ITU-T V.34 (default for Si2434) V90 ITU-T V.90 (default for Si2457)  B Automatic modulation negotiation 0 Disabled 1 Enabled  C,D Min TX rate/Max TX rate are optional numeric values that specify the lowest value at which the DCE may establish a connection. If unspecified (set to 0), they are determined by the carrier and automode settings.  E,F Min RX rate/Max RX rate are optional numeric values which specify the highest value at which the DCE may establish a connection. If unspecified (set to 0), they are determined by the carrier and automode settings.	



Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action	
	Controls the action to be taken upon detection of call waiting.	
	X Mode	
+PCW = X	0 Toggle RI and collect type II Caller ID if enabled by +VCID.	
	1 Hang up.	
	2 Ignore call waiting.	
	Caller ID Type.	
	X Mode	
+VCDT = X	0 After ring only	
+VCD1 = X	1 Always on (Recommended Setting)	
	2 UK	
	3 Japan	
	Caller ID Enable.	
	X Mode	
+VCID = X	0 Off	
	1 On—formatted	
	2 On—raw data format	
+VCIDR?	Type II caller ID information — The Si2457/34/15/04 will display "+VCDIR:" followed by raw caller ID information including checksum.	



### 4.21. Extended AT Commands

The extended AT commands are supported by the Si2457/34/15/04 and are described in Tables 9 through 11.

Table 9. Extended AT& Command Set (Command Defaults in Bold)

Command	Action
&\$	Display AT& current settings.
&D0	ESC is not used
&D1	ESC escapes to command mode from data mode if also enabled by HES U70, bit 15.
&D2	ESC assertion during a modem connection causes the modem to go on-hook and return to command mode.
&D3	ESC assertion causes ATZ command (reset and return OK result code).
&F	Restore factory default settings.
&Gn	Line connection rate limit—This command sets an upper limit on the line speed that the Si2457/34/15/04 can connect. Note that the &Hn commands may limit the line speed as well (&Gn not used for &H0 or &H1). Not all modulations support rates given by &G. Any improper setting will be ignored.
&G3	1200 bps max
&G4	2400 bps max (default for Si2404)
&G5	4.8 kbps max
&G6	7.2 kbps max
&G7	9.6 kbps max
&G8	12 kbps max
&G9	14.4 kbps max (default for Si2415)
&G10	16.8 kbps max
&G11	19.2 kbps max
&G12	21.6 kbps max
&G13	24 kbps max
&G14	26.4 kbps max
&G15	28.8 kbps max
&G16	31.2 kbps max
&G17	33.6 kbps max (default for Si2457 and Si2434)
&Hn	Switched network handshake mode—&Hn commands must be on a separate command line from ATD, ATA, or ATO commands.
&H0	V.90 with automatic fallback (56 kbps to 300 bps) (default for Si2457)
&H1	V.90 only (56 kbps to 28 kbps)
&H2	V.34 with automatic fallback (33.6 kbps to 300 bps) (default for Si2434)
&H3	V.34 only (33.6 kbps to 2400 bps)



Table 9. Extended AT& Command Set (Command Defaults in Bold) (Continued)

Command	Action
&H4	ITU-T V.32bis with automatic fallback (14.4 kbps to 300 bps) (default for Si2415)
&H5	ITU-T V.32bis only (14.4 kbps to 4800 bps)
&H6	ITU-T V.22bis only (2400 bps or 1200 bps)
&H7	ITU-T V.22 only (1200 bps)
&H8	Bell 212 only (1200 bps)
&H9	Bell 103 only (300 bps)
&H10	ITU-T V.21 only (300 bps)
&H11	V.23 (1200/75 bps)
&Pn	Japan pulse dialing
&P0	Configure Si2457/34/15/04 for 10 pulse-per-second pulse dialing. For Japan.
&P1	Configure Si2457/34/15/04 for 20 pulse-per-second pulse dialing. For Japan.
&Tn	Test mode
&T0	Cancel test mode (Escape to command mode to issue AT&T0). This command will also report the number of bit errors encountered on the previous &T4 or &T5 test.
&T2	Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &H AT command. Test loop is through the DSP (Si2457/34/15/04 device) only. ISOmodem® echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode).
&T3	Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &H AT command. Test loop is through the DSP (Si2457/34/15/04), DAA interface section (Si2457/34/15/04), DAA interface (Si3018), and analog hybrid circuit (Si3018). ISOmodem echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode). Phone line termination required as in Figure 1. To test only the link operation, the hybrid and AFE codec can be removed from the test loop by setting the DL bit (U62, bit 1).
&T4	Initiate transmit as originating modem with automatic data generation. Modulation, data rate, and symbol rate are set by &H, &G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &T0.
&T5	Initiate transmit as answering modem with automatic data generation. Modulation, data rate, and symbol rate are set by &H, &G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &T0.
&T6	Compute checksum for firmware-upgradeable section of program memory. If no firmware upgrade is installed, &T6 returns 0x4474.
&Xn	Automatic determination of telephone line type.
&X0	Abort &x1 or &x2 command.



# Si2457/34/15/04

Table 9. Extended AT& Command Set (Command Defaults in Bold) (Continued)

Command	Action
&X1	Automatic determination of telephone line type.  Result code: WXYZn  W: 0 = line supports DTMF dialing.
&X2	Same as &X1, but Y result (PBX) is not tested.
*Y2A	Produce a constant answer tone (ITU-T) and return to command mode. The answer tone continues until the ATH command is received or the S7 timer expires.
&Z	Enter low-power wake-on-ring mode.



Table 10. Extended AT% Command Set (Command Defaults in Bold)

Command	Action
%\$	Display AT% command settings.
%B	Report blacklist. See also S42 register.
%Cn	Data compression
%C0	Disable V.42bis and MNP5 data compression
%C1	Enable V.42bis in transmit and receive paths. If MNP is selected (\N2), then %C1 enables MNP5 in transmit and receive paths.
%C2	Enable V.42bis in transmit path only.
%C3	Enable V.42bis in receive path only.
%On	Answer mode.
%O1	Si2457/34/15/04 will auto-answer a call in answer mode.
%O2	Si2457/34/15/04 will auto-answer a call in originate mode.
%Vn	Automatic Line Status Detection.  After the %V1 and %V2 commands are issued, the Si2457/34/15/04 will automatically check the telephone connection for whether or not a line is present. If a line is present, the Si2457/34/15/04 will automatically check if the line is already in use. Finally, the Si2457/34/15/04 will check line status both before going off-hook and again before dialing. %V1 uses the fixed method, and %V2 uses the adaptive method. %V0 (default) disables this feature.
%V0	Disable automatic line-in-use detection.
%V1	Automatic Line Status Detection—Fixed Method.  Description: Before going off-hook with the ATD, ATO, or ATA commands, the Si2457/34/15/04 compares the line voltage (via LVCS) to registers NOLN (U83) and LIUS (U84):
	Loop VoltageAction $0 \le LVCS \le NOLN$ Report "NO LINE" and remain on-hook. $NOLN \le LVCS \le LIUS$ Report "LINE IN USE" and remain on-hook. $LIUS \le LCVS$ Go off-hook and establish a modem connection.
	Once the call has begun, the off-hook intrusion algorithm (described in "4.12.2. Off-Hook Intrusion Detection" on page 19) operates normally. In addition, the Si2457/34/15/04 will report "NO LINE" if the telephone line is completely disconnected. If the HOI bit (U77, bit 11) is set, "LINE IN USE" is reported upon intrusion.



Table 10. Extended AT% Command Set (Command Defaults in Bold) (Continued)

Command		Action	
%V2	Automatic Line Status Detection—Adaptive Method.		
	Description: Before going off-hook with the ATD, ATO, or ATA commands, the Si2457/34/15/04 com		
	pares the line voltage (via LVCS) to the NLIU (U85) register:		
	Loop Voltage	<u>Action</u>	
	$0 \le LVCS \le (0.0625 \times NLIU)$	Report "NO LINE" and remain on-hook.	
	(0.0625 x NLIU) < LVCS ≤ (0.85 x NLIU)	Report "LINE IN USE" and remain on-hook.	
	(0.85 x NLIU) < LCVS	Go off-hook and establish a modem connection.	
	The NLIU register is updated every 1 ms with the minimum non-zero value of LVCS in the last		
	30 ms. This allows the Si2457/34/15/04 to eliminate errors due to 50/60 Hz interference and also		
	adapt to relatively slow change in the on-hook dc reference value on the telephone line. This algo-		
	rithm does not allow any non-zero values for NLIU below 0x0007. The host may also initialize NLIU		
	prior to issuing the %V2 command. Once the call has begun, the off-hook intrusion algorithm		
	(described in "4.12.2. Off-Hook Intrusion Detection" on page 19) operates normally. In addition, the		
	Si2457/34/15/04 will report "NO LINE" if the telephone line is completely disconnected. If the HOI		
	(U77, bit 11) bit is set, "LINE IN USE" is re	eported upon intrusion.	



Table 11. Extended AT\ Command Set (Command Defaults in Bold)

Command	Action
\\$	Display AT\ command settings.
\Bn	Character length will be automatically set in autobaud mode
\B0	6N1—six data bits, no parity, one stop bit, one start bit, eight bits total (\N0 only) <sup>1</sup>
\B1	7N1—seven data bits, no parity, one stop bit, one start bit, nine bits total (\N0 only) <sup>1</sup>
\B2	7P1—seven data bits, parity optioned by \P, one stop bit, one start bit, 10 bits total
\B3	8N1—eight data bits, no parity, one stop bit, one start bit, 10 bits total
\B5	8P1—eight data bits, parity optioned by \P, one stop bit, one start bit, 11 bits total (\N0 only)
\B6	8X1—eight data bits, one escape bit, one stop bit, one start bit, 11 bits total (enables ninth-bit escape mode)
\Nn	Asynchronous protocol
\N0	Wire mode (no error correction, no compression)
\N2	MNP reliable mode. The Si2457/34/15/04 attempts to connect with the MNP protocol. If unsuccessful, the call is dropped.
\N3	V.42 auto-reliable—The Si2457/34/15/04 attempts to connect with the V.42 protocol. If unsuccessful, the MNP protocol is attempted. If unsuccessful, wire mode is attempted.
\N4	V.42 (LAPM) reliable mode (or drop call)—Same as \N3 except that the Si2457/34/15/04 drops the call instead of connecting in MNP or wire mode.
\N5	V.42 and MNP reliable mode—The Si2457/34/15/04 attempts to connect with V.42. If unsuccessful, MNP is attempted. If MNP us unsuccessful, the call is dropped.
\Pn	Parity type will be automatically set in autobaud mode
\P0	Even
\P1	Space <sup>1</sup>
\P2	Odd
\P3	Mark <sup>1</sup>
\Qn	Modem-to-DTE flow control
\Q0	Disable all flow control—This may only be used if the DTE speed and the VF speed are guaranteed to match throughout the call.
\Q2	Use CTS only

- 1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
- 2. The autobaud feature does not detect this rate.
- 3. Default is \T9 if a pulldown resistor is connected to the autobaud strap pin; otherwise, the default is \T16.



Table 11. Extended AT\ Command Set (Command Defaults in Bold) (Continued)

Command	Action
\Q3	Use RTS/CTS
\Q4	Use XON/XOFF flow control for modem-to-DTE interface. Does not enable modem-to-modem flow control.
\Tn	DTE rate—Change DTE rate. When the Si2457/34/15/04 is configured in autobaud mode (default), \T0 through \T15 will lock the new baud rate and disable autobaud. When the ISOmodem <sup>®</sup> is not in autobaud mode (the autobaud strap pin low on powerup), the result code "OK" is sent at the old DTE rate. Subsequent commands must be sent at the new rate.
\T0	300 bps
\T1	600 bps
\T2	1200 bps
\T3	2400 bps
\T4	4800 bps
\T5	7200 bps
\T6	9600 bps
\T7	12.0 kbps <sup>2</sup>
\T8	14.4 kbps
\T9	19.2 kbps <sup>3</sup>
\T10	38.4 kbps
\T11	57.6 kbps
\T12	115.2 kbps
\T13	230.4 kbps
\T14	245.760 kbps <sup>2</sup>
\T15	307.200 kbps
\T16	Autobaud on <sup>3</sup>
\T17	Autobaud off; lock at current baud rate.

1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.

Rev. 1.3

- 2. The autobaud feature does not detect this rate.
- 3. Default is \T9 if a pulldown resistor is connected to the autobaud strap pin; otherwise, the default is \T16.

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Table 11. Extended AT\ Command Set (Command Defaults in Bold) (Continued)

Command	Action
\U	Serial mode—causes a low pulse (25 ms) on $\overline{\text{RI}}$ and $\overline{\text{DCD}}$ . $\overline{\text{INT}}$ to be the inverse of ESC. $\overline{\text{RTS}}$ to be inverse of $\overline{\text{CTS}}$ .  Parallel mode—causes a low pulse (25 ms) on $\overline{\text{INT}}$ .  This command terminates with a $\overline{\text{RESET}}$ .
\Vn	Connect message type
\V0	Report connect message and protocol message
\V2	Report connect message only (exclude protocol message)
\V4	Report connect and protocol message with both upstream and downstream connect rates.

- 1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
- 2. The autobaud feature does not detect this rate.
- 3. Default is \T9 if a pulldown resistor is connected to the autobaud strap pin; otherwise, the default is \T16.



Table 12. Result Codes

Numeric	Meaning	Verbal Response	X0	X1	X2	Х3	X4	X5	
0	Command was successful	OK	Х	Х	Х	Х	Х	Χ	
1	Link established at 300 bps or higher	CONNECT	Х	Х	Х	Х	Х	Х	
2	Incoming ring detected	RING	Χ	Χ	Χ	Χ	Χ	Χ	
3	Link dropped	NO CARRIER	Χ	Х	Χ	Χ	Χ	Χ	
4	Command failed	ERROR	Χ	Χ	Χ	Χ	Χ	Χ	
5	Link establish at 1200 CONNECT 1200		Χ	Χ	Χ	Χ	Χ		
6	Dial tone not present	NO DIALTONE			Χ		Χ	Χ	
7	Line busy	Line busy BUSY				Χ	Χ	Χ	
8	Remote not answering	NO ANSWER	Х	Χ	Χ	Χ	Χ	Χ	
9	Ringback detected	RINGING						Χ	
10	Link established at 2400	CONNECT 2400		Χ	Χ	Χ	Χ	Χ	
11	Link established at 4800	CONNECT 4800 <sup>1</sup>		Х	Χ	Х	Х	Χ	
12	Link established at 9600	CONNECT 9600 <sup>1</sup>		Х	Χ	Х	Х	Χ	
14	Link established at 19200	CONNECT 19200 <sup>1</sup>		Х	Х	Х	Х	Х	
15	Link established at 7200	CONNECT 7200 <sup>1</sup>		Х	Х	Х	Х	Х	
16	Link established at 12000	CONNECT 12000 <sup>1</sup>		Х	Х	Х	Х	Х	
17	Link established at 14400	CONNECT 14400 <sup>1</sup>		Х	Х	Х	Х	Χ	
18	Link established at 16800	CONNECT 16800 <sup>2</sup>		Х	Х	Х	Х	Χ	
19	Link established at 21600	CONNECT 21600 <sup>2</sup>		Х	Х	Х	Х	Х	
20	Link established at 24000	CONNECT 24000 <sup>2</sup>		Х	Х	Х	Х	Х	
21	Link established at 26400	CONNECT 26400 <sup>2</sup>		Х	Х	Х	Х	Х	
22	Link established at 28800	CONNECT 28800 <sup>2</sup>		Х	Х	Х	Х	Х	
23	Link established at 31200	CONNECT 31200 <sup>2</sup>		Х	Х	Х	Х	Х	
24	Link established at 33600	CONNECT 33600 <sup>2</sup>		Х	Х	Х	Х	Х	
30	Caller ID mark detected	CIDM	Х	Х	Х	Х	Х	Х	
31	Hookswitch flash detected	FLASH	Х	Х	Х	Х	Х	Х	
32	UK CID State Tone Alert Signal detected	STAS	Х	Х	Х	Х	Х	Х	
33	Overcurrent condition	X <sup>2</sup>	Х	Х	Х	Х	Х	Х	
40	Blacklist is full	BLACKLIST FULL (enabled via S42 register)	Х	Х	Х	Х	Х	Х	
41	Attempted number is black-listed.	BLACKLISTED (enabled via S42 register)	Х	Х	Х	Х	Х	Х	
42	No phone line present	NO LINE (enabled via %Vn commands)	Х	Х	Х	Х	Х	Х	

- 1. This message is only supported on the Si2457, Si2434, and Si2415.
- 2. This message is only supported on the Si2457 and Si2434.
- 3. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
- **4.** This message is only supported on the Si2457.



**Table 12. Result Codes (Continued)** 

Numeric	Meaning	Verbal Response	X0	X1	X2	Х3	X4	X5
43	Telephone line is in use	LINE IN USE (enabled via %Vn commands)	Х	Х	Х	Х	Х	Х
44	A polarity reversal was detected	POLARITY REVERSAL (enabled via G modifier)	Х	Х	Х	Х	Х	Х
45	A polarity reversal was NOT detected	NO POLARITY REVERSAL (enabled via G modifier)	Х	Х	Х	Х	Х	Х
52	Link established at 56000	CONNECT 56000 <sup>4</sup>		Χ	Χ	Х	Х	Х
60	Link established at 32000	CONNECT 32000 <sup>4</sup>		Χ	Χ	Х	Х	Х
61	Link established at 48000	CONNECT 48000 <sup>4</sup>		Х	Х	Х	Х	Х
63	Link established at 28000	CONNECT 28000 <sup>4</sup>		Х	Х	Х	Х	Х
64	Link established at 29333	CONNECT 29333 <sup>4</sup>		Χ	Χ	Χ	Χ	Х
65	Link established at 30666	CONNECT 30666 <sup>4</sup>		Χ	Χ	Χ	Χ	Х
66	Link established at 33333	CONNECT 33333 <sup>4</sup>		Χ	Χ	Χ	Χ	Х
67	Link established at 34666	CONNECT 34666 <sup>4</sup>		Χ	Χ	Х	Х	Х
68	Link established at 36000	CONNECT 36000 <sup>4</sup>		Х	Х	Х	Х	Х
69	Link established at 37333	CONNECT 37333 <sup>4</sup>		X X X		Х	Х	
70	No protocol	PROTOCOL: NONE		Set with \V0 command.				
75	Link established at 75	CONNECT 75		Χ	Χ	Χ	Χ	Х
77	V.42 protocol	PROTOCOL: V42	Set with \V0 command.					
79	V.42bis protocol	PROTOCOL: V42bis		Set v	with \V(	) comm	nand.	
80	MNP2 protocol	PROTOCOL: ALTERNATE, + CLASS 2		Set with \V command.				
81	MNP3 protocol	PROTOCOL: ALTERNATE, + CLASS 3		Set	with \V	comm	and.	
82	MNP4 protocol	PROTOCOL: ALTERNATE, + CLASS 4		Set	with \V	comm	and.	
83	MNP5 protocol	PROTOCOL: ALTERNATE, + CLASS 5		Х	Х	Х	Х	Х
90	Link established at 38666	CONNECT 38666 <sup>4</sup>		Χ	Χ	Χ	Χ	Х
91	Link established at 40000	CONNECT 40000 <sup>4</sup>		Х	Х	Х	Х	Х
92	Link established at 41333	CONNECT 41333 <sup>4</sup>		Х	Х	Х	Х	Х
93	Link established at 42666	CONNECT 42666 <sup>4</sup>		Х	Х	Х	Х	Х
94	Link established at 44000	CONNECT 44000 <sup>4</sup>		Х	Х	Х	Х	Х
95	Link established at 45333	CONNECT 45333 <sup>4</sup>		Х	Х	Х	Х	Х
96	Link established at 46666	CONNECT 46666 <sup>4</sup>		Х	Х	Х	Х	Х
97	Link established at 49333	CONNECT 49333 <sup>4</sup>		Х	Х	Х	Х	Х
98	Link established at 50666	CONNECT 50666 <sup>4</sup>		Х	Х	Х	Х	Х
						•	•	•

- 1. This message is only supported on the Si2457, Si2434, and Si2415.
- 2. This message is only supported on the Si2457 and Si2434.
- 3. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
- 4. This message is only supported on the Si2457.



**Table 12. Result Codes (Continued)** 

Numeric	Meaning	Verbal Response	X0	X1	X2	Х3	X4	X5
99	Link established at 52000	CONNECT 52000 <sup>4</sup>		Х	Х	Х	Х	Х
100	Link established at 53333	CONNECT 53333 <sup>3</sup>		Χ	Х	Χ	Х	Х
101	Link established at 54666	CONNECT 54666 <sup>3</sup>		Χ	Х	Χ	Х	Х
102	DTMF dial attempted on a pulse dial only line	UN-OBTAINABLE NUMBER	Х	Х	Х	Х	Х	Х

- 1. This message is only supported on the Si2457, Si2434, and Si2415.
- 2. This message is only supported on the Si2457 and Si2434.
- **3.** X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.
- 4. This message is only supported on the Si2457.



# 5. S-Registers

The S command allows reading (Sn?) or writing (Sn = x) the S-registers. The S-registers store values for functions that typically are rarely changed, such as timers or counters, and the ASCII values of control characters, such as carriage return. Table 13 summarizes the S-register set.

**Table 13. S-Register Description** 

	Definition			
S-Register (Decimal)	Function	Default (Decimal)	Range	Units
0	Automatic answer—Number of rings the Si2457/34/15/04 must detect before answering a call. 0 disables auto answer.	0	0–255	Rings
1	Ring counter.	0	0–255	Rings
2	ESC code character.	43 (+)	0–255	ASCII
3	Carriage return character.	13 (CR)	0–255	ASCII
4	Linefeed character.	10 (LF)	0–255	ASCII
5	Backspace character.	08 (BS)	0–255	ASCII
6	Dial tone wait timer—Number of seconds the Si2457/34/15/04 waits before blind dialing. Only applicable if blind dialing is enabled (X0, X1, X3).	02	0–255	seconds
7	Carrier wait timer—Number of seconds the Si2457/34/15/04 waits for carrier before timing out. This register also sets the number of seconds the modem waits for ringback when originating a call before hanging up. This register also sets the number of seconds the answer tone will continue while using the AT*Y2A command.	80	0–255	seconds
8	Dial pause timer for , and < dial command modifiers.	02	0–255	seconds
9	Carrier presence timer—Time after a loss of carrier that a carrier must be detected before reactivating DCD. S9 is referred to as "carrier loss debounce time."	06	1–255	0.1 second
10	Carrier loss timer—Time the carrier must be lost before the Si2457/34/15/04 disconnects. Setting 255 disables disconnect entirely. If S10 is less than S9, even a momentary loss of carrier causes a disconnect.	14	1–255	0.1 second
12	Escape code guard timer—Minimum guard time required before and after "+++" for the Si2457/34/15/ 04 to recognize a valid escape sequence.	50	1–255	0.02 second
14	Wait for dial tone delay value (in relation to the W dial modifier). Starts when "W" is executed in the dial string.	12	0–255	seconds



**Table 13. S-Register Description (Continued)** 

	Definition			
S-Register (Decimal)	Function	Default (Decimal)	Range	Units
24	Sleep Inactivity Time—Sets the time that the modem operates in normal power mode with no activity on the serial port, parallel port, or telephone line before entering low-power sleep mode. This feature is disabled if the timer is set to 0.	0	0–255	seconds
30	Disconnect Activity Timer—Sets the length of time that the modem stays online before disconnecting with no activity on the serial port, parallel port, or telephone line (Ring, hookswitch flash, or caller ID). This feature is disabled if set to 0.	0	0–255	minutes
38	Hang Up Delay Time—Maximum delay between receipt of ATH0 command and hang up. If time out occurs before all data can be sent, the NO CARRIER (3) result code is sent (operates in V.42 mode only). "OK" response is sent if all data is transmitted before timeout. S38 = 255 disables timeout and modem disconnects only if data is successfully sent or carrier is lost.	20	0–255	seconds
40	Data Pattern—Data pattern generated during &T4 and &T5 transmit tests. <b>0 = All spaces (0s)</b> 1 = All marks (1s)  2 = Random data	0	0–2	
41	V.34 symbol rate - Symbol rate for V.34 when using the &T4 and &T5 commands. <b>0 = 2400</b>	0	0–5	



Table 13. S-Register Description (Continued)

	Definition			
S-Register (Decimal)	Function	Default (Decimal)	Range	Units
42	Blacklisting—The Si2457/34/15/04 will not dial the same number more than two times in three minutes. An attempt to dial a third time within three minutes will result in a "BLACKLISTED" result code. If the blacklist memory is full, any dial to a new number will result in a "BLACKLIST FULL" result code. Numbers are added to the blacklist only if the modem connection fails. The %B command will list the numbers on the blacklists. <b>0</b> = disabled  1 = enabled	0 (disabled)	0–1	
43	Dial Attempts to Blacklist.  When blacklisting is enabled with S42, this value controls the number of dial attempts that will result in a number being blacklisted.	4	0–4	
44	Blacklist Timer. Period during which blacklisting is active.	180	0–255	seconds
50	Minimum on-hook time—Modem will remain on-hook for S50 seconds. Any attempt to go off-hook will be delayed until this timer expires.	3	0–255	seconds
51	Number to start checking for an outside line on a PBX. See &X command for details.	1	0–9	



# 6. User-Access Registers (U-Registers)

U-Registers are 16-bit registers written by the AT:Uaa command and read by the AT:R (read all U-Registers) or AT:Raa (read U-Register aa) commands (see the AT command list in Table 11 on page 35). Many aspects of the modem's and DAA's behavior can be enabled/disabled, configured, monitored, and/or modified through U-Registers; however, most of them will not be needed in normal use.

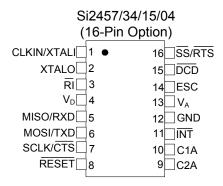
There are two types of U-Registers. The first represents a single 16-bit term, such as a filter coefficient, threshold, delay, or other quantity. These registers can be read from or written to as a single 16-bit value. The second type of U-Register is bit-mapped. Bit-mapped registers are written and/or read in hexadecimal, but each bit or combination of bits in the register represents an independent value or status information. These individual bits are used to enable or disable features and indicate states.

Some U-Registers are reserved and not available to the user. Therefore, there are gaps in the available U-Register address map. Additionally, some bits within available U-Registers are reserved. Any attempt to write a non-zero value to a reserved U-Register or bit may cause unpredictable modem operation.

With over 100 U-Registers, the Si2457/34/15/04 offers an unprecedented level of programmability for a controller-based modem. A detailed list of these registers and their use is beyond the scope of this data sheet. Refer to "AN93: ISOmodem® Chipset Family Designer's Guide" for details.



# 7. Pin Descriptions: Si2457/34/15/04 (16-Pin Option)



Pin #	Pin Name	Description
1	CLKIN/XTALI	XTALI—Crystal Oscillator Pin.  Provides support for parallel resonant AT cut crystals. A 4.9152 MHz or 32.768 kHz crystal or a 32.768 kHz or 4.9152 or 27 MHz clock on XTALI is required.
2	XTALO	XTALO—Crystal Oscillator Pin. Serves as the output of the crystal amplifier.
3	RI	Ring Indicator.  The RI on (active low) indicates the presence of an ON segment of a ring signal on the telephone line.
4	$V_D$	Supply Voltage. Provides the 3.3 V supply voltage to the Si2457/34/15/04.
5	MISO/RXD	Master In Slave Out/Receive Data. Serial data output from modem in SPI mode. Data output to DTE RXD pin in UART mode.
6	MOSI/TXD	Master Out Slave In/Transmit Data. Serial data input to modem in SPI mode. Data input from DTE TXD pin in UART mode.
7	SCLK/CTS	Serial Data Clock/Clear to Send. Signals that the Si2457/34/15/04 is ready to receive more digital data on the TXD pin. Serial data clock input in SPI mode.
8	RESET	Reset Input.  An active low input that is used to reset all control registers to a defined, initialized state.
9	C2A	Isolation Capacitor 2A. Connects to one side of the isolation capacitor C2.
10	C1A	Isolation Capacitor 1A. Connects to one side of the isolation capacitor C1.
11	ĪNT	Interrupt Output. Active low interrupt output.



# Si2457/34/15/04

Pin#	Pin Name	Description
12	GND	Ground. Connects to the system digital ground.
13	V <sub>A</sub>	Regulator Voltage Reference.  Connects to an external capacitor and serves as the reference for the internal voltage regulator.
14	ESC	Escape. A positive edge on this pin causes the modem to go from online (connected) mode to the offline (command) mode.
15	DCD	Carrier Detect. Active low carrier detect.
16	SS/RTS	SPI Slave Select/Request to Send. Active low slave select in SPI mode. Active low request to send input used for flow control in UART mode.



# 8. Pin Descriptions: Si2457/34/15/04 (24-Pin Option)

Si2457/34/15/04 (24-Pin Option) CLKIN/XTALI ☐ 1 • 24 SDO/EECLK/D5 XTALO ☐ 2 23 DCD/D4 22 ESC/D3 CLKOUT/EECS/A0 ☐ 3 FSYNC/D6 4 21 VD3.3 VD3.3 ☐ 5 20 GND 19 VDB GND ☐ 6 VDA ☐ 7 18 SDI/EESD/D2 SS/RTS/D7 8 17 RI/D1 16 INT/DO MISO/RXD/RD 9 15 AOUT/INT MOSI/TXD/WR ☐ 10 14 C1A SCLK/CTS/CS ☐ 11 13 C2A RESET ☐ 12

Pin#	Pin Name	Description
1	CLKIN/XTALI	Clock Input/Crystal Oscillator Pin.  Provides support for parallel resonant AT cut crystals. A 4.9152 MHz or 32.768 kHz crystal or a 32.768 kHz or 4.9152 or 27 MHz clock on XTALI is required.
2	XTALO	Crystal Oscillator Pin. Serves as the output of the crystal amplifier.
3	CLKOUT/EECS/ A0	Clock Output/EEPROM Chip Select/Address Bit 0. Clock output in serial mode. Active low read/write enable for SPI EEPROM in serial mode when pin 4 is pulled low during powerup. Address Enable in parallel mode.
4	FSYNC/D6	Frame Sync/Data Bit. Frame Sync output to codec in serial mode. Bidirectional parallel bus data bit 6 in parallel mode.
5, 21	VD3.3	Digital Supply Voltage.  Provides the 3.3 V supply voltage to the Si2457/34/15/04.
6, 20	GND	Ground. Connects to the system digital ground.
7,19	VDA, VDB	Regulator Voltage Reference.  Connects to an external capacitor and serves as the reference for the internal voltage regulator.
8	SS/RTS/D7	SPI Slave Select/Request to Send/Data Bit.  Active low slave select in SPI mode.  Active low request to send input used for flow control in UART mode. Bidirectional parallel bus data bit 7 in parallel mode.



Pin#	Pin Name	Description
9	MISO/RXD/RD	Master In Slave Out/Receive Data/Read Enable. Serial data output from modem in SPI mode. Data output to DTE RXD pin in UART mode. Active low read enable pin in parallel mode.
10	MOSI/TXD/WR	Master Out Slave In/Transmit Data/Write Enable. Serial data input to modem in SPI mode. Data input from DTE TXD pin in serial mode. Active low write enable pin in parallel mode.
11	SCLK/CTS/CS	Serial Data Clock/Clear to Send/Chip Select. Serial data clock input in SPI mode. Signals that the Si2457/34/15/04 is ready to receive more digital data on the TXD pin in data mode. Active low chip select in parallel mode.
12	RESET	Reset Input.  An active low input that is used to reset all control registers to a defined initialized state.
13	C2A	Isolation Capacitor 2A. Connects to one side of the isolation capacitor, C2.
14	C1A	Isolation Capacitor 1A. Connects to one side of the isolation capacitor, C1.
15	AOUT/INT	Analog Output/Interrupt Output.  Analog output in serial mode. Active low interrupt output in parallel mode.
16	ĪNT/D0	Interrupt Output/Data Bit. Active low interrupt output in serial mode. Bidirectional parallel bus data bit 0 in parallel mode.
17	RI/D1	Ring Indicator/Data Bit.  The RI on (active low) indicates the presence of an ON segment of a ring signal on the telephone line. Bidirectional parallel bus data bit 1 in parallel mode.
18	SDI/EESD/D2	Serial Data In/EEPROM Serial Data Input/Output/Data Bit.  Serial Data In (to codec) output in serial mode. Bidirectional Input/Output to SPI EEPROM in serial mode when pin 4 is pulled low during power up. Bidirectional parallel bus data bit 2 in parallel mode.
22	ESC/D3	Escape/Data Bit. Hardware escape in serial mode. Bidirectional parallel bus data bit 3 in parallel mode.
23	DCD/D4	Carrier Detect/Data Bit. Active low carrier detect in serial mode. Bidirectional parallel bus data bit 4 in parallel mode.
24	SDO/EECLK/D5	Serial Data Out/EEPROM Clock/Data Bit 5. Serial Data Out (from codec) input in serial mode. Clock output for SPI EEPROM in serial mode when pin 4 is pulled low during power up. Bidirectional parallel bus data bit 5 in parallel mode.



# 9. Pin Descriptions: Si3018/10

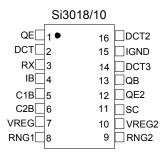


Table 14. Si3018/10 Pin Descriptions

1 QE Transistor Emitter. Connects to the emitter of Q3. 2 DCT DC Termination. Provides dc termination to the telephone network.  Receive Input. Serves as the receive side input from the telephone network.  Internal Bias. Provides a bias voltage to the device.  Isolation Capacitor 1B. Connects to one side of isolation capacitor C1 and communicates with the system side.  Connects to one side of isolation capacitor C2 and communicates with the system side.  VREG Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.  Ring 1. Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connects to the base of transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  Transistor Emitter 2. Connects to the base of transistor Q4.  DC Termination 3. Provides de termination to the telephone network.  Isolated Ground. Connects to ground on the line-side interface.  DC Termination 12.  DC Termination 12.  Provides (termination to the telephone network	Pin#	Pin Name	Description
DCT   DC Termination.   Provides do termination to the telephone network.	1	QE	Transistor Emitter.
Provides dc termination to the telephone network.  Receive Input. Serves as the receive side input from the telephone network.  Internal Bias. Provides a bias voltage to the device.  Isolation Capacitor 1B. Connects to one side of isolation capacitor C1 and communicates with the system side.  VREG Isolation Capacitor 2B. Connects to one side of isolation capacitor C2 and communicates with the system side.  VREG Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.  Ring 1. Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  Transistor Emitter 2. Connects to the emitter of Q4.  QB Transistor Base. Connects to the base of transistor Q4.  DCT3 DC Termination 3. Provides the dc termination to the telephone network.  Isolated Ground. Connects to ground on the line-side interface.			Connects to the emitter of Q3.
RX Receive Input. Serves as the receive side input from the telephone network.  IB Internal Bias. Provides a bias voltage to the device.  SCIB Isolation Capacitor 1B. Connects to one side of isolation capacitor C1 and communicates with the system side.  Connects to one side of isolation capacitor C2 and communicates with the system side.  VREG Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.  RING1 Ring 1. Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  RING2 Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  Transistor Emitter 2. Connects to the emitter of Q4.  Transistor Base. Connects to the emitter of Q4.  DCT3 DC Termination 3. Provides the dc termination to the telephone network.  IGND Isolated Ground. Connects to ground on the line-side interface.	2	DCT	DC Termination.
Serves as the receive side input from the telephone network.    IB			Provides dc termination to the telephone network.
Internal Bias.   Provides a bias voltage to the device.	3	RX	Receive Input.
Provides a bias voltage to the device.    Provides   Solation Capacitor 1B.			Serves as the receive side input from the telephone network.
Solation Capacitor 1B.   Connects to one side of isolation capacitor C1 and communicates with the system side.	4	IB	Internal Bias.
Connects to one side of isolation capacitor C1 and communicates with the system side.    Connects to one side of isolation capacitor C2 and communicates with the system side.   Connects to one side of isolation capacitor C2 and communicates with the system side.   VREG			Provides a bias voltage to the device.
C2B	5	C1B	Isolation Capacitor 1B.
Connects to one side of isolation capacitor C2 and communicates with the system side.  7 VREG Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal power supply.  8 RNG1 Ring 1. Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  9 RNG2 Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			Connects to one side of isolation capacitor C1 and communicates with the system side.
<ul> <li>VREG Voltage Regulator.         Connects to an external capacitor to provide bypassing for an internal power supply.</li> <li>RNG1 Ring 1.         Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.</li> <li>RNG2 Ring 2.         Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.</li> <li>VREG2 Voltage Regulator 2.         Connects to an external capacitor to provide bypassing for an internal power supply.</li> <li>SC SC Connection.         Enables external transistor network. Should be tied through a 0 Ω resistor to I<sub>GND</sub>.</li> <li>QE2 Transistor Emitter 2.         Connects to the emitter of Q4.</li> <li>QB Transistor Base.         Connects to the base of transistor Q4.</li> <li>DCT3 DC Termination 3.         Provides the dc termination to the telephone network.</li> <li>IGND Isolated Ground.         Connects to ground on the line-side interface.</li> <li>DC Termination 2.</li> </ul>	6	C2B	Isolation Capacitor 2B.
Connects to an external capacitor to provide bypassing for an internal power supply.  Ring 1. Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  Transistor Emitter 2. Connects to the emitter of Q4.  QB Transistor Base. Connects to the base of transistor Q4.  DCT3 DC Termination 3. Provides the dc termination to the telephone network.  ISOND Isolated Ground. Connects to ground on the line-side interface.  DC Termination 2.			Connects to one side of isolation capacitor C2 and communicates with the system side.
8 RNG1 Ring 1. Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  9 RNG2 Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	7	VREG	Voltage Regulator.
Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  9 RNG2 Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			, , , , , , , , , , , , , , , , , , , ,
caller ID signals to the Si2457/34/15/04.  9 RNG2 Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	8	RNG1	
9 RNG2 Ring 2. Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			· ·
Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			
caller ID signals to the Si2457/34/15/04.  10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	9	RNG2	
10 VREG2 Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.  11 SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			
Connects to an external capacitor to provide bypassing for an internal power supply.  SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  Transistor Emitter 2. Connects to the emitter of Q4.  Replace Transistor Base. Connects to the base of transistor Q4.  DCT3 DC Termination 3. Provides the dc termination to the telephone network.  IGND Isolated Ground. Connects to ground on the line-side interface.  DCT2 DC Termination 2.	10	VDEC2	
SC SC Connection. Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	10	VREGZ	
Enables external transistor network. Should be tied through a 0 Ω resistor to I <sub>GND</sub> .  12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	11	SC	
12 QE2 Transistor Emitter 2. Connects to the emitter of Q4.  13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	• • •	00	
13 QB Transistor Base. Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	12	QE2	
Connects to the base of transistor Q4.  14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			Connects to the emitter of Q4.
14 DCT3 DC Termination 3. Provides the dc termination to the telephone network.  15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.	13	QB	Transistor Base.
Provides the dc termination to the telephone network.  IGND Isolated Ground. Connects to ground on the line-side interface.  DCT2 DC Termination 2.			Connects to the base of transistor Q4.
Provides the dc termination to the telephone network.  IGND Isolated Ground. Connects to ground on the line-side interface.  DCT2 DC Termination 2.	14	DCT3	DC Termination 3.
15 IGND Isolated Ground. Connects to ground on the line-side interface.  16 DCT2 DC Termination 2.			
16 DCT2 DC Termination 2.	15	IGND	
16 DCT2 DC Termination 2.			Connects to ground on the line-side interface.
Provides do termination to the telephone network	16	DCT2	
i formes de termination to the telephone network.			Provides dc termination to the telephone network.



# 10. Ordering Guide

Chipset	Max Speed	System-Side Package	System-Side*	Line-Side*	Temp Range
Si2457	56 kbps	24-pin TSSOP	Si2457-D-FT	Si3018-F-FS	0 to 70 °C
Si2457	56 kbps	16-pin SOIC	Si2457-D-FS	Si3018-F-FS	0 to 70 °C
Si2434	33.6 kbps	24-pin TSSOP	Si2434-D-FT	Si3018-F-FS	0 to 70 °C
Si2434	33.6 kbps	16-pin SOIC	Si2434-D-FS	Si3018-F-FS	0 to 70 °C
Si2415	14.4 kbps	24-pin TSSOP	Si2415-D-FT	Si3018-F-FS	0 to 70 °C
Si2415	14.4 kbps	16-pin SOIC	Si2415-D-FS	Si3018-F-FS	0 to 70 °C
Si2404	2400 bps	24-pin TSSOP	Si2404-D-FT	Si3010-F-FS	0 to 70 °C
Si2404	2400 bps	16-pin SOIC	Si2404-D-FS	Si3010-F-FS	0 to 70 °C
Si2457	56 kbps	24-pin TSSOP	Si2457-D-GT	Si3018-F-GS	–40 to +85 °C
Si2434	33.6 kbps	24-pin TSSOP	Si2434-D-GT	Si3018-F-GS	–40 to +85 °C
Si2415	14.4 kbps	24-pin TSSOP	Si2415-D-GT	Si3018-F-GS	–40 to +85 °C
Si2404	2400 bps	24-pin TSSOP	Si2404-D-GT	Si3018-F-GS	–40 to +85 °C

\*Note: Add an "R" at the end of the device to denote tape and reel option.



# 11. Package Markings (Top Markings)

Codes for the Si2457-D-FT, Si2457-D-FS, Si2434-D-FT, Si2434-D-FS, Si2415-D-FS, Si2415-D-FS, Si2404-D-FT, Si2404-D-FS, Si3018-F-FS, and Si3010-F-FS top marks are as follows:

- YY = Current Year
- WW = Work Week
- R = Die Revision
- TTTTT = Trace Code
- XX = Assembly Country Code

### 11.1. Si2457-D-FT Top Marking

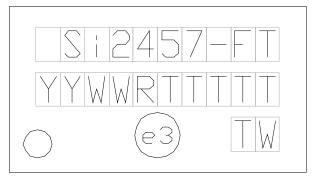


Figure 11. Si2457-D-FT Top Marking

# 11.2. Si2457-D-FS Top Marking



Figure 12. Si2457-D-FS Top Marking

### 11.3. Si2434-D-FT Top Marking

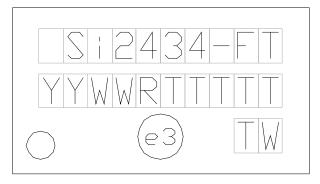


Figure 13. Si2434-D-FT Top Marking



# 11.4. Si2434-D-FS Top Marking



Figure 14. Si2434-D-FS Top Marking

# 11.5. Si2415-D-FT Top Marking

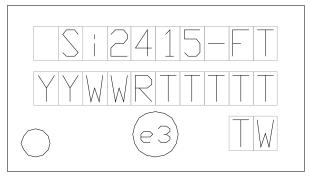


Figure 15. Si2415-D-FT Top Marking

### 11.6. Si2415-D-FS Top Marking



Figure 16. Si2415-D-FS Top Marking

### 11.7. Si2404-D-FT Top Marking

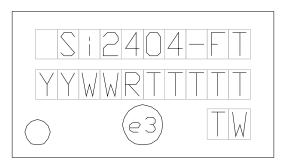


Figure 17. Si2404-D-FT Top Marking



# 11.8. Si2404-D-FS Top Marking



Figure 18. Si2404-D-FS Top Marking

# 11.9. Si3010-F-FS Top Marking



Figure 19. Si3010-F-FS Top Marking

# 11.10. Si3018-F-FS Top Marking



Figure 20. Si3018-F-FS Top Marking



# 12. Package Outline: 24-Pin TSSOP

Figure 21 illustrates the package details for the Si2457/34/15/04 24-pin packaging option. Table 15 lists the values for the dimensions shown in the illustration.

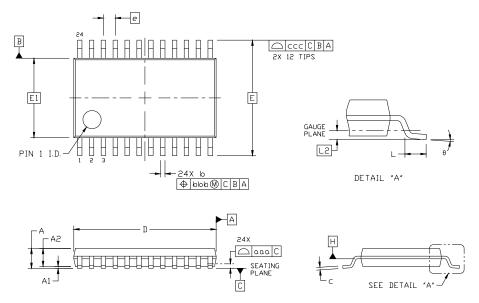


Figure 21. 24-Pin Thin Shrink Small Outline Package (TSSOP)

Table 15.	Package	Diagram	Dimensions

Dimension	Min	Nom	Max
Α	_	_	1.20
A1	0.05	_	0.15
A2	0.80	1.00	1.05
b	0.19	_	0.30
С	0.09	_	0.20
D	7.70	7.80	7.90
E		6.40 BSC	
E1	4.30	4.40	4.50
е	0.65 BSC		
L	0.45	0.60	0.75
L2	0.25 BSC		
θ	0°	_	8°
aaa	0.10		
bbb	0.10		
ccc	0.20		

#### Notes:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
- This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AD.
- **4.** Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



# 13. 24-Pin TSSOP Land Pattern

Figure 22 illustrates the recommended land pattern for the Si2457/34/15/04 24-Pin TSSOP. Table 16 lists the values for the dimensions shown in the illustration.

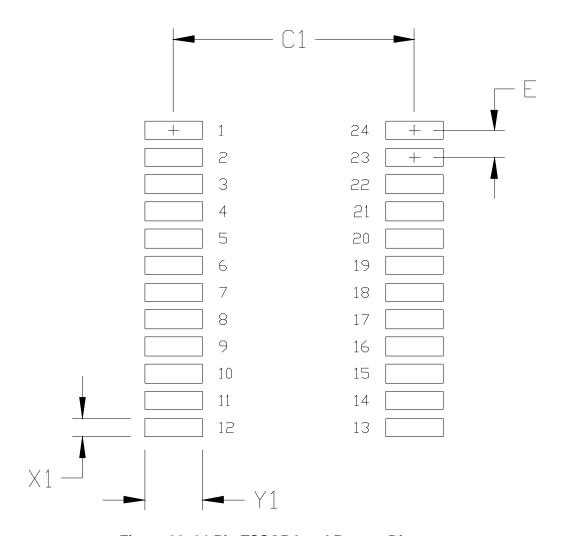


Figure 22. 24-Pin TSSOP Land Pattern Diagram

Table 16. 24-Pin TSSOP PCB Land Pattern

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.80
E	Pad Row Pitch	0.65
X1	Pad Width	0.45
Y1	Pad Length	1.40

#### Notes:

- This Land Pattern Design is based on IPC-7351 specifications for Density Level B (Median Land Protrusion).
- 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.



# 14. Package Outline: 16-Pin SOIC

Figure 23 illustrates the package details for the Si2457/34/15/04 16-pin packaging option. Table 17 lists the values for the dimensions shown in the illustration.

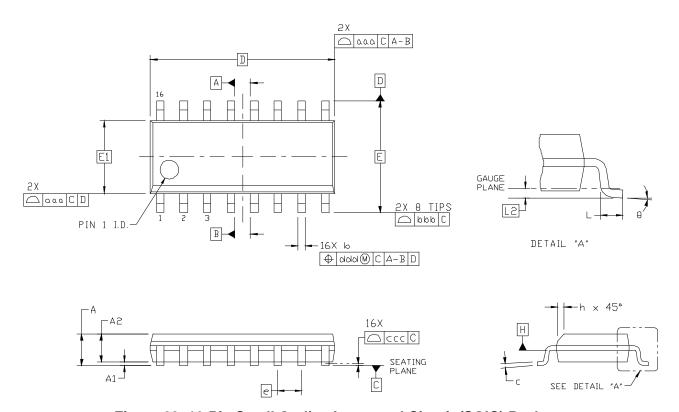


Figure 23. 16-Pin Small Outline Integrated Circuit (SOIC) Package



**Table 17. Package Diagram Dimensions** 

Dimension	Min	Max		
A	_	1.75		
A1	0.10	0.25		
A2	1.25	_		
b	0.31	0.51		
С	0.17	0.25		
D	9.90 [	9.90 BSC		
Е	6.00	6.00 BSC		
E1	3.90 I	3.90 BSC		
е	1.27 [	1.27 BSC		
L	0.40	1.27		
L2	0.25 [	0.25 BSC		
h	0.25	0.50		
θ	0°	8°		
aaa	0.10			
bbb	0.20			
ccc	0.10			
ddd	0.25			

#### lotes:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
- **3.** This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
- **4.** Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



#### 15. 16-Pin SOIC Land Pattern

Figure 24 illustrates the recommended land pattern for the Si2457/34/15/04 16-Pin SOIC. Table 18 lists the values for the dimensions shown in the illustration.

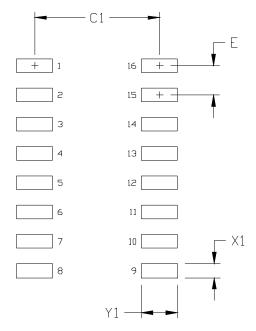


Figure 24. 16-Pin SOIC Land Pattern Diagram

Table 18, 16-Pin SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

### Notes:

#### General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.
- **4.** All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

#### Stencil Design

- **6.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 7. The stencil thickness should be 0.125 mm (5 mils).
- **8.** The ratio of stencil aperture to land pad size should be 1:1.

#### **Card Assembly**

- 9. A No-Clean, Type-3 solder paste is recommended.
- 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



### **DOCUMENT CHANGE LIST**

#### **Revision 0.91 to Revision 1.0**

- Added Figure 5 typical schematic with 16-pin system-side option.
- Updated Table 3 to include 16-pin system-side parameters.
- Updated default register setting in Table 16.
- Added Si2404 information.
- Added 16-pin system-side option.
- Updated "4. Functional Description" on page 17.
- Added "7. Pin Descriptions: Si2457/34/15/04 (16-Pin Option)" on page 45.
- Updated "10. Ordering Guide" on page 50 to reflect part revision.

#### Revision 1.0 to Revision 1.1

Added industrial temperature range devices.

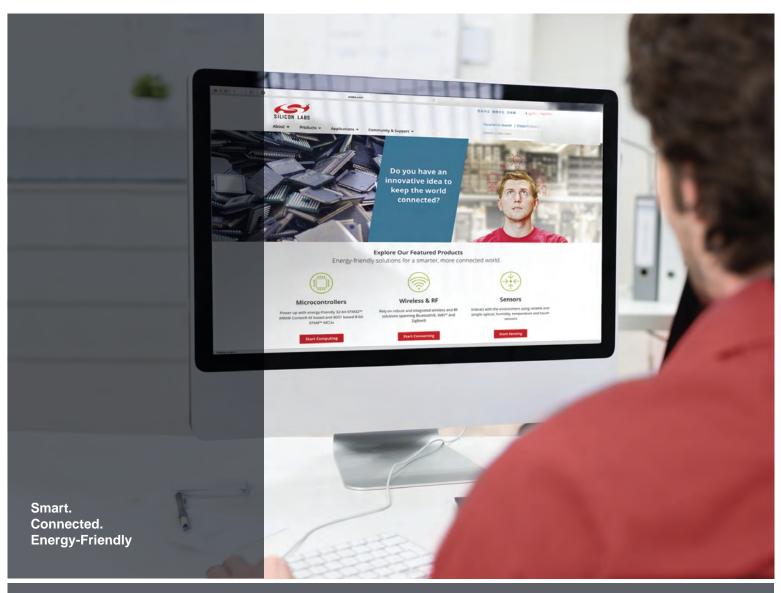
#### **Revision 1.1 to Revision 1.2**

- Added Revision D additions and changes:
  - 32.768 kHz oscillator option
  - SPI interface
- Moved U-Register details to AN93.
- Added package markings.

#### **Revision 1.2 to Revision 1.3**

- Removed 5 V interface logic support.
- Lowered digital input voltage V<sub>IND</sub> max from 5.3 V to (V<sub>D</sub> + 0.3) V.
- Lowered total supply current (typ) from 26 to 17 mA.
- Added total supply current, wake-on-ring specification.











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