LM3203 Step-Down DC-DC Converter with Bypass Mode for CDMA / WCDMA RF Power Amplifiers

Check for Samples: LM3203

FEATURES

- **2MHz (Typ.) PWM Switching Frequency**
- **Operates from a Single Li-Ion Cell (2.7V to 5.5V)**
- **Adjustable Output Voltage (0.8V to 3.6V)**
- **500mA Maximum Load Capability (PWM and Bypass Mode)**
- **PWM / Forced Bypass Mode**
- **Low R_{DSON} Bypass FET: 85mΩ (Typ.)**
- **High Efficiency (96% typ. at 3.6V_{IN}, 3.2V_{OUT} at 150mA)**
- **Fast Turn-On Time When Enabled (50µs typ.), 3GPP Compliant**
- **10-Pin DSBGA Package**
- **Current Overload Protection**
- **Thermal Overload Protection**

APPLICATIONS

- **Cellular Phones**
- **Hand-Held Radios**
- **RF PC Cards**
- **Battery Powered RF Devices**

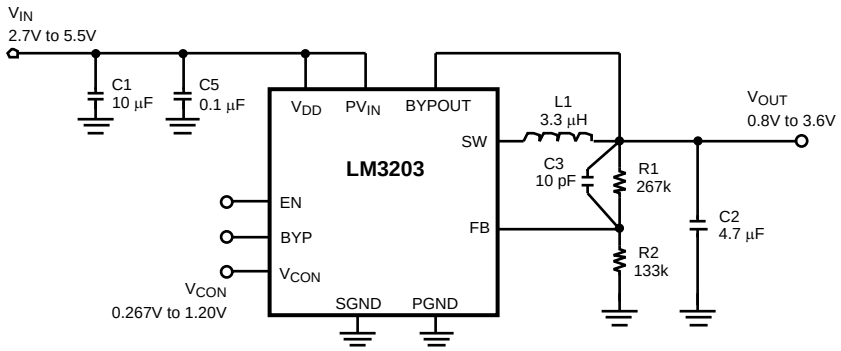
DESCRIPTION

The LM3203 is a DC-DC converter optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell. However, they may be used in many other applications. It steps down an input voltage of 2.7V to 5.5V to an adjustable output voltage of 0.8V to 3.6V. The output voltage is set using a V_{CON} analog input and external resistor dividers for optimizing efficiency of the RF PA at various power levels.

The LM3203 offers 3 modes for mobile phones and similar RF PA applications. Fixed-frequency PWM mode minimizes RF interference. Bypass mode turns on an internal bypass switch to power the PA directly from the battery. Shutdown mode turns the device off and reduces battery consumption to 0.1µA (typ.).

The LM3203 is available in a 10-pin lead free DSBGA package. A high switching frequency (2MHz) allows use of tiny surface-mount components.

TYPICAL APPLICATION



CONNECTION DIAGRAMS

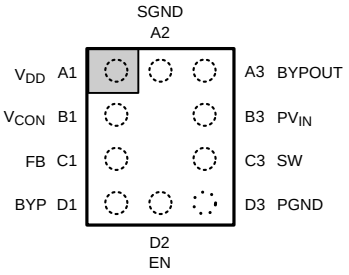


Figure 1. Top View

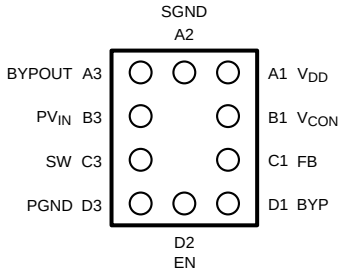


Figure 2. Bottom View

10–Bump Thin DSBGA Package, Large Bump.

See NS Package Number YPA0010NHA.

PIN DESCRIPTION

Pin #	Name	Description
A1	V_{DD}	Analog Supply Input. A 0.1 µF ceramic capacitor is recommended to be placed as close to this pin as possible. (Figure 31)
B1	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode. (Refer to Setting the Output Voltage) Do not leave floating.
C1	FB	Feedback Analog Input. Connect to the external resistor divider. (Figure 31)
D1	BYP	Bypass. Use this digital input to command operation in Bypass mode. Set BYP low for PWM operation.
D2	EN	Enable Input. Set this digital input high after Vin >2.7V for normal operation. For shutdown, set low.
D3	PGND	Power Ground
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3203.
B3	PV_{IN}	Power Supply Voltage Input to the internal PFET switch and Bypass FET. (Figure 31)
A3	BYPOUT	Bypass FET Drain. Connect to the output capacitor. (Figure 31) Connect this pin to V_{DD} when Bypass mode is NOT required. Do not leave floating.
A2	SGND	Analog and Control Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

V_{DD}, PV_{IN} to SGND		−0.2V to +6.0V
PGND to SGND		−0.2V to +0.2V
EN, FB, BYP, V_{CON}		(SGND −0.2V) to (V_{DD} +0.2V) w/6.0V max
SW, BYPOUT		(PGND −0.2V) to (PV_{IN} +0.2V) w/6.0V max
PV_{IN} to V_{DD}		−0.2V to +0.2V
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)		+260°C
ESD Rating(5)	Human Body Model	2.0 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(5) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7) . TI recommends that all integrated circuits be handled with appropriate precautions.

OPERATING RATINGS(1)(2)

Input Voltage Range		2.7V to 5.5V
Recommended Load Current	PWM Mode	0mA to 500mA
	Bypass Mode	0mA to 500mA
Junction Temperature (T_J) Range		−30°C to +125°C
Ambient Temperature (T_A) Range(3)		−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal	100°C/W
Resistance (θ_{JA}), YPA10 Package(1)	

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-2. A 1" x 1", 4 layer, 1.5oz. Cu board was used for the measurements.

ELECTRICAL CHARACTERISTICS[1][2]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, specifications apply to the LM3203 with: $PV_{IN} = V_{DD} = EN = 3.6V$, $BYP = 0V$, $V_{CON} = 0.267V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range[3]	$PV_{IN} = V_{DD} = V_{IN}$	2.7		5.5	V
$V_{FB,\ MIN}$	Feedback Voltage at Minimum Setting	$V_{CON} = 0.267V$, $V_{IN} = 3.6V$	**0.250**	0.267	**0.284**	V
$V_{FB,\ MAX}$	Feedback Voltage at Maximum Setting	$V_{CON} = 1.20V$, $V_{IN} = 4.2V$	**1.176**	1.200	**1.224**	V
OVP	Over-Voltage Protection Threshold	See[4]		100	150	mV
I_{SHDN}	Shutdown Supply Current[5]	$EN = SW = BYPOUT = V_{CON} = FB = 0V$		0.1	**3**	µA
I_{Q_PWM}	DC Bias Current into V_{DD}	$V_{CON} = 0.267V$, $FB = 2V$, $BYPOUT = 0V$, No Switching		675	**780**	µA
I_{Q_BYP}		$BYP = 3.6V$, $V_{CON} = 0.5V$, No Load		680	**780**	µA
$R_{DSON\ (P)}$	Pin-Pin Resistance for P-FET	$I_{SW} = 500mA$		320	**450**	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for N-FET	$I_{SW} = -200mA$		310	**450**	mΩ
$R_{DSON\ (BYP)}$	Pin-Pin Resistance for Bypass FET	$I_{BYPOUT} = 500mA$		85	**120**	mΩ
$I_{LIM\text{-}PFET}$	Switch Current Limit	See[6]	**700**	820	**940**	mA
$I_{LIM\text{-}BYP}$	Bypass FET Current Limit	See[7]	**800**	1000	**1200**	mA
F_{OSC}	Internal Oscillator Frequency		**1.7**	2	**2.2**	MHz
V_{IH}	Logic High Input Threshold for EN, BYP		**1.20**			V
V_{IL}	Logic Low Input Threshold for EN, BYP				**0.4**	V
I_{PIN}	Pin Pull Down Current for EN, BYP	EN, BYP = 3.6V		5	**10**	µA
Gain	V_{CON} to V_{OUT} Gain			1		V/V
Z_{CON}	V_{CON} Input Resistance	$V_{CON} = 1.2V$		1		MΩ

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The LM3203 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(4) Over-Voltage protection (OVP) threshold is the voltage above the nominal V_{OUT} where the OVP comparator turns off the PFET switch while in PWM mode. The OVP threshold will be the value of the threshold at the FB voltage times the resistor divider ratio. In the Figure 31, 100mV (typ.) × ((267K + 133K) ÷ 133K).
(5) Shutdown current includes leakage current of PFET and Bypass FET.
(6) Electrical Characteristics table reflects open loop data (FB=0V and current drawn from SW pin ramped up until cycle by cycle current limit is activated). Refer to Typical Performance Characteristics (Open/Closed Loop Current Limit vs Temperature (PWM Mode) curve) for closed loop data and its variation with regards to supply voltage and temperature. Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.
(7) Bypass FET current limit is defined as the load current at which the FB voltage is 1V lower than V_{IN}.

SYSTEM CHARACTERISTICS

The following spec table entries are specified by design over ambient temperature range if the component values in the typical application circuit are used. **These parameters are not specified by production testing.**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{STARTUP}$	Time for V_{OUT} to rise to 3.4V in PWM mode	V_{IN} = 4.2V, C_{OUT} = 4.7µF, R_{LOAD} = 10Ω L = 3.3uH (I_{SAT} > 0.94A) EN = Low to High		50		µs
$T_{RESPONSE}$	Time for V_{OUT} to Rise from 0.8V to 3.6V in PWM Mode	V_{IN} = 4.2V, C_{OUT} = 4.7µF, R_{LOAD} = 10Ω L = 3.3uH (I_{SAT} > 0.94A)		30		µs
C_{CON}	V_{CON} Input Capacitance	V_{CON} = 1V, Test frequency = 100kHz			15	pF
T_{ON_BYP}	Bypass FET Turn On Time In Bypass Mode	V_{IN} = 3.6V, V_{CON} = 0.267V, C_{OUT} = 4.7µF, R_{LOAD} = 10Ω BYP = Low to High			30	µs

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit in Figure 31, $PV_{IN} = V_{DD} = EN = 3.6V$, $BYP = 0V$, $T_A = 25°C$, unless otherwise noted)

Quiescent Current vs Supply Voltage (V_{CON} = 0.267V, FB = 2V, No Load)

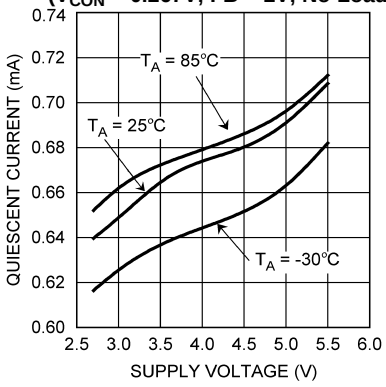


Figure 3.

Shutdown Current vs Temperature (EN = 0V)

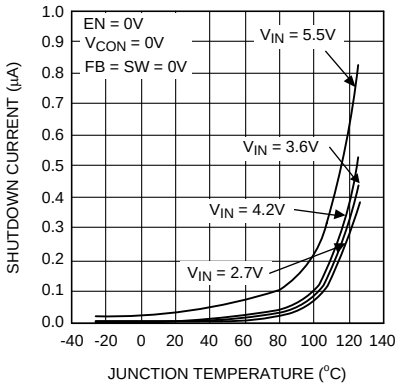


Figure 4.

Switching Frequency Variation vs Temperature (V_{OUT} = 1.5V, I_{OUT} = 200 mA)

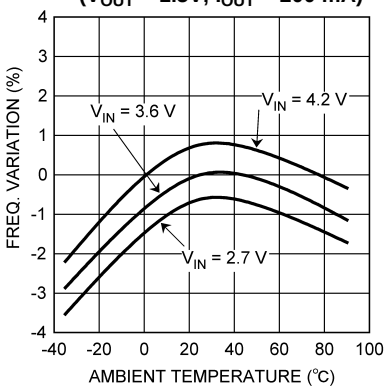


Figure 5.

Output Voltage vs Supply Voltage (V_{OUT} = 1.5V, V_{CON} = 0.5V)

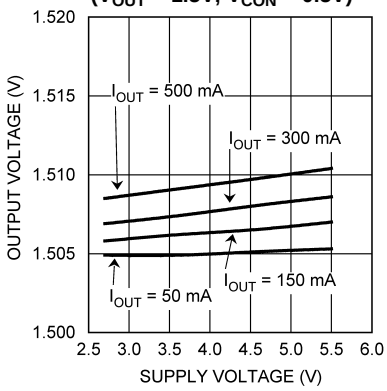


Figure 6.

Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 1.5V, V_{CON} = 0.5V)

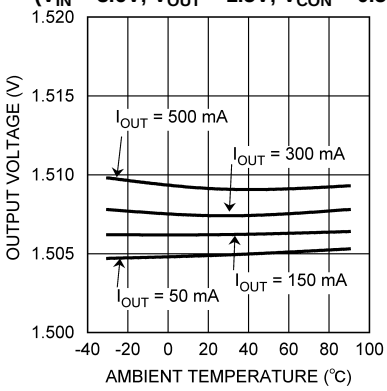


Figure 7.

Output Voltage vs Temperature (V_{IN} = 4.2V, V_{OUT} = 3.4V, V_{CON} = 1.13V)

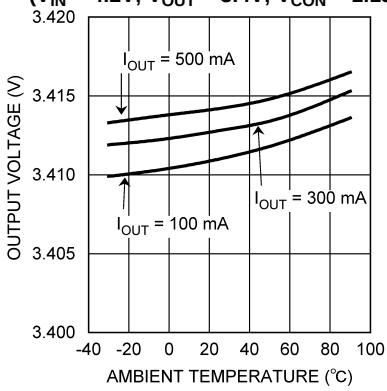


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, PV_{IN} = V_{DD} = EN = 3.6V, BYP = 0V, T_A = 25°C, unless otherwise noted)

Open/Closed Loop Current Limit vs Temperature (PWM Mode)

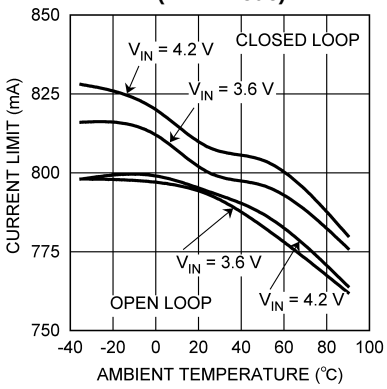


Figure 9.

Output Voltage vs Output Current (BYP Mode, V_{IN} = BYP = 3.6V)

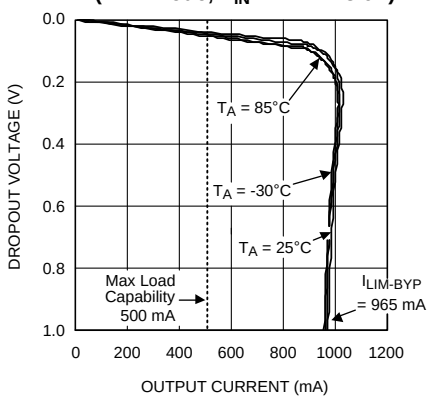


Figure 10.

Low V_{CON} Voltage vs Output Voltage (R_{LOAD} = 15Ω)

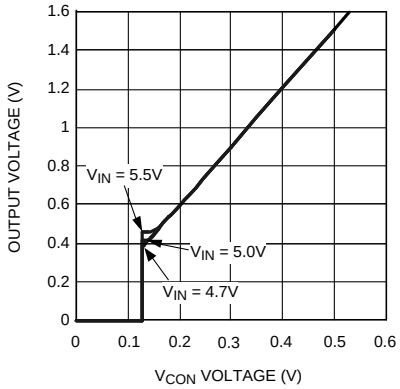


Figure 11.

Efficiency vs Output Voltage (V_{IN} = 3.9V)

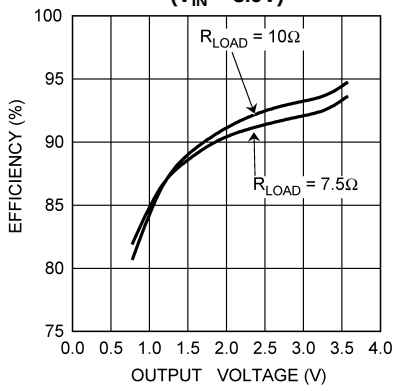


Figure 12.

Efficiency vs Output Current (V_{OUT} = 1.5V, V_{CON} = 0.5V)

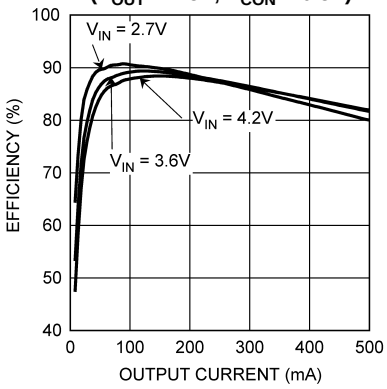


Figure 13.

Efficiency vs Output Current (V_{OUT} = 3.25V, V_{CON} = 1.08V)

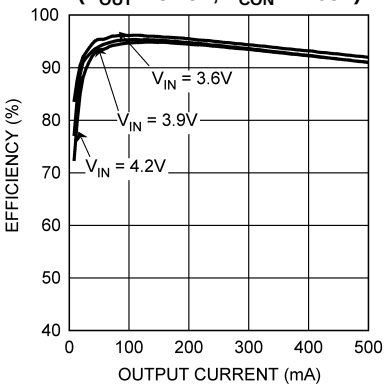


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, $PV_{IN} = V_{DD} = EN = 3.6V$, BYP = 0V, $T_A = 25°C$, unless otherwise noted)

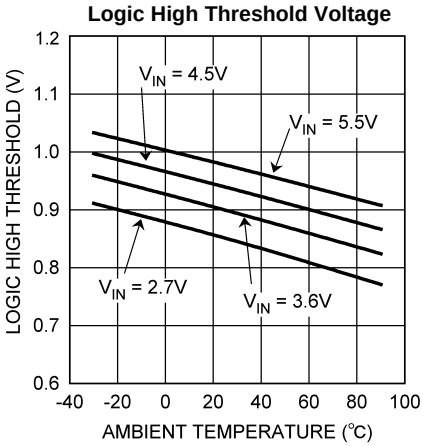


Figure 15.

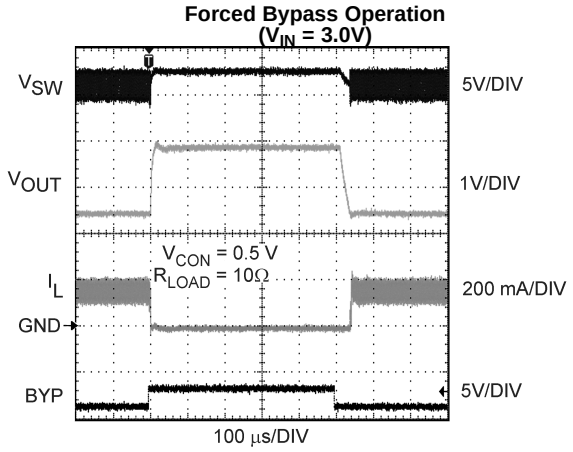


Figure 16.

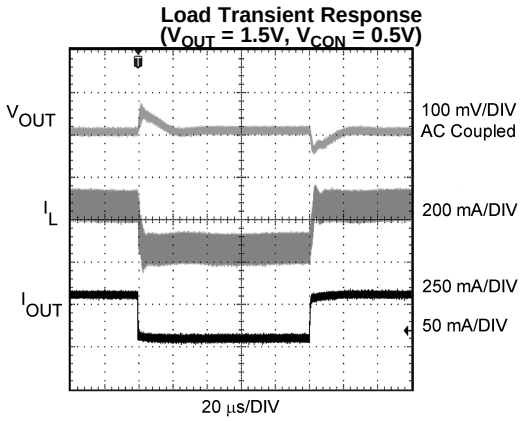


Figure 17.

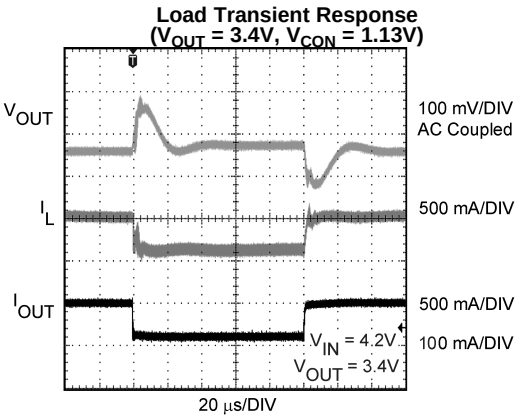


Figure 18.

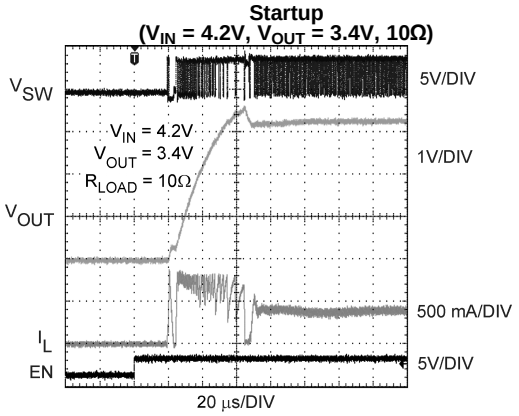


Figure 19.

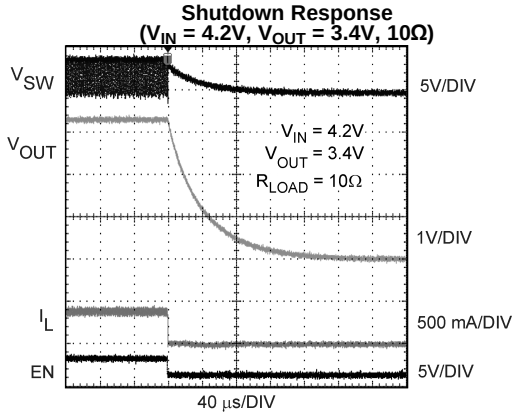


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, $PV_{IN} = V_{DD} = EN = 3.6V$, BYP = 0V, $T_A = 25°C$, unless otherwise noted)

Line Transient Response
(V_{IN} = 3.0V to 3.6V)

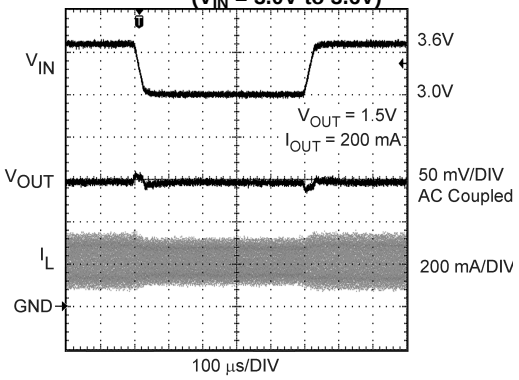


Figure 21.

V_{CON} Voltage Response
(V_{IN} = 4.2V, V_{CON} = 0.5V/1.13V)

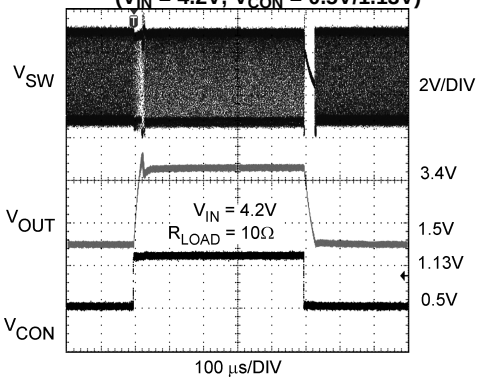


Figure 22.

Timed Current Limit Response
(normal operation to short circuit)

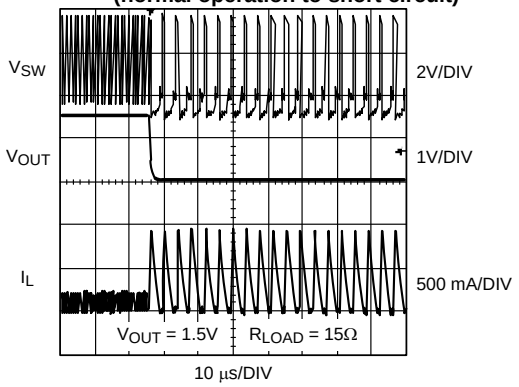


Figure 23.

Output Voltage Ripple
(V_{OUT} = 1.5V, V_{CON} = 0.5V)

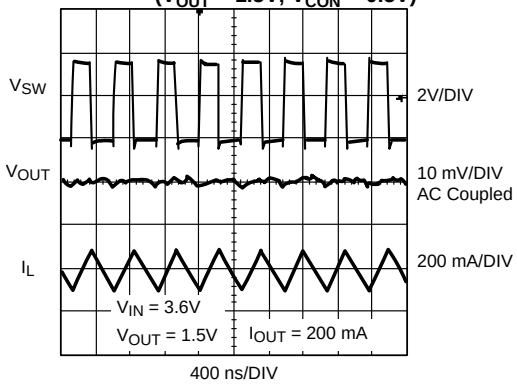


Figure 24.

Output Voltage Ripple
(V_{OUT} = 3.25V, V_{CON} = 1.08V)

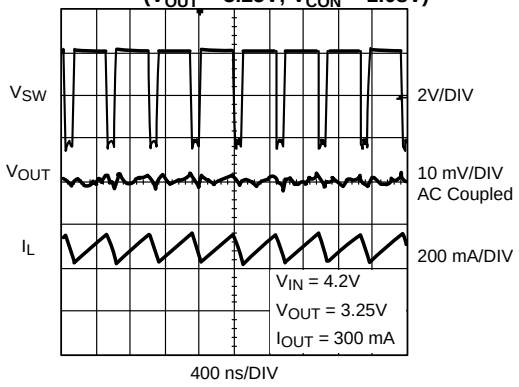


Figure 25.

Output Voltage Ripple in Dropout
(V_{IN} = 3.57V, V_{OUT} = 3.25V, I_{LOAD} = 200 mA)

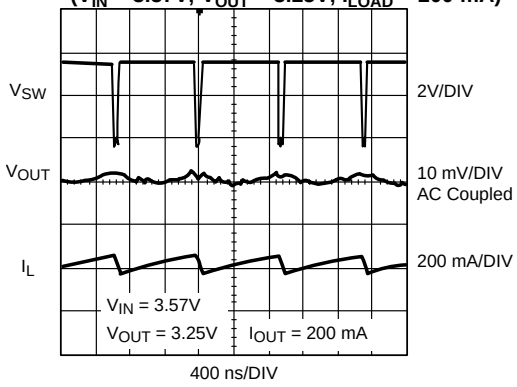


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit in Figure 31, $PV_{IN} = V_{DD} = EN = 3.6V$, BYP = 0V, $T_A = 25°C$, unless otherwise noted)

R_{DSON} vs Temperature (P-FET)

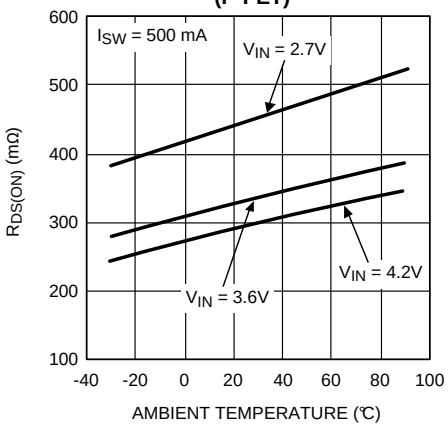


Figure 27.

R_{DSON} vs Temperature (N-FET)

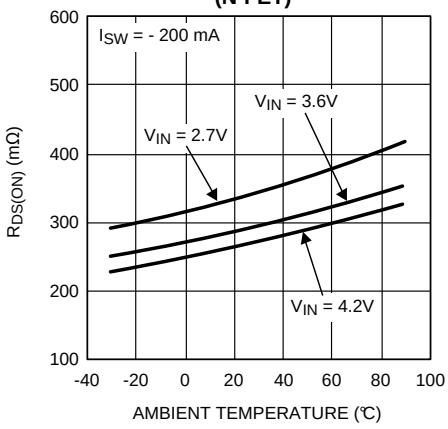


Figure 28.

R_{DSON} vs Temperature (Bypass FET)

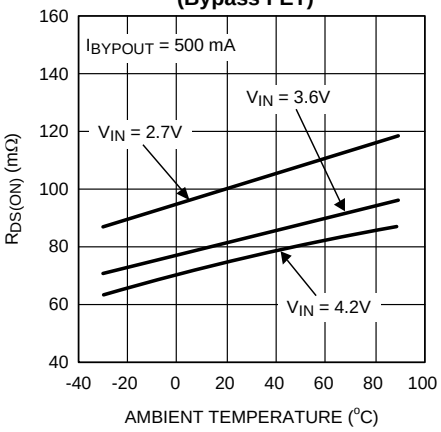


Figure 29.

Dropout Voltage vs Output Current (R_{DC} : Inductor DC Resistance)

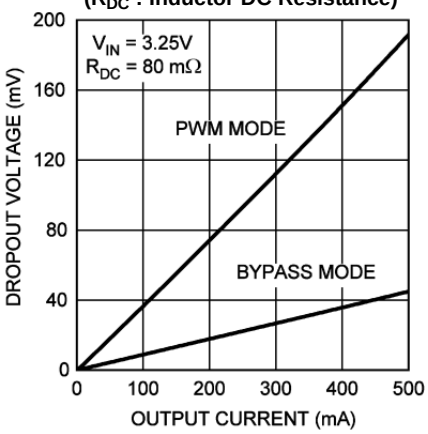
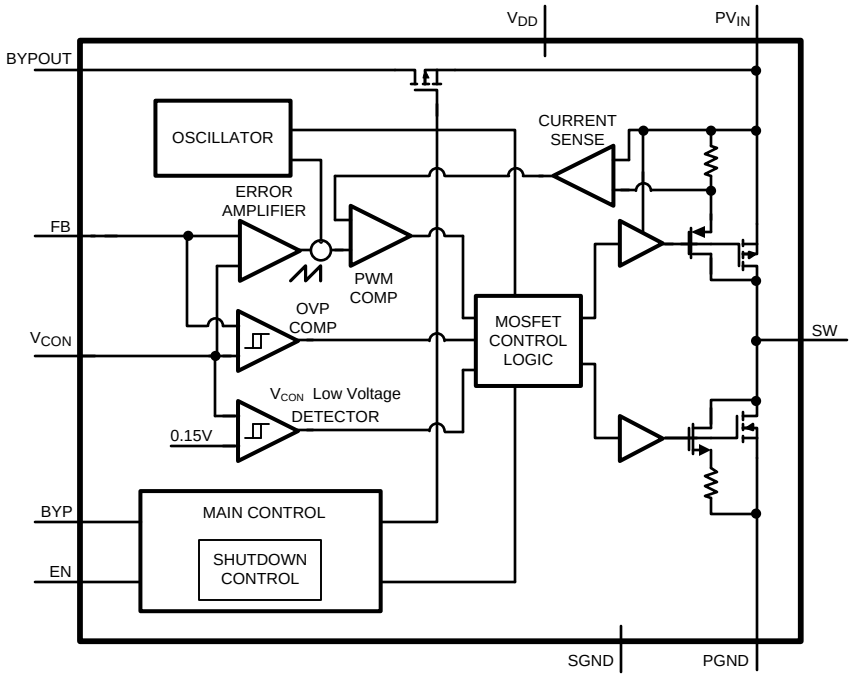


Figure 30.

BLOCK DIAGRAM



OPERATION DESCRIPTION

The LM3203 is a simple, step-down DC-DC converter with a bypass switch, optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on current-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 500mA. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

The device has all three of the pin-selectable operating modes required for powering RF PAs in mobile phones and other sophisticated portable device with complex power management needs. Fixed-frequency PWM operation offers regulated output at high efficiency while minimizing interference with sensitive IF and data acquisition circuits. Bypass mode turns on an internal FET bypass switch to power the PA directly from the battery. This helps the RF power amplifier maintain its operating power during low battery conditions by reducing the dropout voltage across the LM3203. Shutdown mode turns the device off and reduces battery consumption to 0.1µA (typ.).

DC PWM mode output voltage precision is +/-2% for $1.2V_{OUT}$. Efficiency is typically around 96% for a 150mA load with 3.2V output, 3.6V input. PWM mode quiescent current is 0.675 mA (typ.). The FB pin voltage is dynamically programmable from 0.267V to 1.2V by adjusting the voltage on the V_{CON}. External divider resistors can change the output voltge range. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection, over voltage protection and thermal shutdown.

The LM3203 is constructed using a chip-scale 10-pin DSBGA package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (2MHz typ.) reduces the size of external components. Use of a DSBGA package requires special design considerations for implementation. (See DSBGA Package Assembly and Use section.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions. (See Shutdown Mode section.)

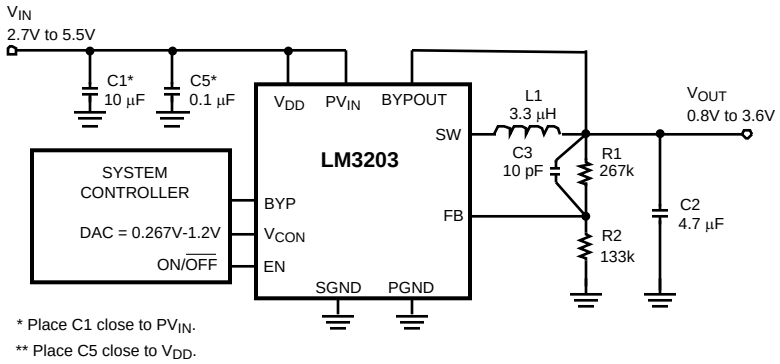


Figure 31. Typical Operating System Circuit where baseband controls the output voltage using a DAC

Circuit Operation

Referring to Figure 31, the LM3203 operates as follows. During the first part of each switching cycle, the control block in the LM3203 turns on the internal PFET (P-channel MOSFET) switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} - V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is going high, and releases it when inductor current is going low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM Mode

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the PFET drain current to a slope-compensated reference current generated by the error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load. The minimum on-time of PFET in PWM mode is 50ns (typ.).

Bypass Mode

The LM3203 contains an internal PFET switch for bypassing the PWM DC-DC converter during Bypass mode. In Bypass mode, this PFET is turned on to power the PA directly from the battery for maximum RF output power. Bypass mode is more efficient than operating in PWM mode at 100% duty cycle because the resistance of the bypass PFET is less than the series resistance of the PWM PFET and inductor. This translates into higher voltage available on the output in Bypass mode, for a given battery voltage. The part can be placed in bypass mode by sending BYP pin high. It remains in bypass mode until BYP pin goes low.

It is recommended to connect BYPOUT pin directly to the output capacitor with a separate trace and not to the FB pin. Connect the BYPOUT pin to the V_{DD} pin when Bypass mode is not required.

If V_{CON} is less than approx. 0.15V, the Bypass FET is turned off.

Operating Mode Selection Control

The LM3203 is designed for digital control of the operating modes using the BYP pin. Setting the BYP pin high (>1.2V) places the device in Bypass mode. Setting BYP pin low (<0.4V) forces operation in PWM mode.

Bypass and PWM operation overlap during the transition between the two modes. This transition time is approximately 31µs when changing from PWM to Bypass mode, and 15µs when changing from Bypass to PWM mode. This helps prevent under or overshoots during the transition period between PWM and Bypass modes.

Shutdown Mode

Setting the EN digital pin low (<0.4V) places the LM3203 in a 0.1µA (typ.) Shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3203 are turned off. Setting EN high (>1.2V) enables normal operation.

EN should be set low to turn off the LM3203 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3203 is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing and requirements for small package size outweigh the benefit of including UVLO (Under Voltage Lock-Out) circuitry.

Dynamically Adjustable Output Voltage

The LM3203 features dynamically adjustable output voltage. The output can be set by changing the voltage on the analog V_{CON} pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See Setting the Output Voltage section for further details.

Over Voltage Protection

The LM3203 has an over voltage comparator that prevents the output voltage from rising too high, when the device is left in PWM mode under light-load conditions, during output voltage steps, or during startup. When the FB pin voltage rises by 100mV over the V_{CON} voltage, the OVP comparator inhibits PWM operation to skip pulses until the feedback voltage returns to the V_{CON} voltage. During the over voltage protection mode, both the PWM PFET and the NFET synchronous rectifier are off. When the part comes out of the over-voltage protection mode, the NFET synchronous rectifier remains off for approximately 3.5µs to avoid inductor current going negative.

Internal Synchronous Rectification

While in PWM mode, the LM3203 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the internal NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. There is no zero cross detect, which means that the NFET can conduct current in both directions and inductor current is always continuous. The advantage of this method is that the part remains in PWM mode at light loads or no load conditions. The NFET has a current limit. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

Current Limiting

A current limit feature allows the LM3203 to protect itself and external components during overload conditions. In PWM mode, a 940mA (max.) cycle-by-cycle current limit is normally used. If an excessive load pulls the output voltage down to below approximately 0.375V, indicating a possible short to ground, then the device switches to a timed current limit mode. In timed current limit mode, the internal PFET switch is turned off after the current comparator trips, and the beginning of the next cycle is inhibited for 3.5µs to force the instantaneous inductor current to ramp down to a safe value. After the 3.5µs interval, the internal PFET is turned on again. This cycle is

repeated until the load is reduced and the output voltage exceeds approximately 0.375V. Therefore, the device may not startup if an excessive load is connected to the output when the device is enabled. The synchronous rectifier is off in the timed current limit mode. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions. This timed current limit function is disabled if the BYPOUT pin is connected to V_{DD}.

A current limit is also provided for the NFET. This is approximately −500mA. Both the NFET and the PFET are turned off in negative current limit until the PFET is turned on again at the beginning of the next cycle. The negative current limit inhibits buildup of excessive negative inductor current.

In the Bypass mode, the bypass current limit is 1000mA (typ.). The output voltage drops when the bypass current limit kicks in.

Thermal Overload Protection

The LM3203 has a thermal overload protection function to protect the device from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off in PWM mode, and the Bypass PFET is turned off in Bypass mode. When the temperature drops below 130°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device.

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The LM3203 features a pin-controlled variable feedback voltage. It can be programmed for an output voltage from 0.8V to 3.6V by setting the voltage on the V_{CON} pin, as in the formula below (Refer to Figure 31). In this scheme the output voltage is directly proportional to V_{CON}.

$$V_{OUT} = ((R1 + R2) / R2) \times V_{CON} \quad (1)$$

When V_{CON} is between 0.267V and 1.20V, the output voltage will follow the above equation. For example, the V_{OUT} is proportionally 3 times of V_{CON} when external resistor dividers are used as in Figure 31 .

If V_{OUT} is over 3.6V, sub-harmonic oscillation may occur because of insufficient slope compensation.

If the target voltage is less than 0.8V, the output voltage may not be regulated due to the required on-time being less than the minimum on-time (50ns). The output voltage can go lower than 0.8V providing a limited V_{IN} range is used. Refer to Typical Performance Characteristics (Low V_{CON} Voltage vs Output Voltage curve) for details. This curve is for a typical part and there could be part to part variation for output voltages less than 0.8V over the limited V_{IN} range. In addition, if the V_{CON} voltage is less than approx. 0.15V, the LM3203 output is off, but the internal bias circuits are still active.

INDUCTOR SELECTION

A 3.3µH inductor with saturation current rating over 940mA is recommended for almost all applications. The inductor resistance should be less than 0.3Ω for better efficiency. Table 1 lists suggested inductors and suppliers.

Table 1. Suggested Inductors and Suppliers

Model	Size (WxLxH) [mm]	Vendor
DO3314-332MX	3.3 x 3.3 x 1.4	Coilcraft
NR3015T3R3M	3.0 x 3.0 x 1.5	Taiyo- Yuden

A 2.2uH inductor can be used if maximum current in PWM mode is 300mA. For low-cost applications, an unshielded bobbin inductor can be used. For noise-critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to layout the board with footprints accommodating both types for design flexibility. This allows substitution of an unshielded inductor, in the event that noise from low-cost bobbin models is unacceptable. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field. This can cause poor efficiency, regulation errors or stress to a DC-DC converter like the LM3203.

CAPACITOR SELECTION

The LM3203 is designed to be used with ceramic capacitors. Use a 10µF ceramic capacitor for the input and a 4.7µF ceramic capacitor for the output. Ceramic capacitors such as X5R, X7R and B are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 2 lists suggested capacitors and suppliers.

Table 2. Suggested Capacitors and Suppliers(1)

Model	Size (EIA)	Vendor
LMK212BJ475MG	2012 (0805)	Taiyo-Yuden
C2012X5R0J475K	2012 (0805)	TDK
C3216X5R1A106K	3216 (1206)	TDK

(1) 4.7µF for C_{OUT} and 10µF for C_{IN}

The DC bias characteristics of the capacitor must be considered when selecting case sizes. If smaller case size such as 1608 (0603) is selected, the dc bias could reduce the cap value by as much as 40%, in addition to the 20% tolerances and 15% temperature coefficients. Request dc bias curves from manufacturer when making selection.The device has been designed to be stable with output capacitance as low as 3µF to account for capacitor tolerances.This value includes dc bias reduction, manufacturing tolerences and temp coefficients.

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3203 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. A 0.1µF capacitor is also recommended close to V_{DD} pin. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in TI Application Note 1112 (SNVA009). Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 (SNVA009) for specific instructions how to do this. The 10-Bump package used for the LM3203 has 300 micron solder balls and requires 10.82 mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6-7 mil wide, for a section approximately 6 mil long or longer, as a thermal relief. Then each trace should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3203 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps B3, C3 and D3. Because PGND and PV_{IN} are typically connected to large copper planes, inadequate thermal relief can result in inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metalization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

Do not use or power-up the LM3203 while subjecting it to high intensity red or infrared light; otherwise degraded, unpredictable or erratic operation may result. Examples of light sources with high red or infrared content include the sun and halogen lamps. Place the device in a case opaque to red or infrared light.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance. Good layout for the LM3203 can be implemented by following a few simple design rules.

1. Place the LM3203 on 10.82 mil pads. As a thermal relief, connect to each pad with a 7 mil wide, approximately 7 mil long traces, and when incrementally increase each trace to its optimal width. The important criterion is symmetry to ensure the solder bumps on the LM3203 re-flow evenly (see DSBGA Package Assembly and Use).
2. Place the LM3203, inductor and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor close to the LM3203. The input capacitor should be placed right next to the device between PV_{IN} and PGND pin.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3203 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3203 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction, prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the LM3203, and filter capacitors together using generous component side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3203 by giving it a low impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces, such as the voltage feedback trace, away from noisy traces and components. The voltage feedback trace must remain close to the LM3203 circuit and should be routed directly from FB pin to V_{OUT} at the output capacitor. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and the layer on which the feedback trace is routed. This reduces EMI radiation on to the DC-DC converter's own voltage feedback trace.
7. It is recommended to connect BYPOUT pin to V_{OUT} at the output capacitor using a separate trace, instead of connecting it directly to the FB pin for better noise immunity.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3203TL/NOPB	ACTIVE	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	SFYB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

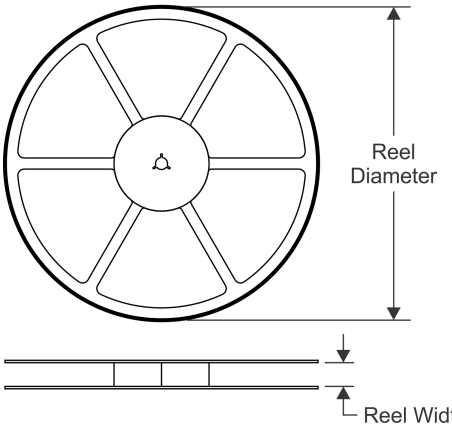
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

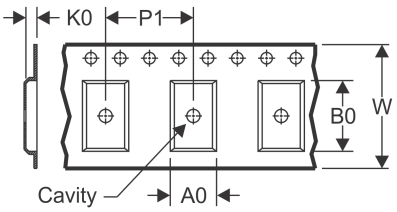
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

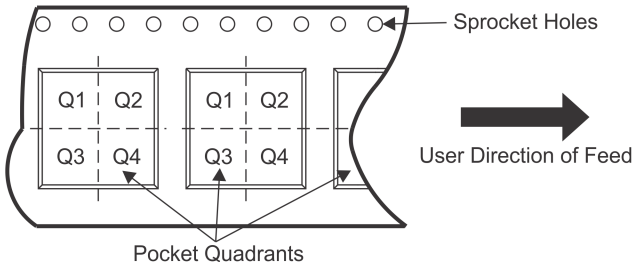


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

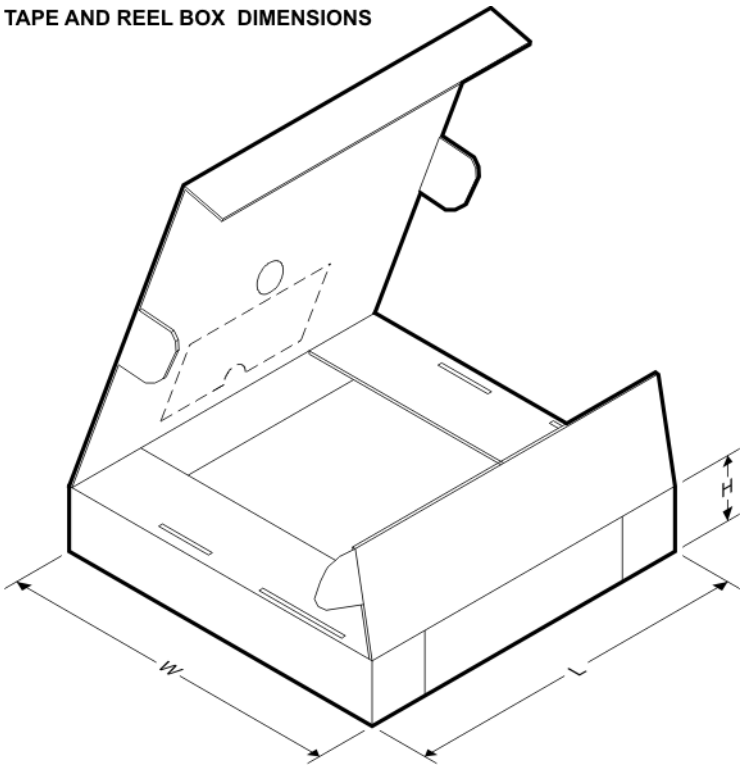
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3203TL/NOPB	DSBGA	YPA	10	250	178.0	8.4	1.96	2.31	0.76	4.0	8.0	Q1

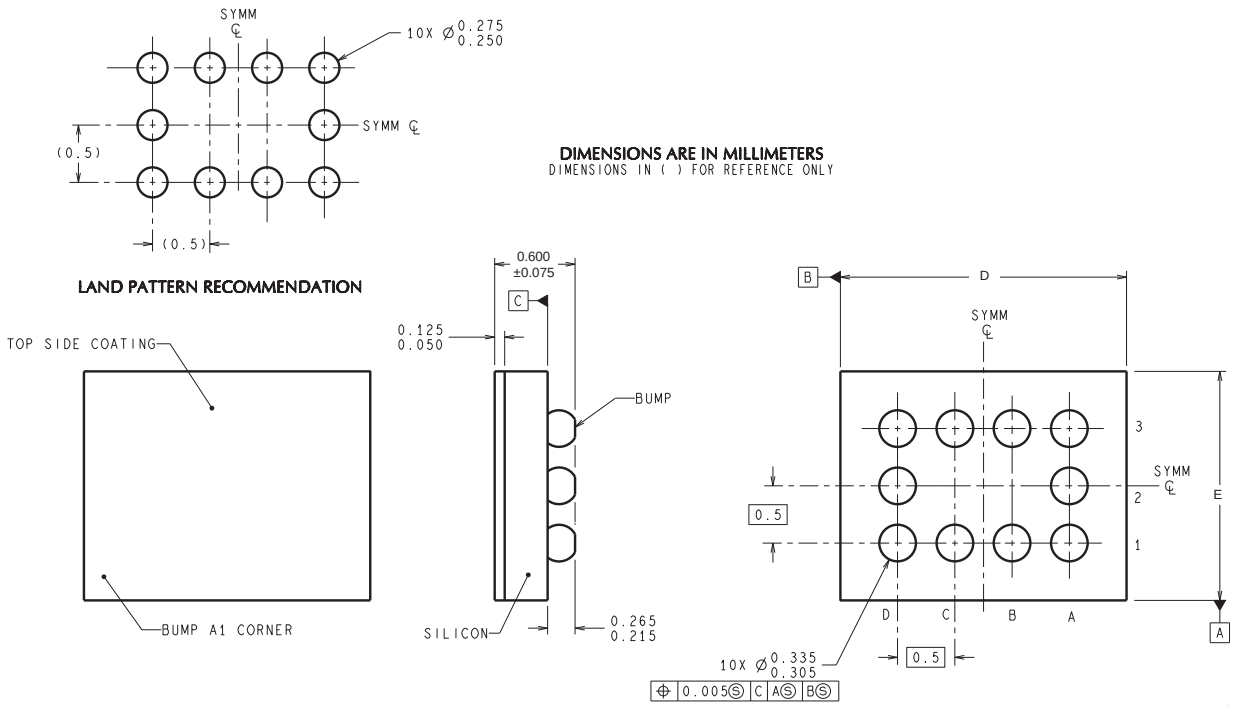
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3203TL/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0

YPA0010



D: Max = 2.226 mm, Min =2.165 mm

E: Max = 1.862 mm, Min =1.801 mm

4215069/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265