

P-Channel 30-V (D-S) MOSFET

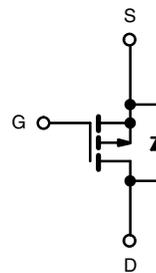
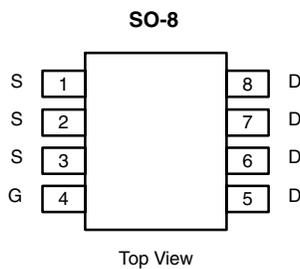
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.02 @ $V_{GS} = -10$ V	-8.0
	0.035 @ $V_{GS} = -4.5$ V	-6.0

FEATURES

- Lead (Pb)-Free Version is RoHS Compliant



RoHS
COMPLIANT



P-Channel MOSFET

Ordering Information: Si4435DY-T1-REV A
Si4435DY-T1-A-E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-8.0
		$T_A = 70^\circ\text{C}$	-6.4
Pulsed Drain Current	I_{DM}	-50	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.5
		$T_A = 70^\circ\text{C}$	1.6
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.0	-2.0	-3.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -30 V, V _{GS} = 0 V, T _J = 70 °C			-5	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-40			A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-10			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = -8.0 A		0.015	0.02	Ω
		V _{GS} = -4.5 V, I _D = -5.0 A		0.022	0.035	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -8.0 A		20		S
Diode Forward Voltage ^b	V _{SD}	I _S = -2.1 A, V _{GS} = 0 V		-0.75	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -4.6 A		47	60	nC
Gate-Source Charge	Q _{gs}			9.5		
Gate-Drain Charge	Q _{gd}			8		
Gate Resistance	R _G			2.75	4.1	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≈ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		16	30	ns
Rise Time	t _r			17	30	
Turn-Off Delay Time	t _{d(off)}			75	120	
Fall Time	t _f			31	80	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -2.1 A, di/dt = 100 A/μs		40	80	

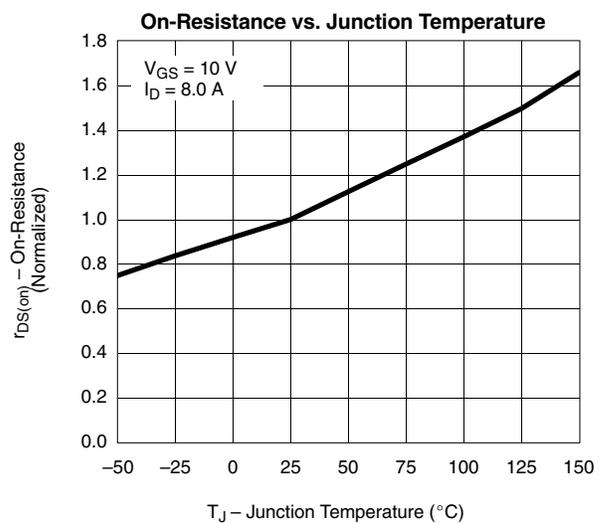
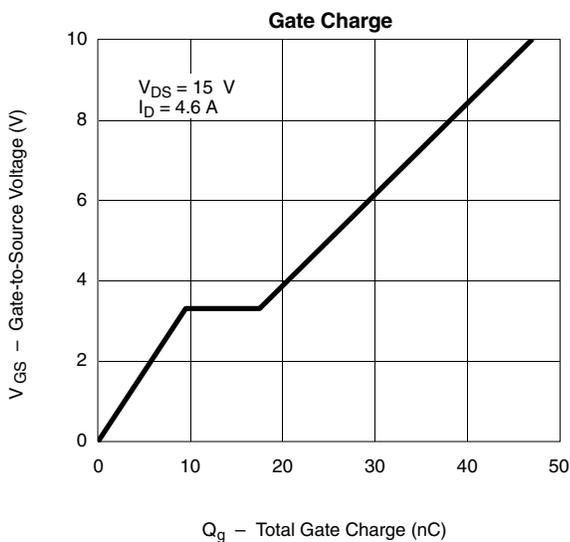
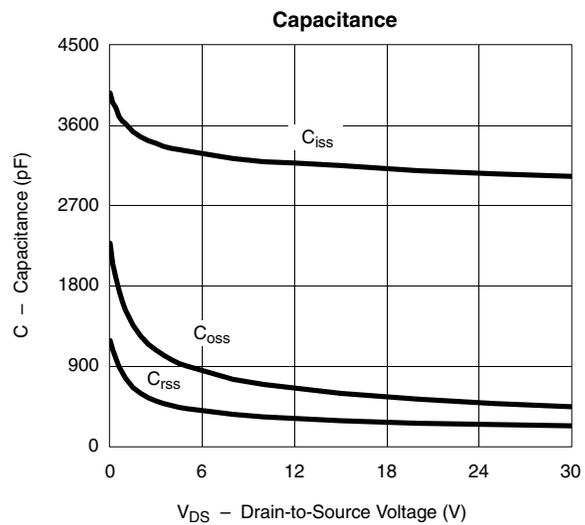
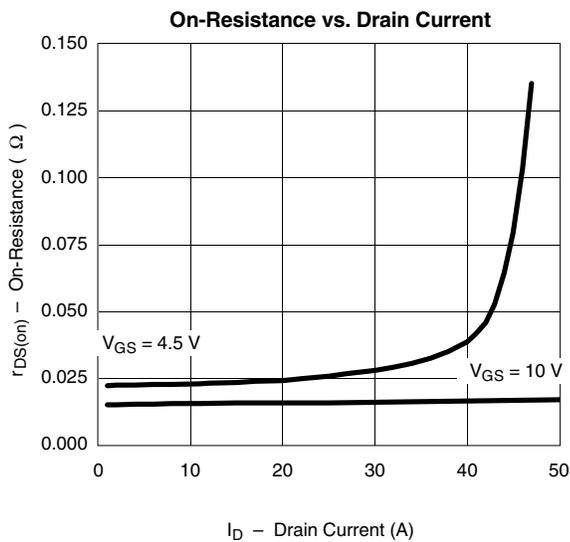
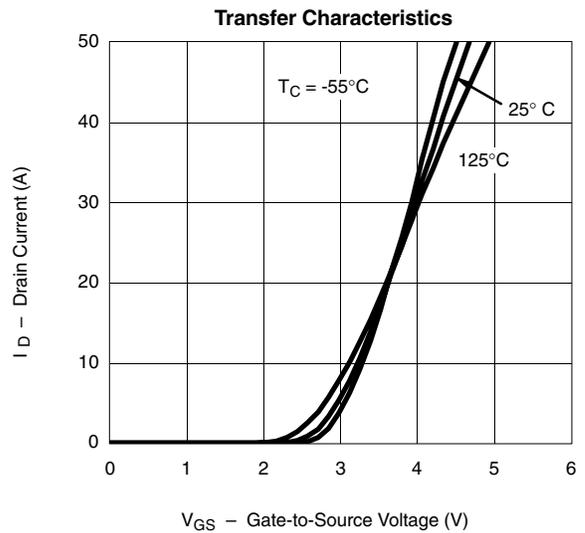
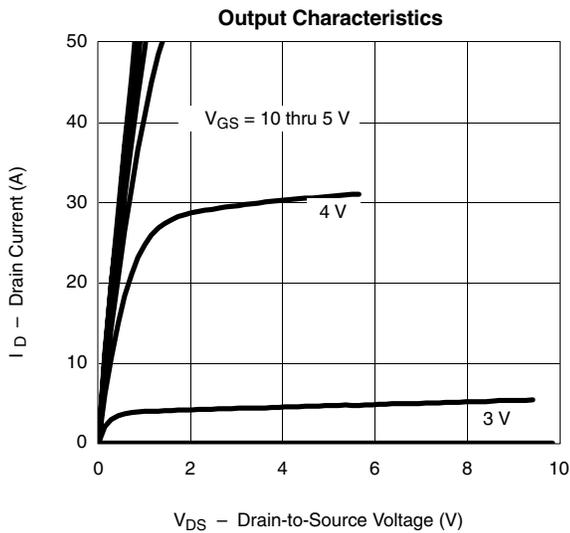
Notes

- a. Guaranteed by design, not subject to production testing. Values shown are for Product Revision A.
 b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

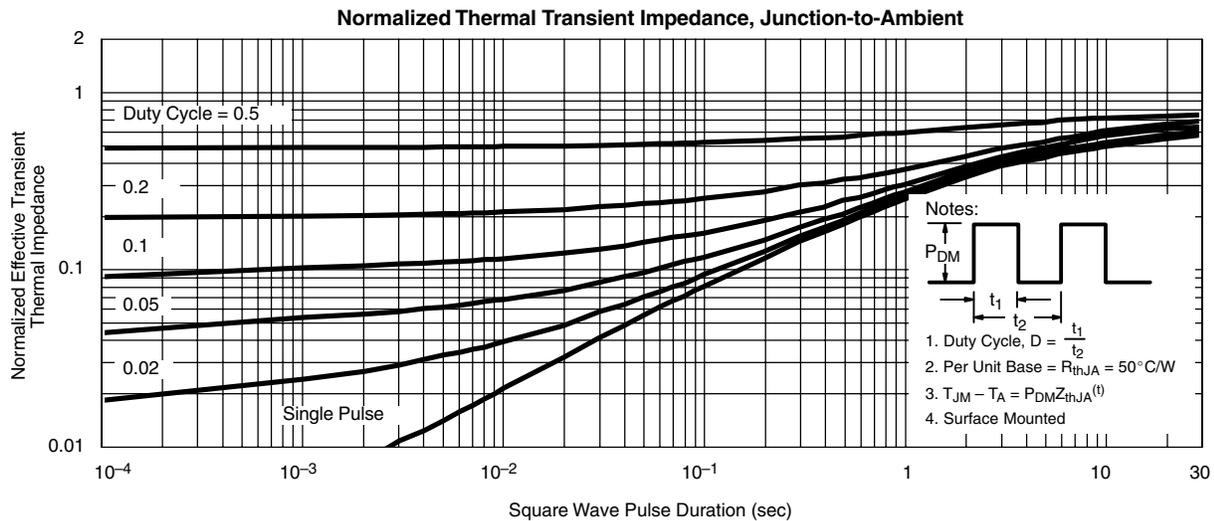
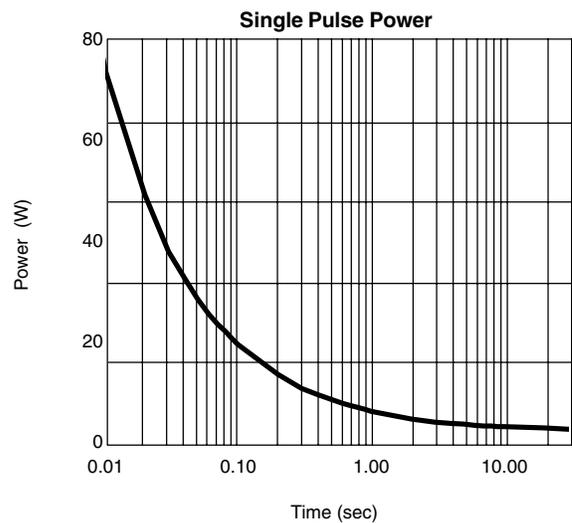
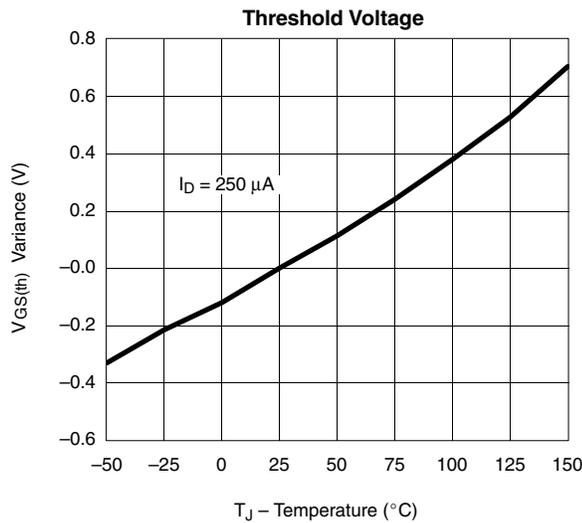
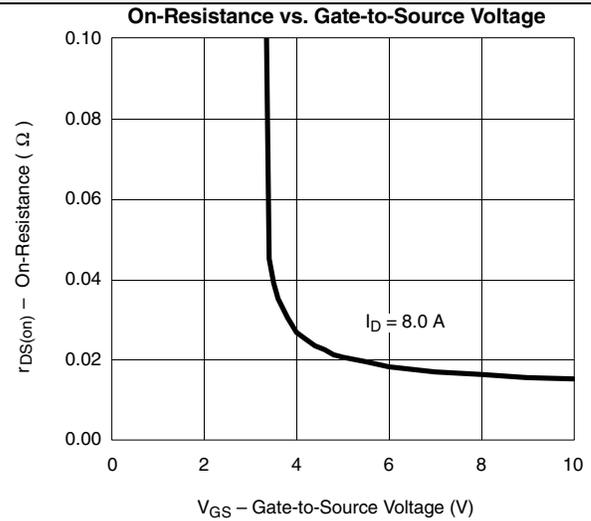
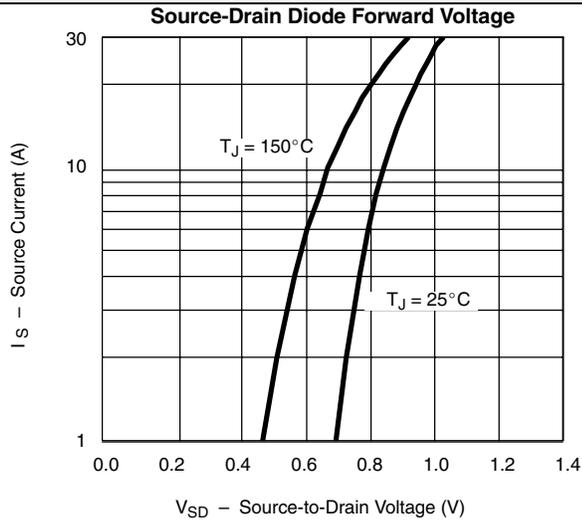
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS, PRODUCT REVISION A (25°C UNLESS NOTED)



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