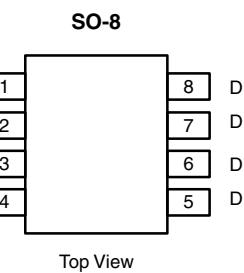


P-Channel 2.5 V (G-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)
- 20	0.008 at V _{GS} = - 10 V	- 18.6	54 nC
	0.010 at V _{GS} = - 4.5 V	- 16.6	
	0.014 at V _{GS} = - 2.5 V	- 14	

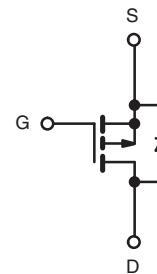
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Adaptor Switch
- High Current Load Switch
- Notebook



Ordering Information: Si4463CDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 20	V	
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	I _D	- 18.6	A	
		- 15		
		- 13.6 ^{a, b}		
		- 10.8 ^{a, b}		
Pulsed Drain Current	I _{DM}	- 60		
Continuous Source-Drain Diode Current	I _S	- 4.5		
		- 2.4 ^{a, b}		
Avalanche Current	I _{AS}	- 20		
Single-Pulse Avalanche Energy	E _{AS}	20	mJ	
Maximum Power Dissipation	P _D	5	W	
		3.2		
		2.7 ^{a, b}		
		1.7 ^{a, b}		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	38	46	°C/W
Maximum Junction-to-Foot	R _{thJF}	20	25	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 85 °C/W.
- Based on T_C = 25 °C.

Si4463CDY

Vishay Siliconix

**SPECIFICATIONS** ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$		- 12		mV/ $^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			3.5		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	- 0.6		- 1.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$			- 1	μA
		$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 70^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq -10 \text{ V}$, $V_{GS} = -10 \text{ V}$	- 30			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}$, $I_D = -13 \text{ A}$		0.006	0.008	Ω
		$V_{GS} = -4.5 \text{ V}$, $I_D = -12 \text{ A}$		0.0073	0.0100	
		$V_{GS} = -2.5 \text{ V}$, $I_D = -5 \text{ A}$		0.011	0.014	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10 \text{ V}$, $I_D = -13 \text{ A}$		60		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		4250		pF
Output Capacitance	C_{oss}			840		
Reverse Transfer Capacitance	C_{rss}			830		
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -10 \text{ A}$		108	162	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -10 \text{ V}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -10 \text{ A}$		54	81	
Gate-Drain Charge	Q_{gd}			7.8		
Gate Resistance	R_g		$f = 1 \text{ MHz}$	18.5		
Turn-On Delay Time	$t_{d(\text{on})}$			0.5	2.3	4.6
Rise Time	t_r	$V_{DD} = -10 \text{ V}$, $R_L = 2 \Omega$ $I_D \geq -5 \text{ A}$, $V_{GEN} = -10 \text{ V}$, $R_g = 1 \Omega$		12	24	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			10	20	
Fall Time	t_f			70	120	
Turn-On Delay Time	$t_{d(\text{on})}$			11	22	
Rise Time	t_r	$V_{DD} = -10 \text{ V}$, $R_L = 2 \Omega$ $I_D \geq -5 \text{ A}$, $V_{GEN} = -4.5 \text{ V}$, $R_g = 1 \Omega$		34	65	
Turn-Off Delay Time	$t_{d(\text{off})}$			35	65	
Fall Time	t_f			70	120	
				30	60	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			- 4.5	A
Pulse Diode Forward Current	I_{SM}				- 60	
Body Diode Voltage	V_{SD}	$I_S = -3 \text{ A}$, $V_{GS} = 0 \text{ V}$		- 0.70	- 1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -2.3 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		54	100	ns
Body Diode Reverse Recovery Charge	Q_{rr}			60	120	nC
Reverse Recovery Fall Time	t_a			26		ns
Reverse Recovery Rise Time	t_b			28		

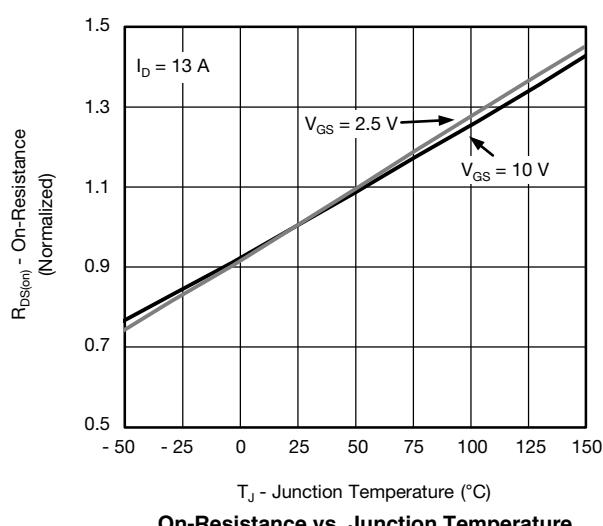
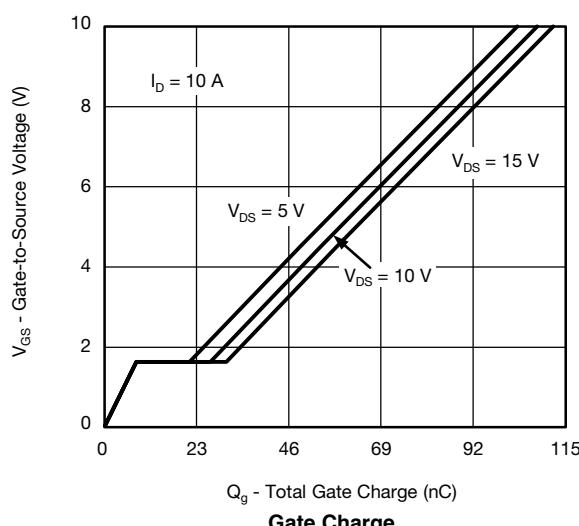
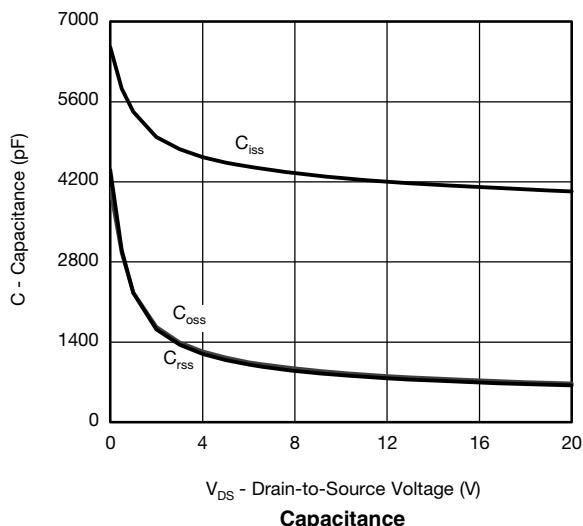
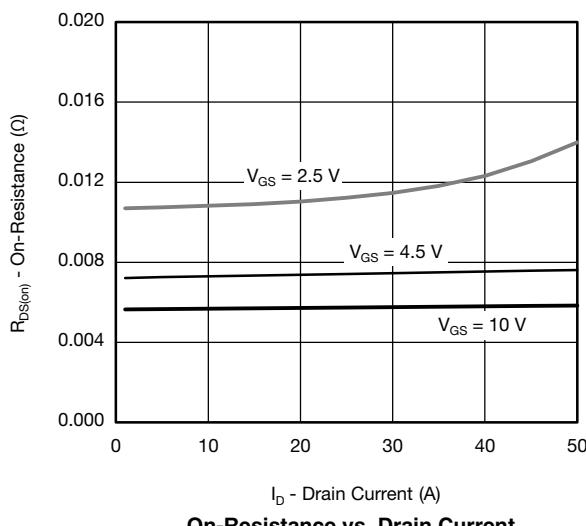
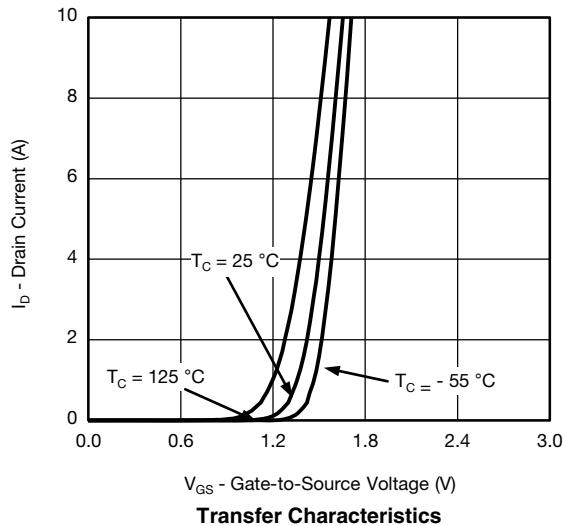
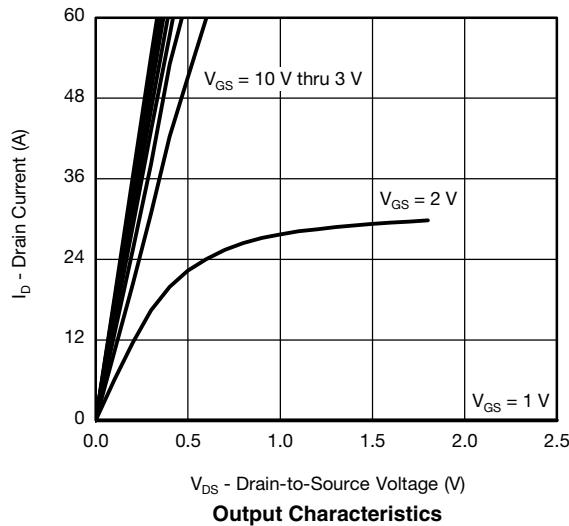
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

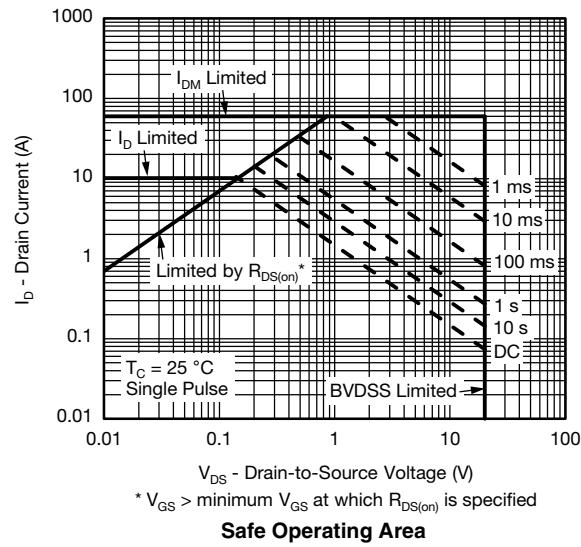
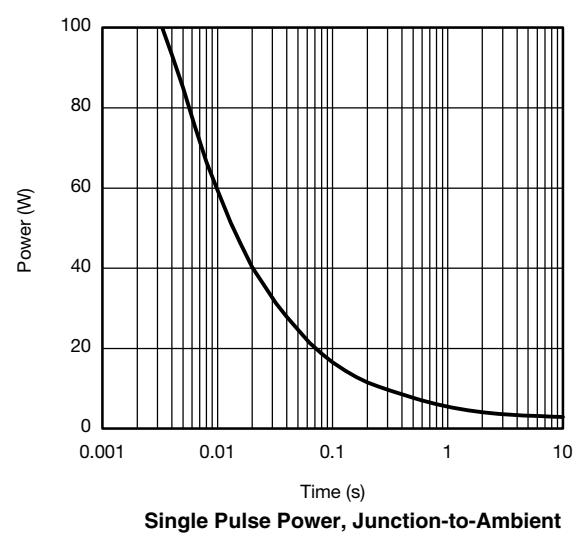
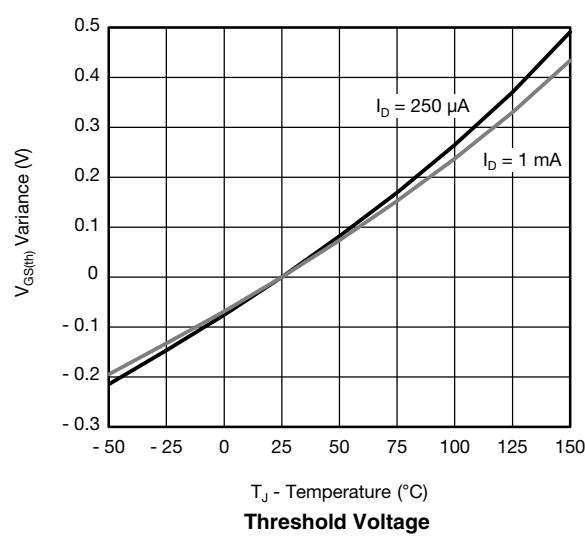
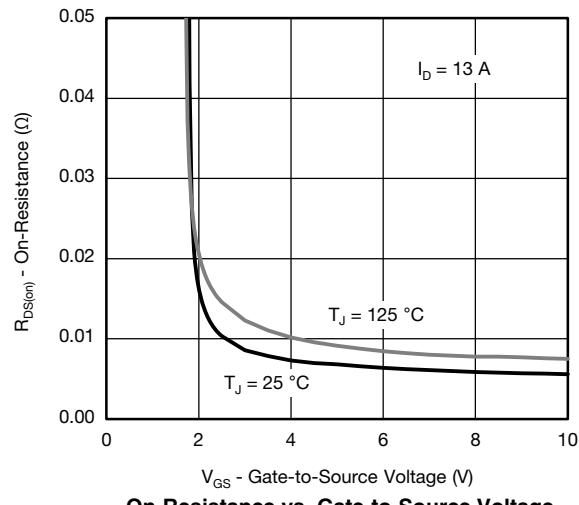
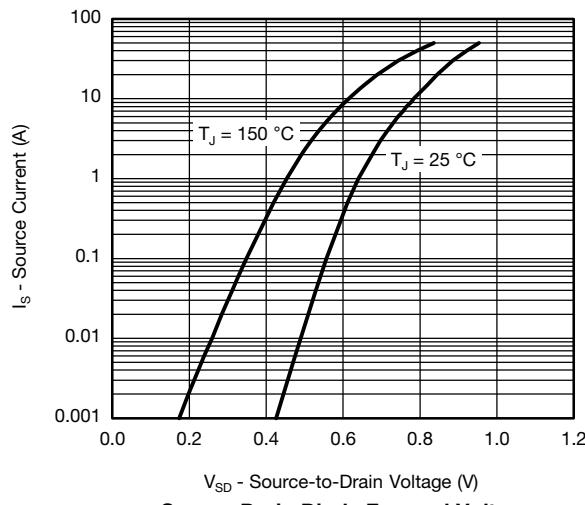
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

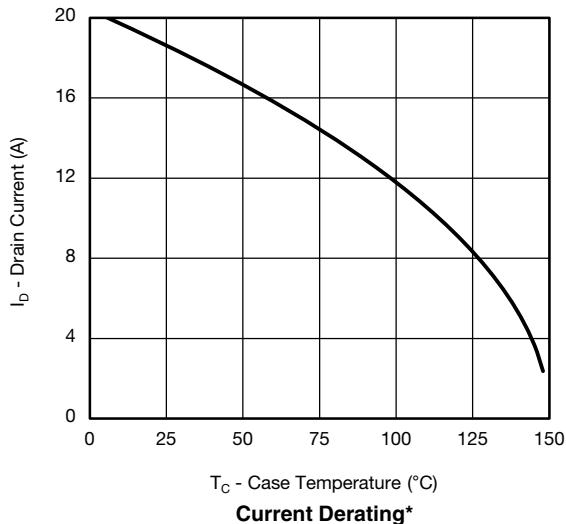
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



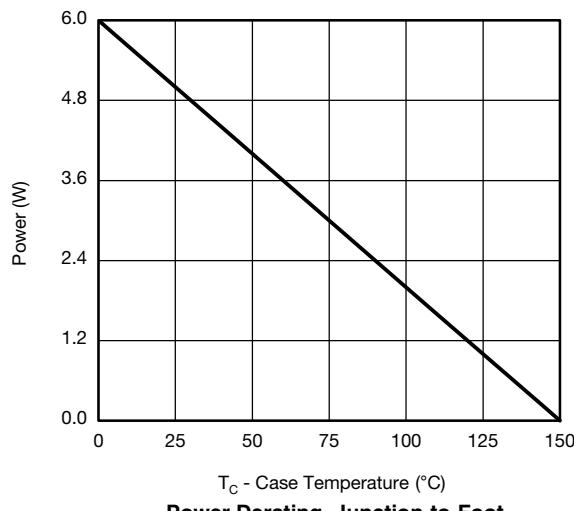
Si4463CDY

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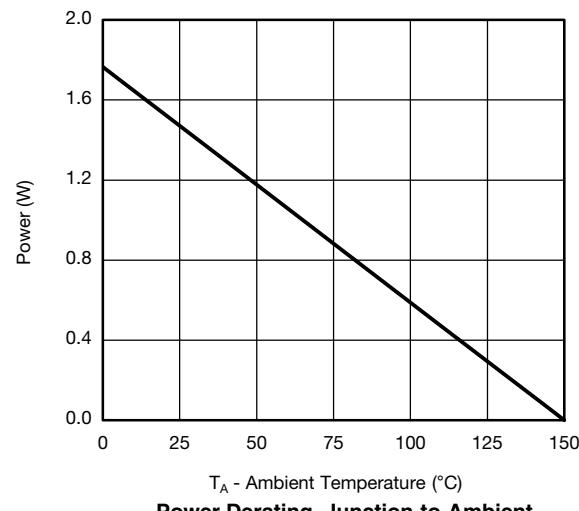
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
 T_C - Case Temperature (°C)

Current Derating*

 T_C - Case Temperature (°C)

Power Derating, Junction-to-Foot

 T_A - Ambient Temperature (°C)

Power Derating, Junction-to-Ambient

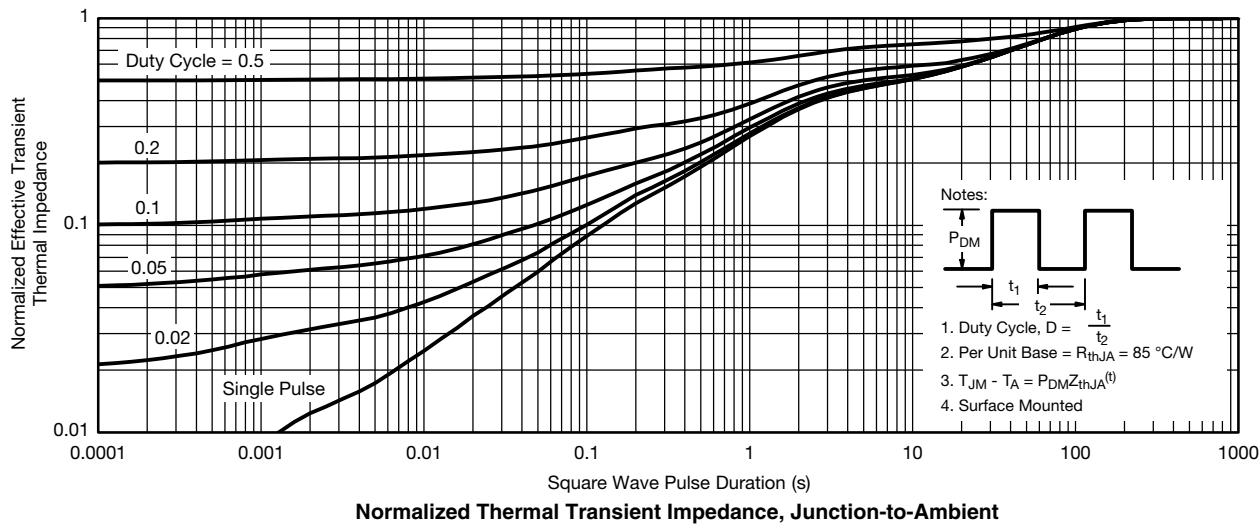
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si4463CDY

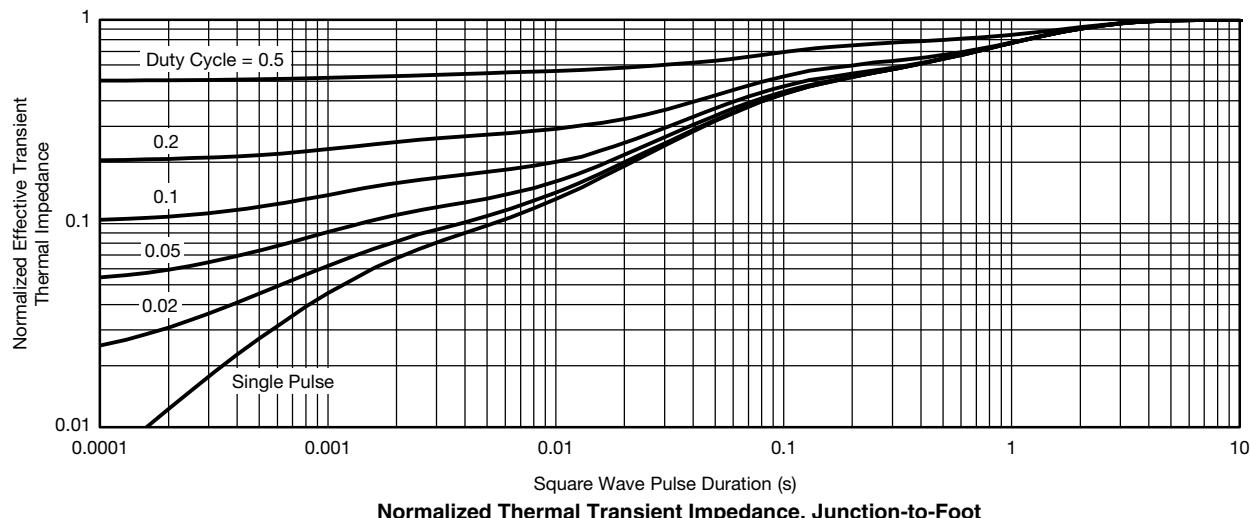
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

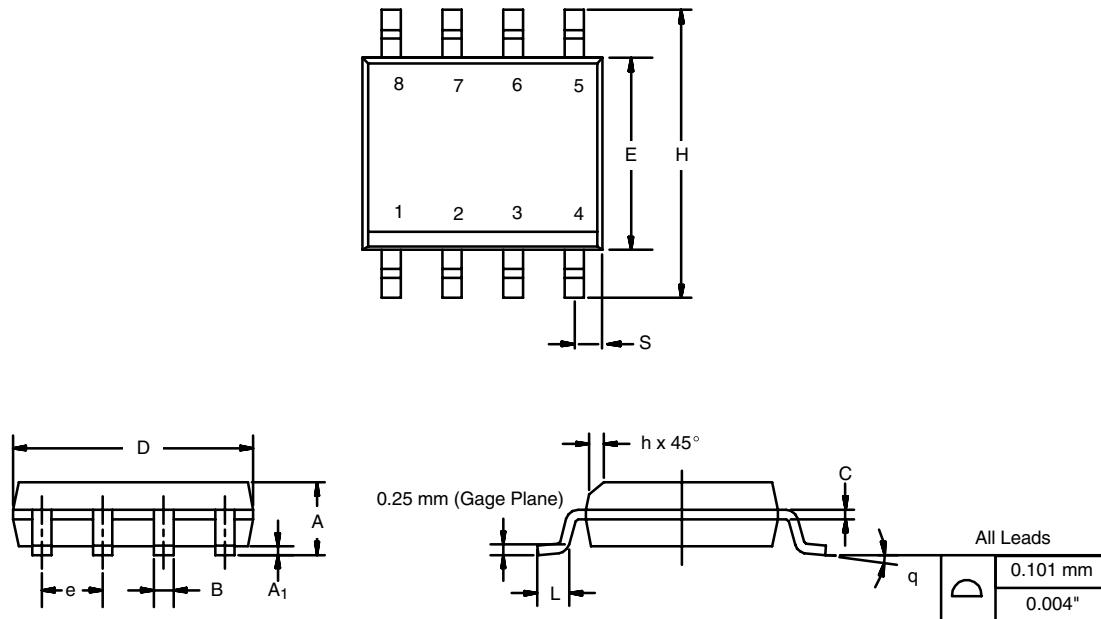


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67335.

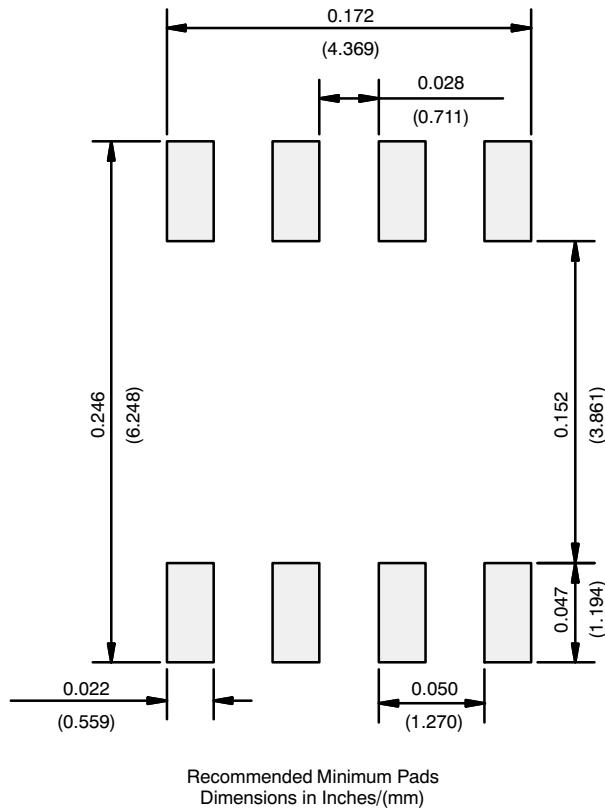
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



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