Si5326-VTSS-EVB

Si5326 Sync-E Vitesse Timing Module User's Guide

1. Introduction

The Si5326-VTSS-EVB is a platform for evaluating Silicon Laboratories' Si5326 Any-Frequency Precision Clock. The Si5326 Any-Frequency Precision Clock is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly-integrated PLL solution that eliminates the need for external VCXO and loop filter components. The device has excellent phase noise and jitter performance. The Si5326 jitter attenuating clock multiplier supports jitter generation of 0.3 ps RMS (typ) across the 12 kHz–20 MHz and 50 kHz–80 MHz jitter filter bandwidths. The DSPLL loop bandwidth is digitally-programmable, providing jitter performance optimization at the application level. This device is ideal for providing clock multiplication/clock division, jitter attenuation, and clock distribution in mid-range and high-performance timing applications. The Si5326-VTSS-EVB is designed as an add-on to a Vitesse Ethernet switch reference board.

The compatible reference boards are listed below, along with each board's Vitesse devices and other features. For more information on any of these boards, visit www.vitesse.com.

- VSCxxxxEV—VSC7407 28-port 1GbE L2 Switch + VSC8664 Synchronous Ethernet PHYs
- VSC5606EV—VSC7640 24-port 1GbE RJ45 + 4-port 10GbE L2/L3 Carrier Ethernet Switch + VSC8664 Synchronous Ethernet PHYs
- VSC5607EV—VSC7460 24-port 1GbE SFP + 4-port 10GbE L2/L3 Carrier Ethernet Switch
- VSC5608EV—VSC7460 48-port 1GbE RJ45 L2/L3 Carrier Ethernet Switch + VSC8512 PHYs
- VSC5611EV—VSC7429 26-port 1GbE L2 Carrier Ethernet Switch + VSC8512 Synchronous Ethernet PHY
- VSC7428EV—VSC7428 8-port 1GbE + 2-port 2.5GbE L2/L3 Carrier Ethernet Switch with fully integrated 1GbE PHYs

Sophisticated management of the Si5326-VTSS-EVB is fully-integrated into the switch management software, which is run by the ARM9™ CPU embedded in the switch engine. The Vitesse VSCxxxxEV Ethernet switch reference board and the Si5326-VTSS-EVB provide a low-cost, no-risk, sophisticated Sync-E-capable Gigabit Ethernet switch solution. The Si5326-VTSS-EVB is compliant with the Vitesse specification, RDR-0017-01-03-SyncE_addon_board.

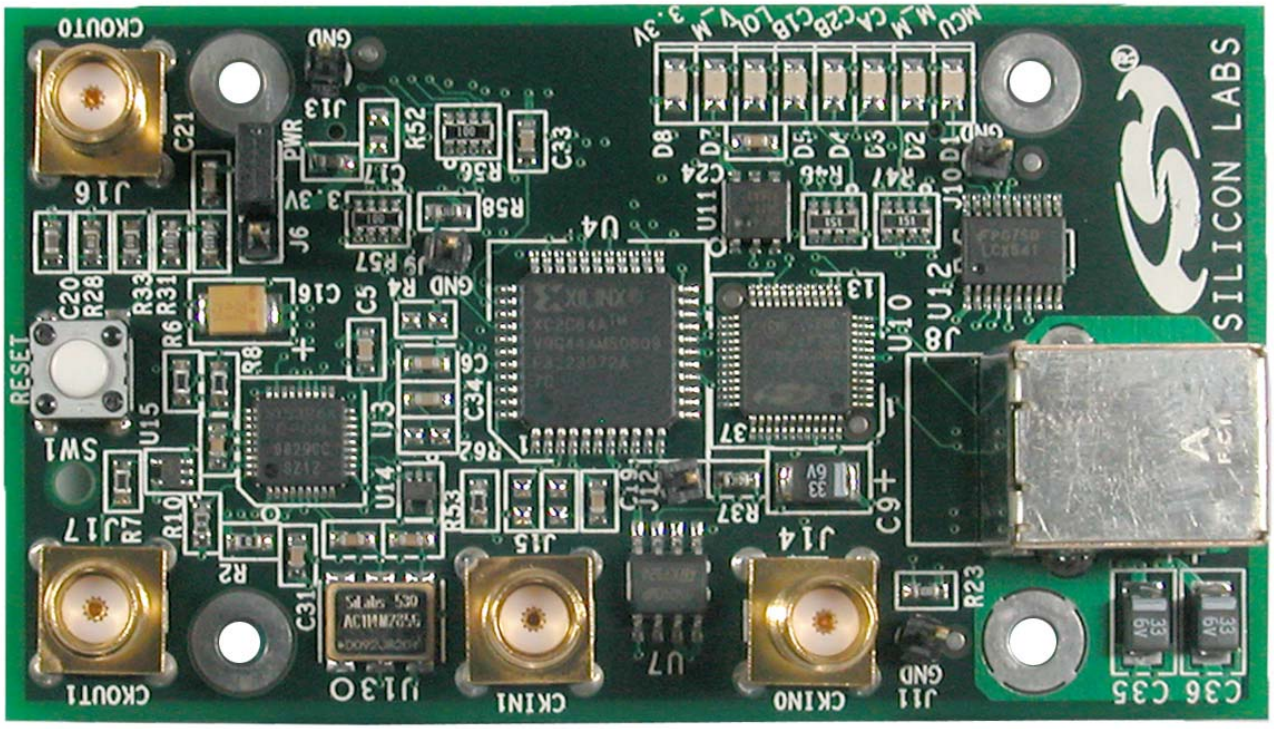

Figure 1. Si5326-VTSS-EVB Top

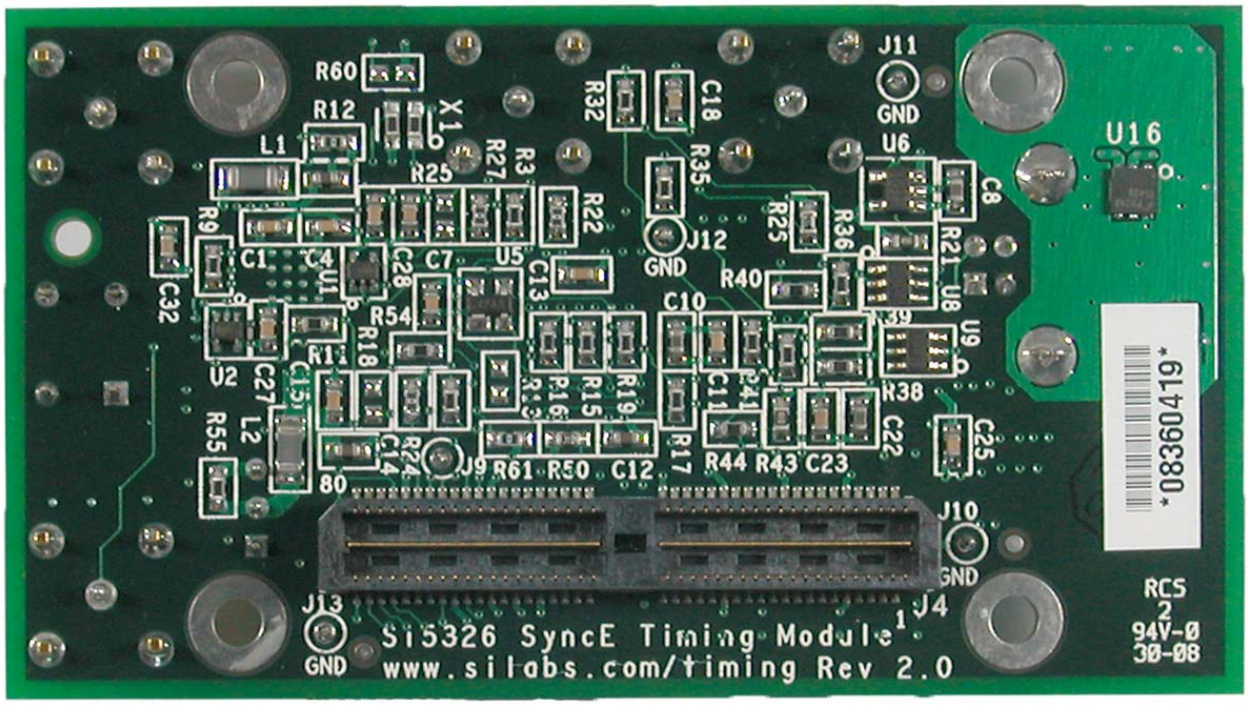

Figure 2. Si5326-VTSS-EVB Bottom

2. Applications

The Si5326 Any-Frequency Precision Clock has a comprehensive feature set, including any-frequency synthesis, two clock inputs, two clock outputs, alarm and status outputs, hitless switching between input clocks, programmable output clock signal format (LVPECL, LVDS, CML, CMOS), output phase adjustment between output clocks, and output phase adjustment between all output clocks and the selected reference input clock (phase increment/decrement). The Si5326 is controlled by a microprocessor or MCU (microcontroller unit) via an I^2C or SPI interface and is a jitter-attenuating clock multiplier with a loop bandwidth ranging from 60 Hz to 8.4 kHz. For more details, consult the Silicon Laboratories timing products website at www.silabs.com/timing.

The evaluation board (EVB) has a Silicon Labs MCU (C8051F340) that supports USB communications with a PC host. The device is controlled and monitored through the serial port (either SPI or I^2C). The serial port can connect to either the MCU or to the Vitesse Ethernet switch reference board. A CPLD that performs arbitration between the slaves and hosts sits between the MCU, the switch reference board, and the Any-Frequency Precision Clock device. The EVB is configured for CMOS clock inputs and outputs. Clock IO going to/from the Vitesse Ethernet switch reference board can be monitored using separate SMA connectors. The EVB can also be run stand-alone using either a separate power supply connector or directly from USB power. LEDs are provided for convenient monitoring of key status signals.

3. Features

The Si5326-VTSS-EVB includes the following:

- CD with documentation and EVB software including the DSPLLsim configuration software utility
- EVB circuit board including an Si5326
- User's Guide (this document)

4. Si5326-VTSS-EVB Configuration and Management Quick Start

The Si5326-VTSS-EVB can be configured, controlled, and monitored with the Vitesse VSCxxxxEV evaluation board or by a host PC's USB port. The USB port should be used when it is necessary to customize the Si5326's configuration. For more information, see "7.Installing Software for the Direct Control of the Si5326-VTSS-EVB" on page 10.

4.1. Managing the Vitesse VSCxxxxEV Ethernet Switch Reference Board and an Attached Si5326-VTSS-EVB through a Web GUI

Before you can log in to this, you must know the IP address of the VSCxxxxEV board. First, connect any of the VSCxxxxEV Ethernet ports to your computer network, which should provide access to a DHCP server. Power up the VSCxxxxEV board and wait a few minutes. Now, the VSCxxxxEV board has received an IP address from the DHCP server. Next, connect your PC to the VSCxxxxEV board using a serial cable (DB9 connector) and a terminal program, such as Windows' Hyperterm (115200 baud, 8 data bits, 1 stop bit, no parity) for getting access to the VSCxxxxEV command line interface. The CLI command "ip conf" will return the IP address of the VSCxxxxEV.

Then you can log in to the VSCxxxxEV management web GUI using a web browser and the IP address from above (type "http://xx.xx.xx.xx" in your browser's address line, with xx.xx.xx.xx being the IP address of the VSCxxxxEV). A password request will appearl; user name is "admin", and password is blank/empty. Select the SyncE bullet in the configuration menu, and you are presented with the Si5326-VTSS-EVB management GUI shown in Figure 3.

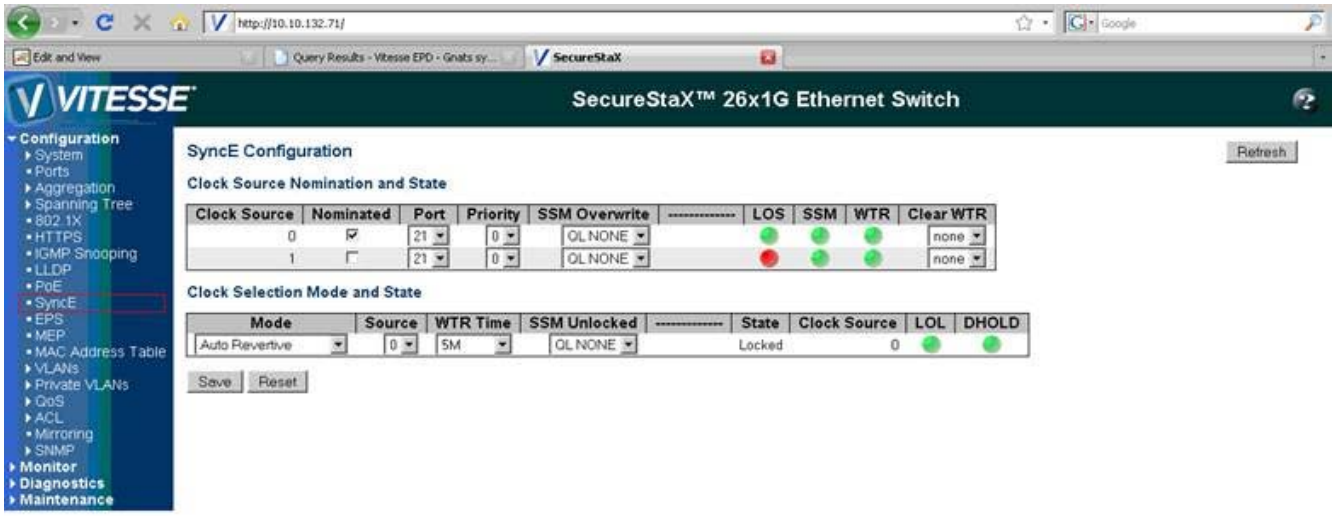

Figure 3. Si5326-VTSS-EVB Management GUI

The GUI help pages provide information on the fields available in the management interface and are accessed through the question mark button at the top right.

If you need to update the VSCxxxxEV firmware, refer to Vitesse application note “AN0123: Reference System Software Update", which is available as part of the "VSC7407 Software, Tools, and Application Notes" collateral package at www.vitesse.com.

5. Functional Description

The Si5326-VTSS-EVB and its software allow for a complete and simple evaluation of the functions, features, and performance of the Si5326 Any-Frequency Precision Clock.

5.1. Block Diagram

Refer to the block diagram of the evaluation board shown in Figure 4. The VSCxxxxEV communicates to the Si5326 through the CPLD. The MCU also communicates to the host PC over a USB connection, also through the CPLD.

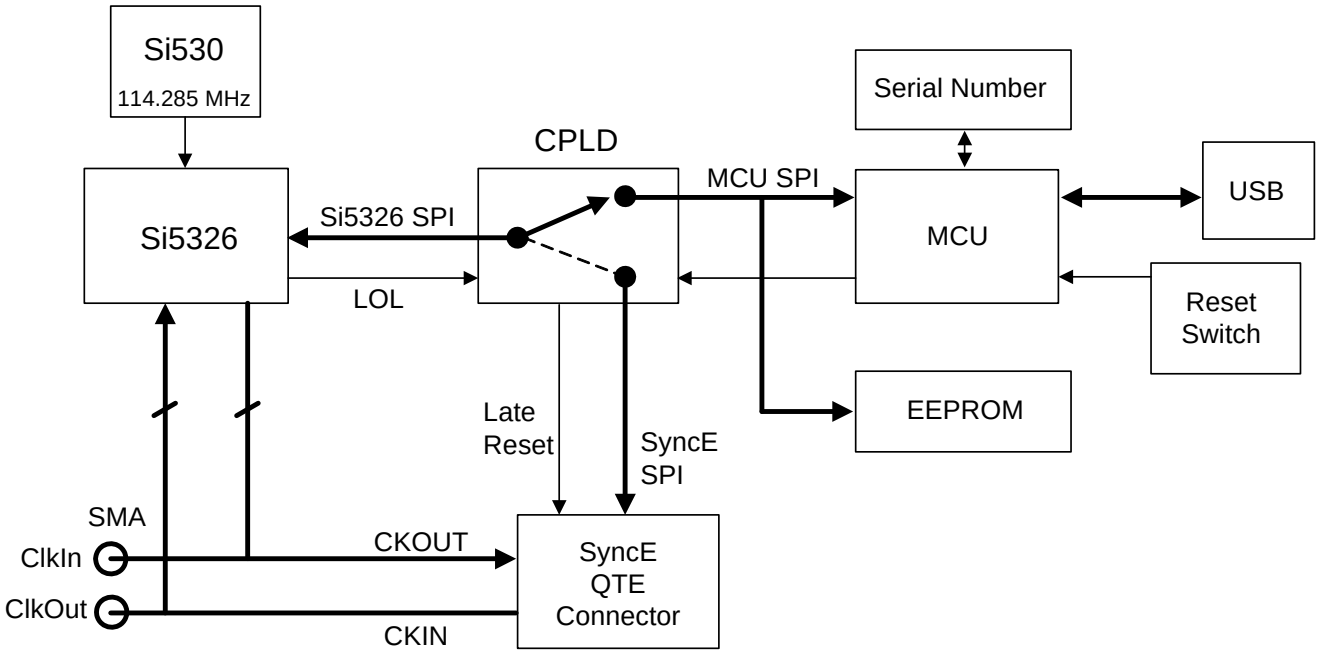

Figure 4. Si5326-VTSS-EVB Block Diagram

5.2. Si5326 Input and Output Clocks

The Si5326 has two clock inputs coming from the VSCxxxxEV that are dc-coupled and can be monitored at two SMA output connectors. These SMA connectors can optionally be configured to be clock inputs instead of being clock monitoring outputs. A 114.285 MHz differential PECL Si530 oscillator provides the reference supply to the Si5326. There are optional provisions for using a lower-cost third overtone crystal instead of the Si530 oscillator. The clock outputs go to both the VSCxxxxEV and two SMA connectors. All clock input and output is configured for dc-coupled LVCMOS operating at 3.3 V.

The CPLD arbitrates between the two possible SPI bus masters: the MCU and the VSCxxxxEV. The arbitration logic is very simple: the MCU has priority over the VSCxxxxEV and will override it at any time. The CPLD also generates the Late Reset signal that goes to the VSCxxxxEV. Late Reset holds the VSCxxxxEV in a reset condition until the clock output of the Si5326 has been initialized and its output clock is stable. The CPLD also buffers the alarm output of the Si5326 and sends it to the VSCxxxxEV interrupt.

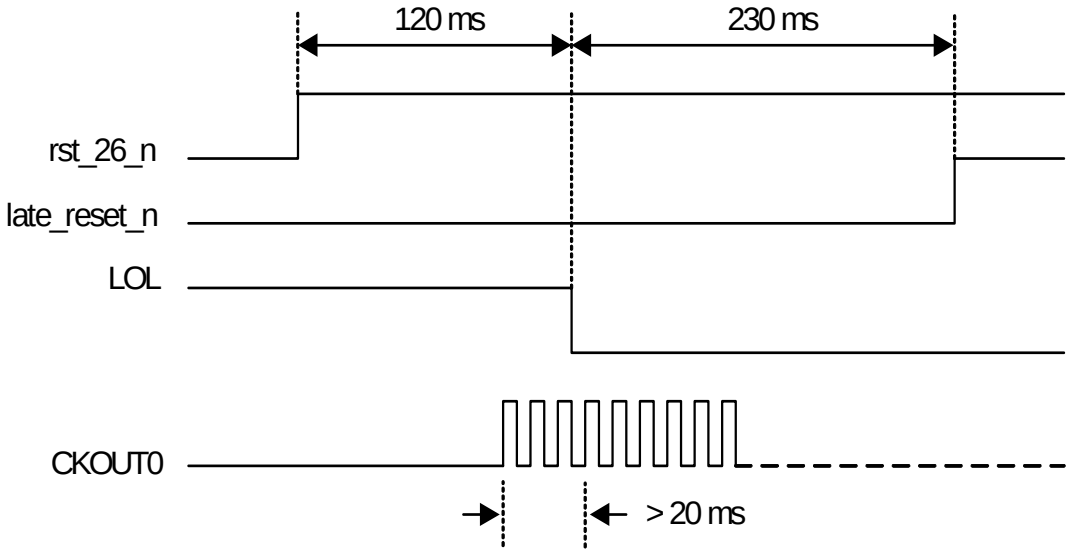

Figure 5. Late Reset Timing

The MCU connects to a host PC's USB port. It also loads the Si5326 with a power-up frequency plan immediately after a reset condition goes away. The power-up frequency plan is contained in the EEPROM, and the EVB has an MCU-readable serial number device so that the EVB can be uniquely identified.

6. Connectors and LEDs

6.1. LEDs

The board contains eight LEDs that provide a quick and convenient means of determining board status.

Table 1. LED Status and Description

LED	Color	Label	Description
D1	yellow	MCU	Normally ON; flashes for MCU errors
D2	yellow	M_M	MCU Master; ON when the MCU is the SPI bus master
D3	green	CA	OFF when CKIN1 is selected, ON for CKIN2 or Free Run
D4	red	C2B	ON when CKIN2 is bad or not present
D5	red	C1B	ON when CKIN1 is bad or not present
D6	red	LOL	ON when there is a loss of lock (LOL)
D7	green	V_M	ON when VSCxxxxEV is the SPI bus master
D8	Green	3.3V	ON when 3.3 V is present

6.2. User Jumpers and Headers

See Figure 6 to locate the jumpers and connectors described below.

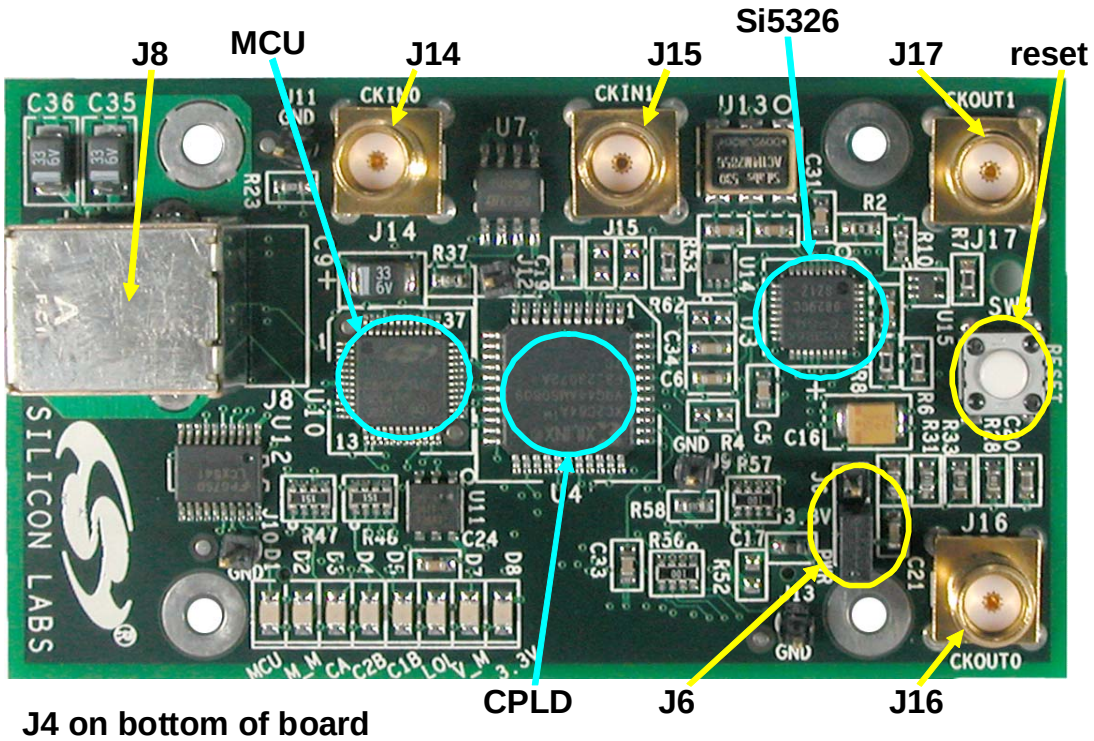

Figure 6. Connectors and Jumper Header Locations

J14 and J15 are the SMA output connectors for monitoring CKIN0 and CKIN2, respectively. By adding and removing components (see schematic), these connectors can be configured as 3.3 V LVCMOS clock inputs.

J16 and J17 are the SMA clock output monitor connectors for CKOUT0 and CKOUT1, respectively. They are dc-coupled 3.3 V LVCMOS outputs that include series termination.

J4 is the connector that goes to the VSCxxxxEV motherboard. It supplies the power, clock inputs/outputs, SPI bus signal, and other control and monitoring signals. The pinout for J4 is a subset of that described in Vitesse specification RDR-0017-01-03-SyncE_addon_board.

Table 2. Pin Names

Pin	Name	Pin	Name
1	FastLink_N_0	2	—
3	ClkIn0	4	—
5	FastLink_N_1	6	—
7	ClkIn1	8	—
9	—	10	—
11	Gnd	12	—
13	—	14	Gnd
15	—	16	—
17	—	18	—
19	—	20	—
21	—	22	—
23	—	24	—
25	—	26	—
27	—	28	—
29	Gnd	30	Gnd
31	—	32	—
33	—	34	—
35	—	36	—
37	—	38	—
39	Gnd	40	Gnd
41	FreeClkIn	42	—
43	ClkOut0	44	—
45	—	46	—
47	ClkOut1	48	—
49	Gnd	50	—
51	ClkOut2	52	—
53	Gnd	54	—
55	—	56	—
57	Gnd	58	Gnd
59	SPI_EN_n	60	SPI_MOSI
61	SPI_CLK	62	SPI_MISO
63	Gnd	64	Gnd
65	I2C_SDA	66	LATE_RESET_n

Table 2. Pin Names (Continued)

Pin	Name	Pin	Name
67	I2C_SCL	68	INT_n
69	VCC_3V3	70	PRESENT_n
71	VCC_3V3	72	Gnd
73	RST_N (Spare0)	74	TCK (Spare4)
75	C2CK (Spare1)	76	TDI (Spare5)
79	C2D (Spare2)	78	TDO (Spare6)
79	VCCAUX (Spare3)	80	TMS, Spare7)

6.2.1. Stand Alone Power

The EVB can optionally be powered from the USB connector for stand-alone operation. J6 is normally jumpered from pin1 to pin 2 so that power comes from the VSCxxxxEV. To power the Si5326-VTSS-EVB from the USB port, jumper J6 pin 2 to J6 pin 3.

6.2.2. USB Connection

J8 is the USB connector that goes to the PC host. The Si5326-VTSS-EVB is normally powered from the VSCxxxxEV, not the USB port.

7. Installing Software for the Direct Control of the Si5326-VTSS-EVB

Some applications may call for the input and/or output frequency of the Si5326-VTSS-EVB to be custom-tailored. It may also be necessary to change or monitor internal Si5326 registers. To accomplish this, the Precision Clock EVB Software should be installed. The following sections describe how to install the EVB software.

The procedure for installing the Precision Clock EVB Software, DSPLLsim, is included on the release CD for the Si5326-VTSS-EVB. DSPLLsim and its release notes can also be downloaded from the Silabs web site: www.silabs.com/timing. Follow the links for 1-PLL Jitter Attenuators and look under the Tools tab.

Note: These programs can control any of the Any-Frequency Precision Clock devices including the Si5316, Si532x, and Si536x devices. This software can be installed once per PC and used for all available Precision Clock EVBs.

8. Si5326-VTTS-EVB Schematics

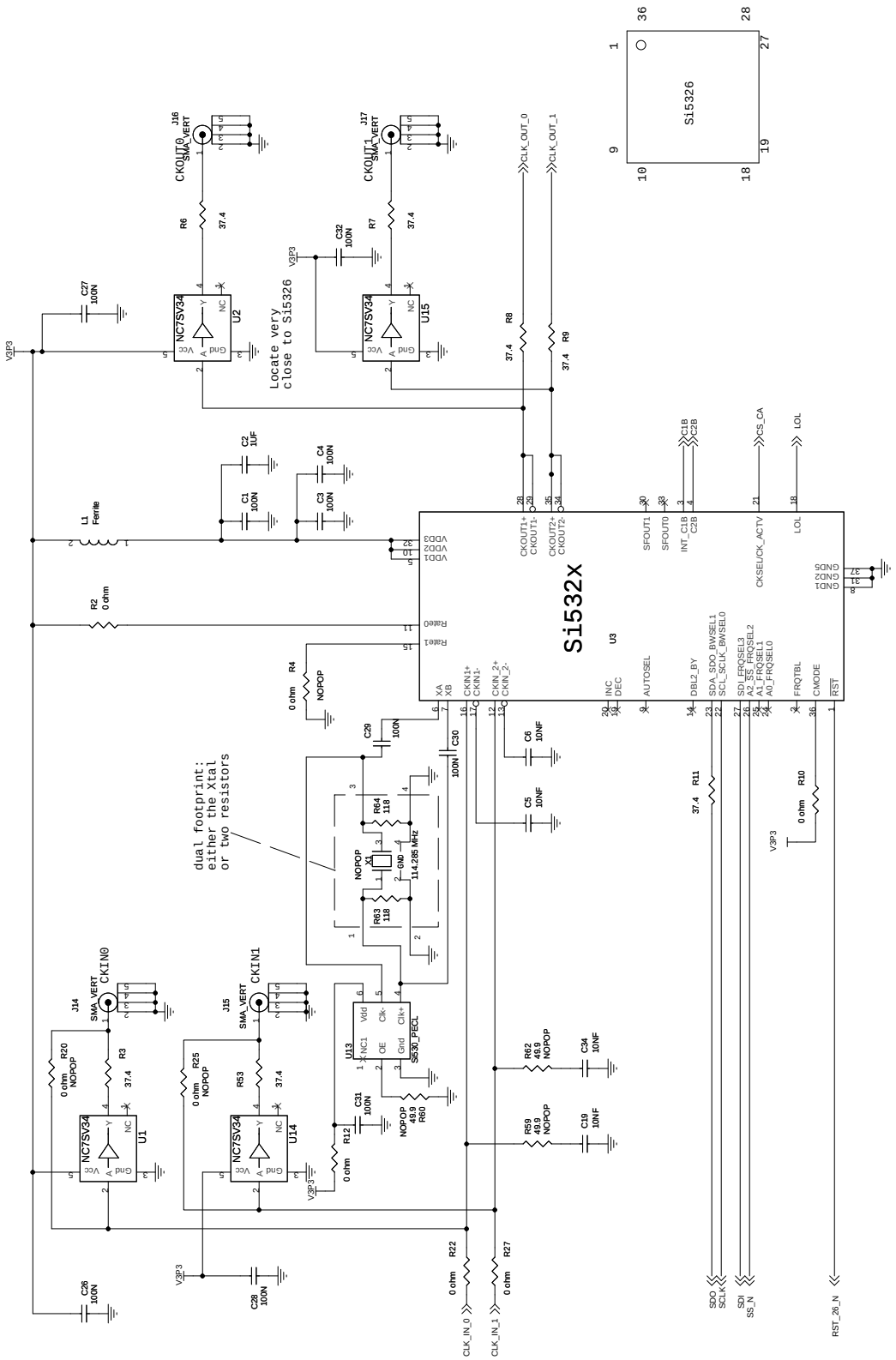

Figure 7. Si5326 Schematic

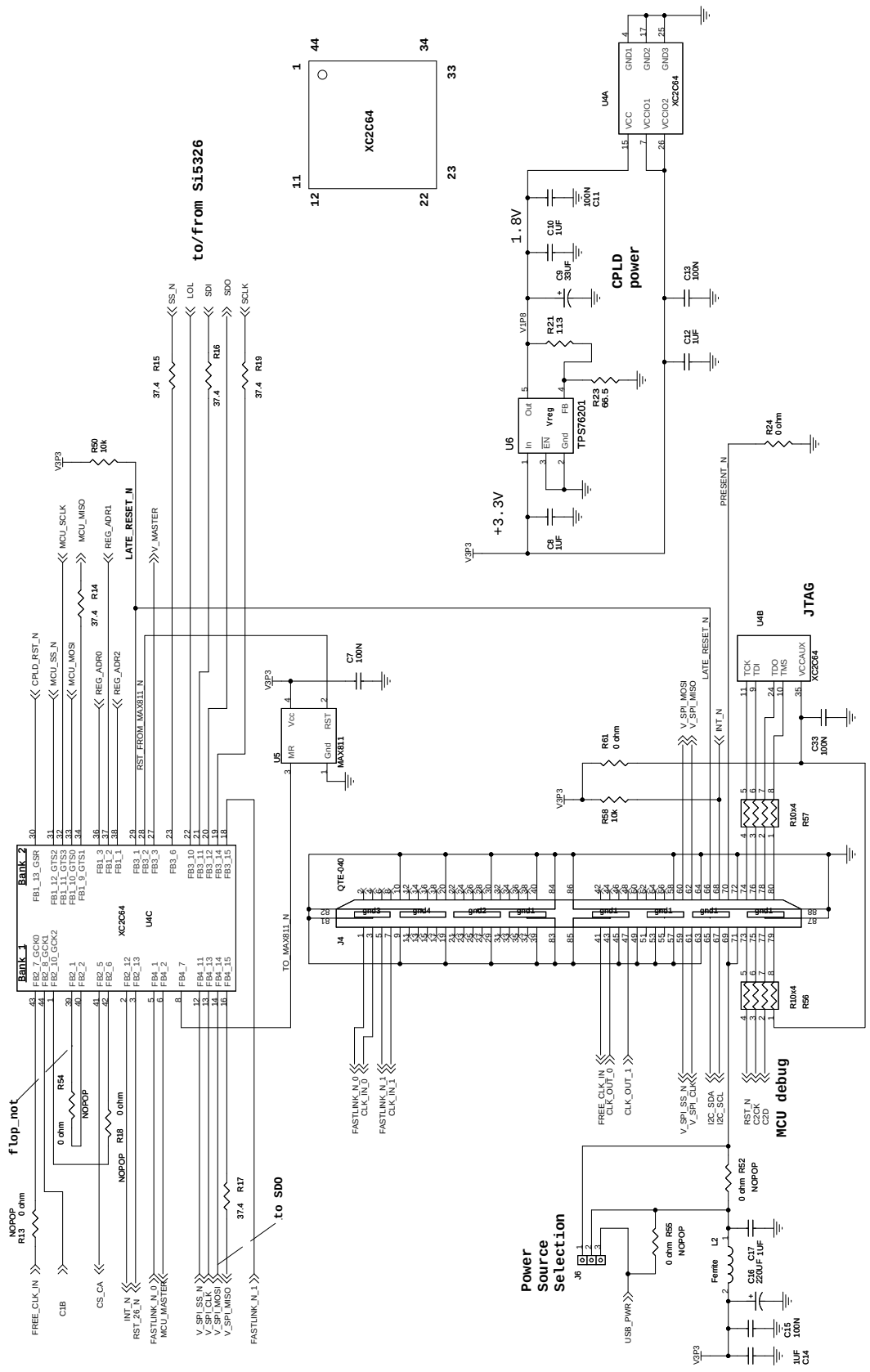

Figure 8. Si5326 CPLD

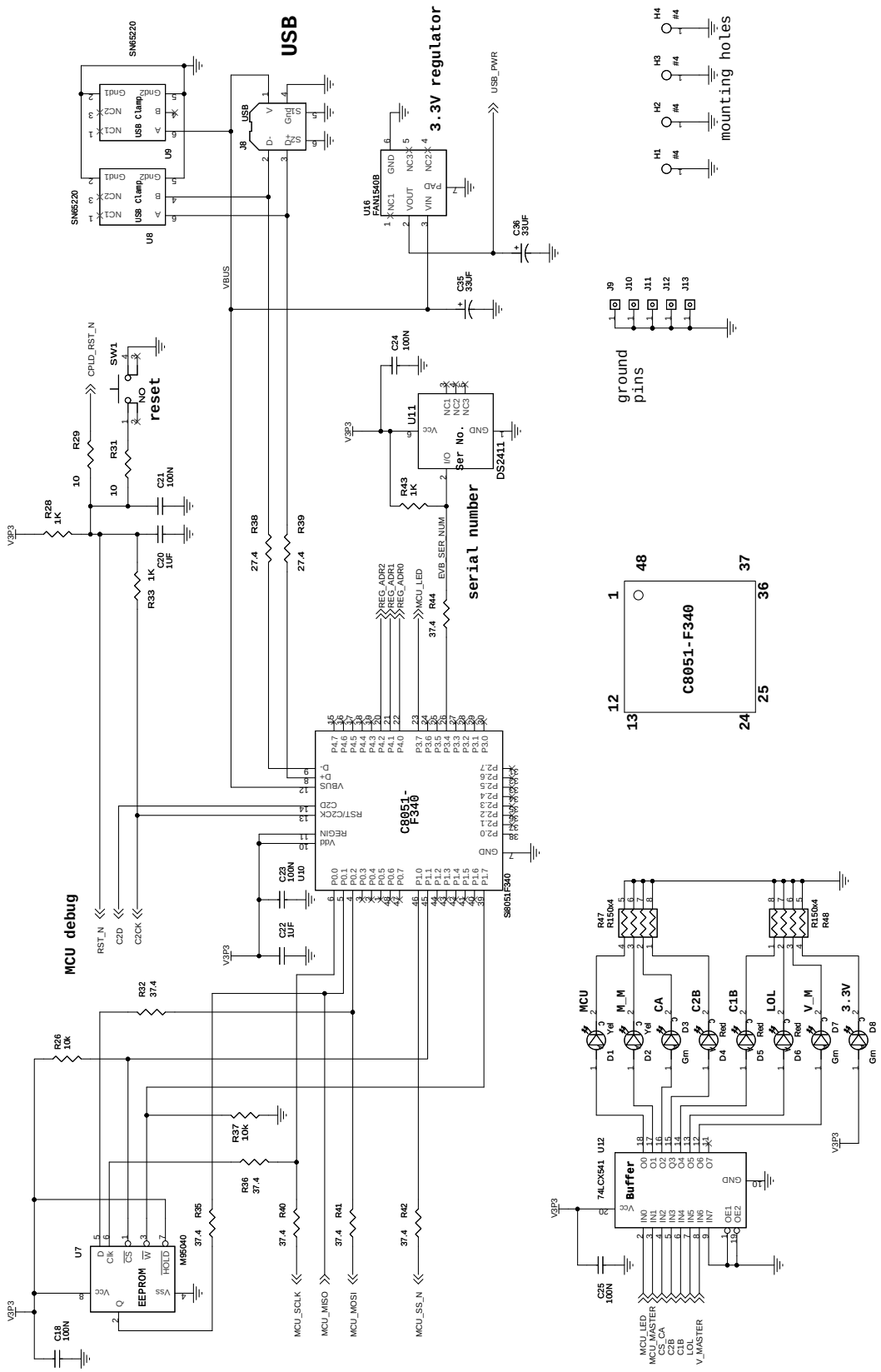

Figure 9. Si5326-MCU

9. Bill of Materials

Table 3. Bill of Materials

Item	Qty	Reference	Part	Mfgr	Mfr Part Num	Digi-Key
1	20	C1,C3,C4,C7,C11, C13,C15,C18,C21, C23,C24,C25,C26, C27,C28,C29,C30, C31,C32,C33	100 nF	Venkel	C0603X7R160-104KNE	
2	8	C2,C8,C10,C12,C14, C17,C20,C22	1 µF	Venkel	C0603X7R6R3-105KNE	
3	4	C5,C6,C19,C34	10 nF	Venkel	C0603X7R160-103KNE	
4	3	C9,C35,C36	33 µF	Venkel	TA006TCM336MBR	
5	1	C16	220 µF	Kemet	T494B227M004AT	399-4631-1-ND
6	2	D1,D2	Yel	Lumex	SML-LXT0805YW-TR	67-1554-1-ND
7	3	D3,D7,D8	Grn	Lumex	SML-LXT0805GW-TR	67-1553-1-ND
8	3	D4,D5,D6	Red	Lumex	SML-LXT0805SRW-TR	67-1555-1-ND
10	1	J4	QTE-040	Samtec	QTE-040-01-L-D-A	SAM8132-ND
11	1	J6	Jmpr_3pin			
12	1	J8	USB	FCI	61729-0010BLF	609-1039-ND
13	5	J9,J10,J11,J12,J13	Jmpr_1pin			
14	4	J14,J15,J16,J17	SMA_VERT	Johnson	142-0701-211	J494-ND
15	2	L1,L2	Ferrite	Venkel	FBC1206-471H	
16	7	R2,R10,R12, R22,R24,R27,R61	0 Ω	Venkel	CR0603-16W-000T	
17	19	R3,R6,R7,R8,R9,R11, R14,R15,R16,R17, R19,R32,R35,R36, R40,R41,R42,R44, R53,R54,R55	37.4 Ω	Venkel	CR0603-16W-37R4FT	
19	1	R21	113 Ω	Venkel	CR0603-16W-1130FT	
20	1	R23	66.5 Ω	Venkel	CR0603-16W-66R5FT	
21	4	R26,R37, R50,R58	10 kΩ	Venkel	CR603-16W-1002FT	
22	3	R28,R33,R43	1 kΩ	Venkel	CR0603-16W-1001FT	
23	2	R29,R31	10 Ω	Venkel	CR0603-16W-10R0FT	
24	2	R38,R39	27.4 Ω	Venkel	CR0603-16W-27R4FT	
25	2	R47,R48	R150x4	Panasonic	EXB-38V151JV	Y9151CT-ND
26	2	R56,R57	R10x4	Panasonic	EXB-38V100JV	Y9100CT-ND
28	1	SW1	NO	Mountain Switch	101-0161-EV	101-0161(Mouser)

Table 3. Bill of Materials

Item	Qty	Reference	Part	Mfgr	Mfr Part Num	Digi-Key
29	4	U1,U2,U14,U15	NC7SV34	Fairchild	NC7SV34P5X	NC7SV34P5X-ND
30	1	U3	Si5326C-C-GM	Silicon Labs	5326C-C-GM	
32	1	U4	XC2C64	Xilinx	XC2C64A-7VQG44C	122-1410-ND
33	1	U5	MAX811	Maxim	MAX811TEUS	MAX811TEUS-ND
34	1	U6	TPS76201	TI	TPS76201DBVT	296-11013-1-ND
35	1	U7	M95040	ST Micro	M95040-WMN6P	
36	2	U8,U9	SN65220	TI	SN65220DBVT	296-9694-1-ND
37	1	U10	Si8051F340	Silicon Labs	C8051F340-GQ	
38	1	U11	DS2411	Maxim/Dallas	DS2411P	
39	1	U12	74LCX541	Fairchild	74LCX541MTC_NL	TC74LCX541FTFCT-ND
40	1	U13	Si530_PECL	Silabs	530AC114M285DG	
40	1	U13 alternate*	Si530_CML	Silabs	530HB121M109DG	
41	1	U16	FAN1540B	Fairchild	FAN1540B	FAN1540MPXCT-ND

***Note:** The alternate Si530 cannot be used without changing the EVB configuration. Contact Silicon Labs for details.

10. Si5326-VTSS-EVB Layout

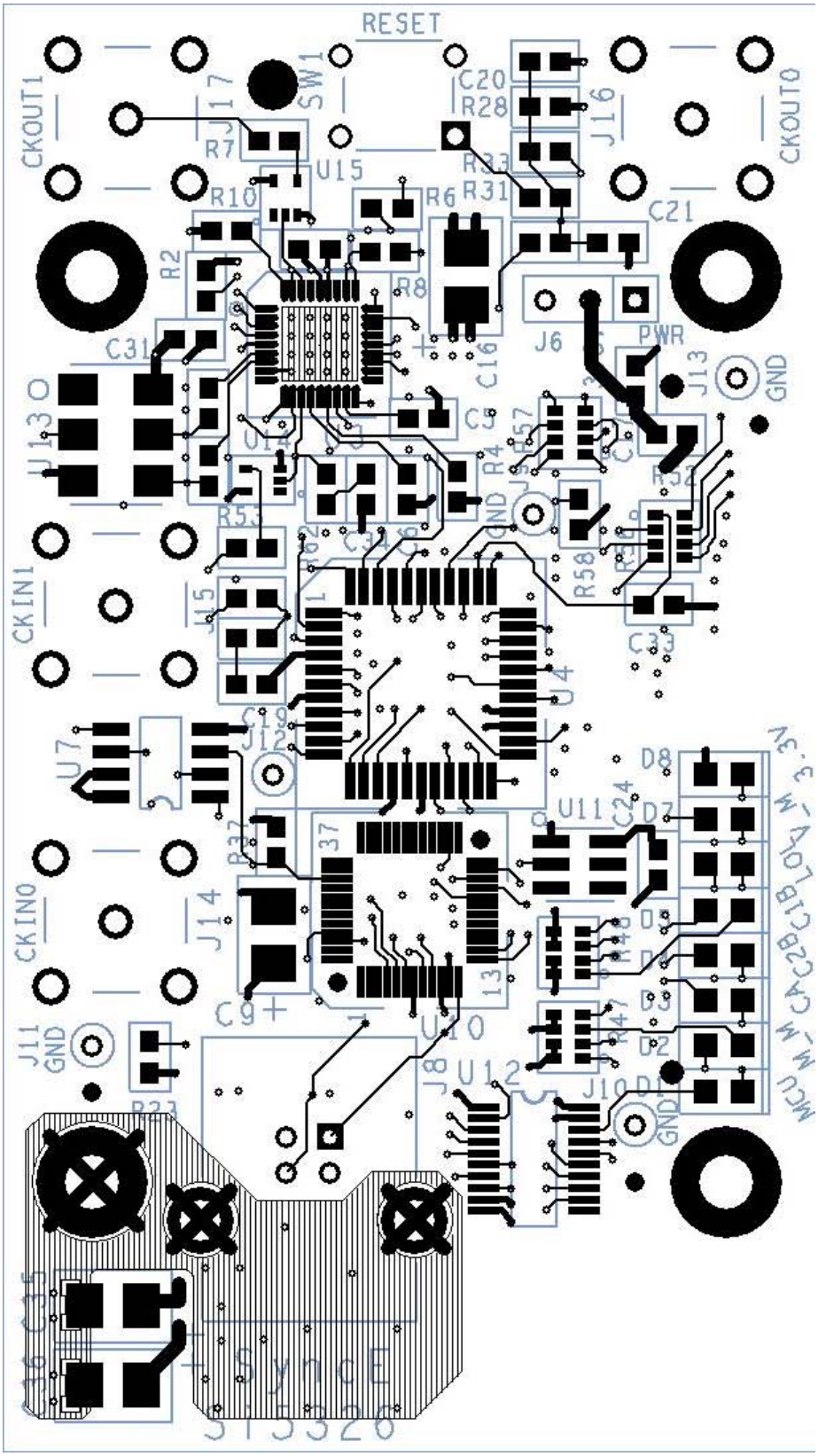

Figure 10. Top Layer

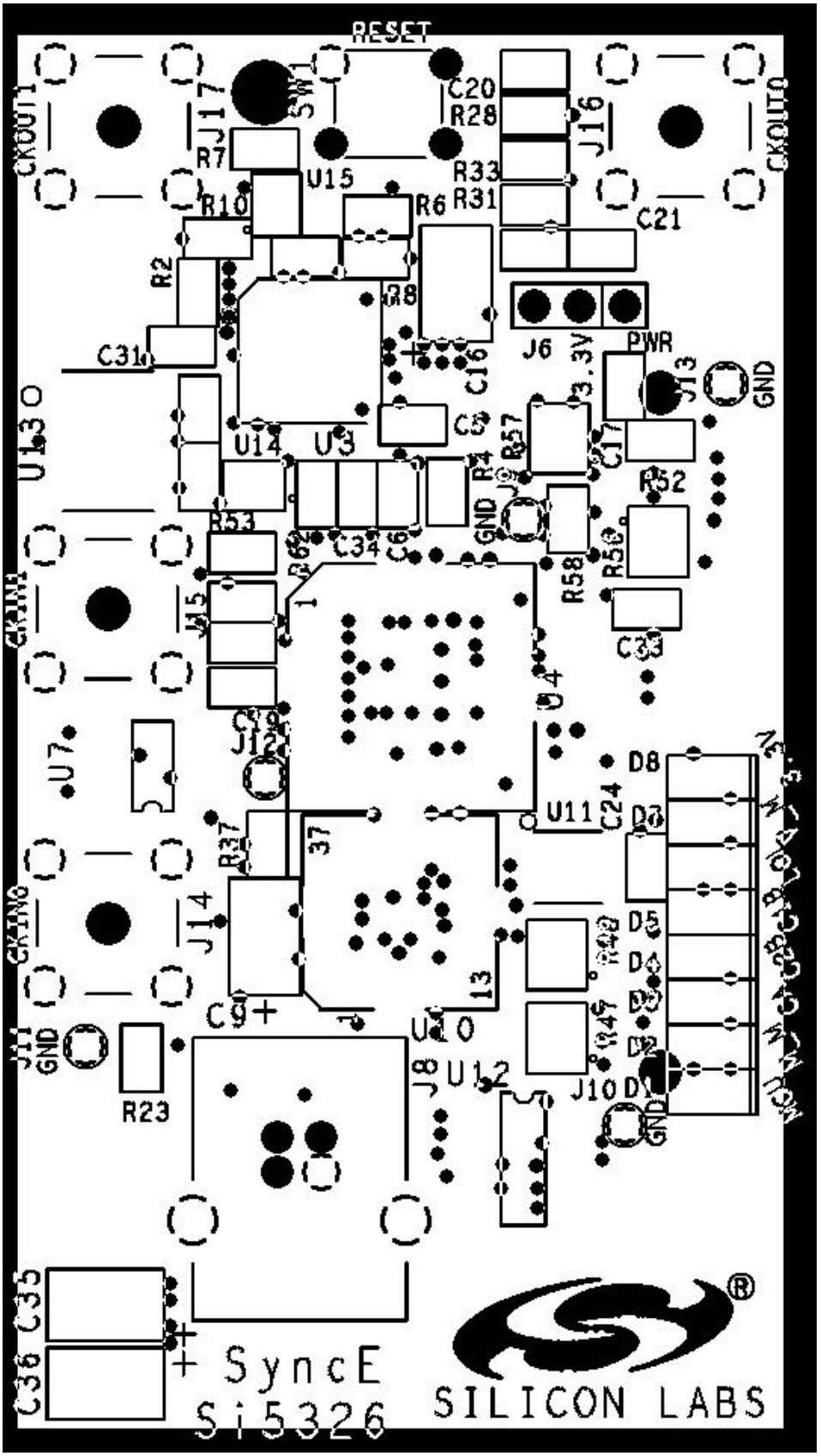

Figure 11. Ground Layer

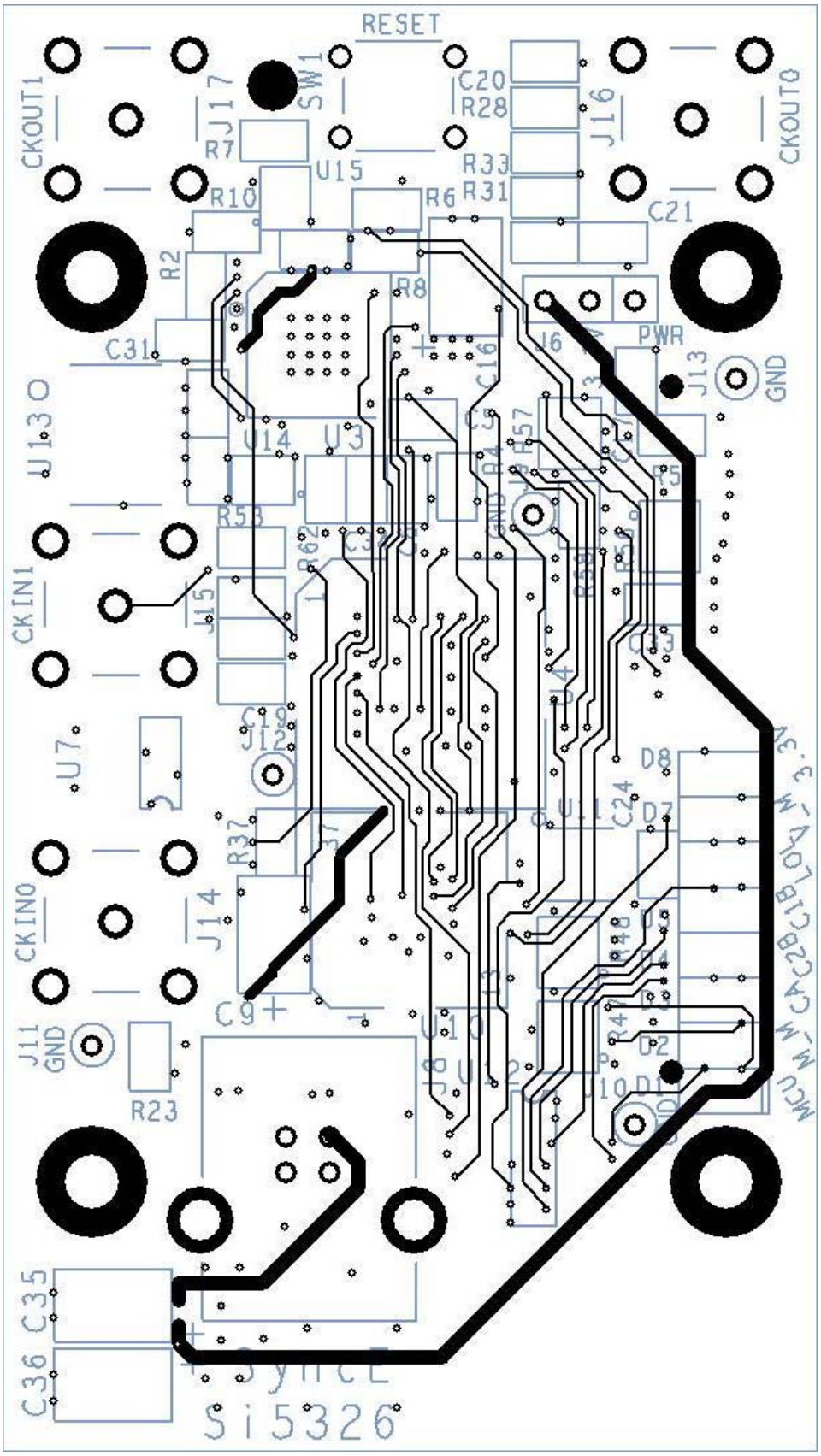

Figure 12. Signal Layer (1 of 2)

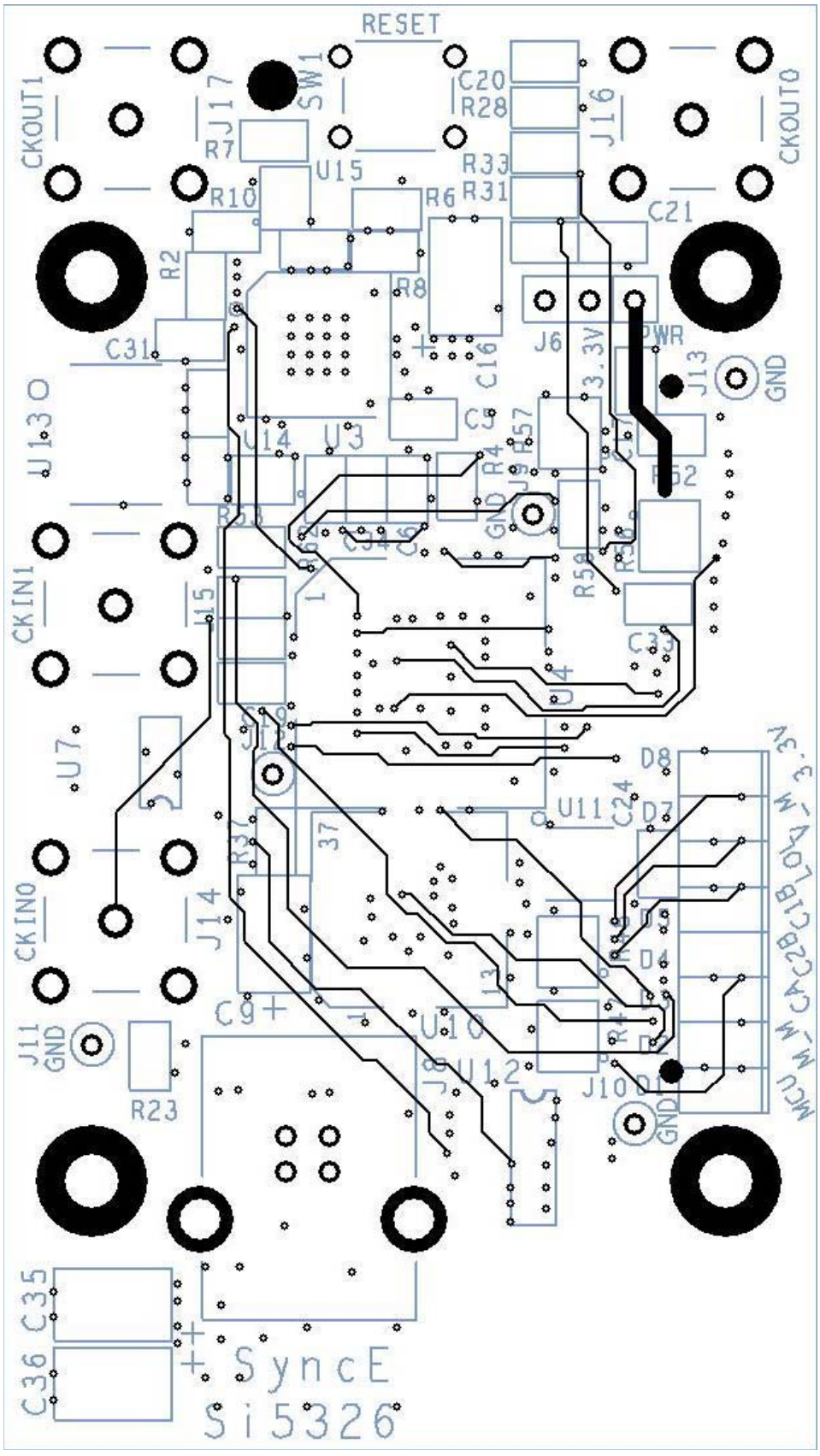

Figure 13. Signal Layer (2 of 2)

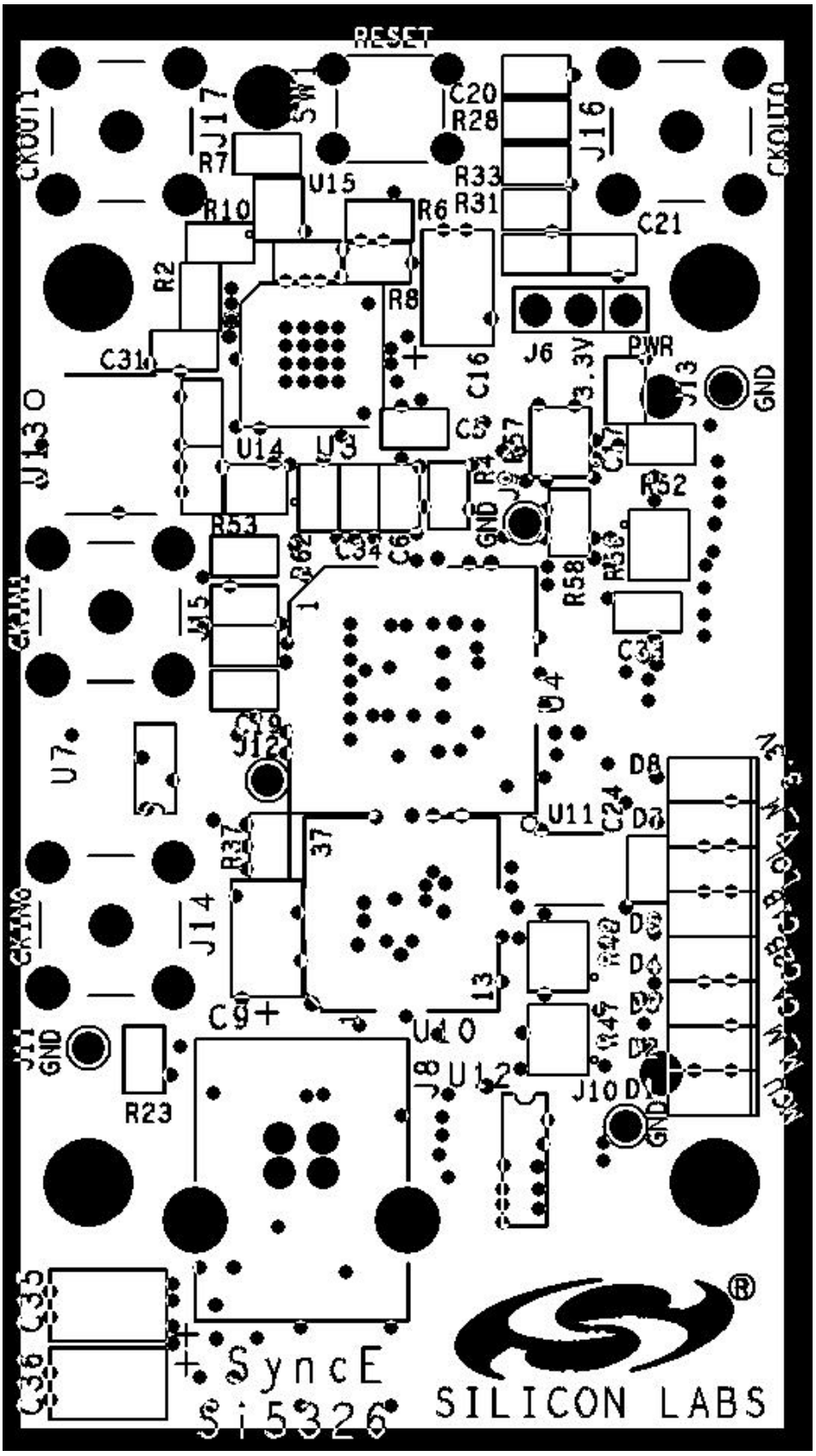

Figure 14. Power Layer

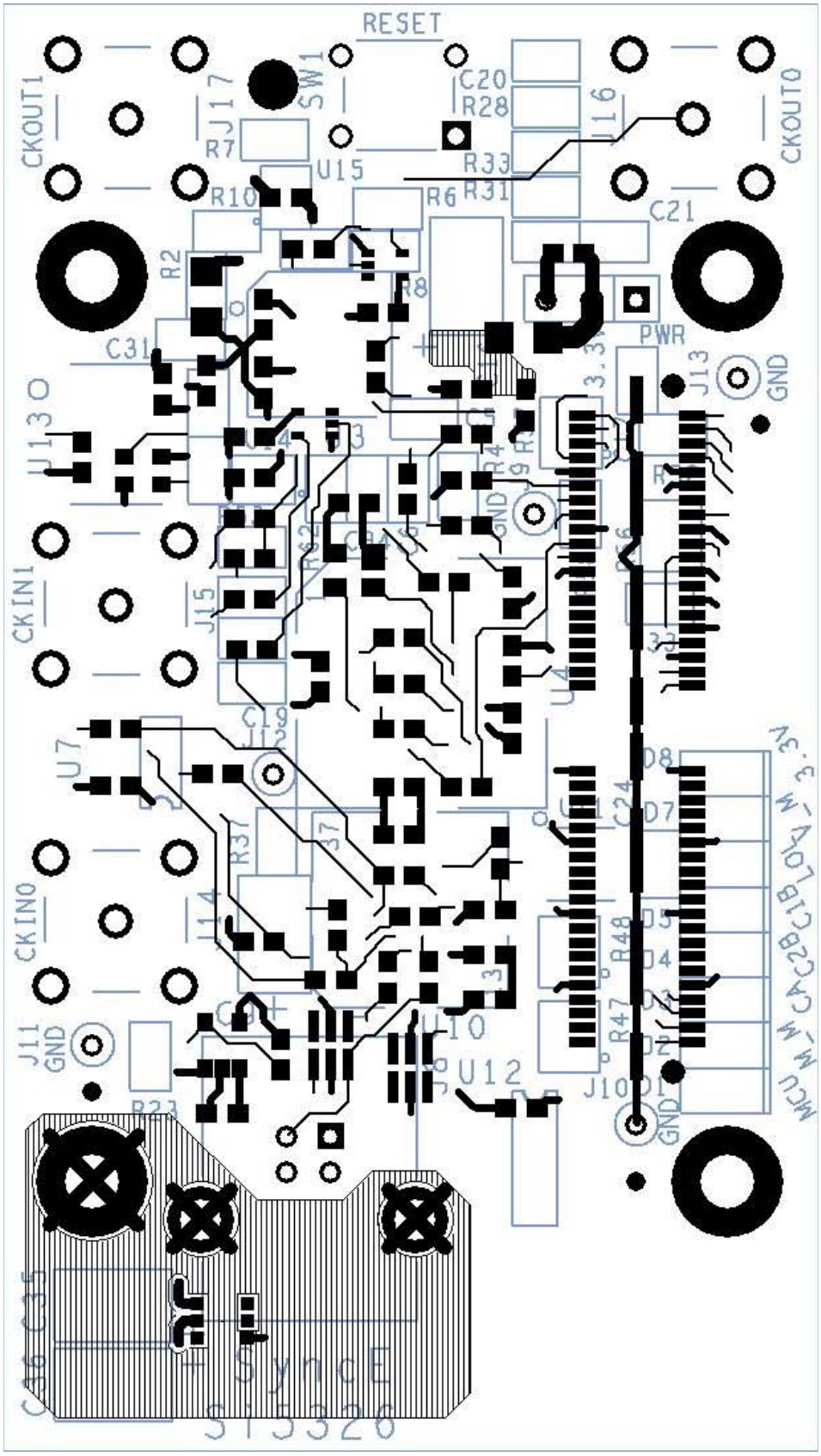

Figure 15. Bottom Layer

APPENDIX A—POWERUP AND FACTORY DEFAULT SETTINGS

The Si5326-VTSS-EVB power-up frequency plan is as follows:
Si5326 Frequency Plan

CKIN Frequencies (MHz)
CKIN1: 125.000000
CKIN2: 114.281820

Input Clock Multiplcation Ratios
CKIN2 to CKIN1: 5714091/6250000

fosc: 5.000000 GHz

Output Clock Multiplication Ratios
CKOUT1 to CKIN1: 1/1

CKOUT Frequencies (MHz)
CKOUT1: 125.000000

PLL Divider Settings
(Note: These are not binary register values.)
N1_HS: 10
NC1_LS: 4

N2_HS: 11
N2_LS: 3520

N31: 968
N32: 885

f3: 0.129132 MHz

Free Run Mode Enabled (FREE_RUN_EN = 1)
XA-XB Frequency: 114.285000 MHz

Available Loop Bandwidths using BWSEL (kHz)
0.06 (BWSEL_REG = 7)
0.12 (BWSEL_REG = 6)
0.24 (BWSEL_REG = 5)
0.49 (BWSEL_REG = 4)
0.98 (BWSEL_REG = 3)

2.02 (BWSEL_REG = 2)
4.28 (BWSEL_REG = 1)

Input Frequency Operating Range (MHz)

CKIN1 Min: 121.250000 Max: 141.750000
CKIN2 Min: 110.853564 Max: 129.595816

Output Frequency Operating Range (MHz)

CKOUT1 Min: 121.250000 Max: 141.750000

Phase Offset Resolution for Independent Skew:

2.0000 ns

Free Run Mode Details:

Actual CKOUT1: 125.003254 MHz
Error between Actual and Desired CKOUT1: 26.032000 ppm
Actual CKOUT1/XA-XB Frequency Ratio: 1.093785

Si5326-VTSS-EVB Power Up Register Setup Description:

```
<?xml version="1.0" encoding="us-ascii" standalone="yes" ?>
- <!-- Note: Do not edit the first line or type above it. -->
- <!-- Created on: Thursday, March 27, 2008 2:59 PM -->
- <settings version="2" chipType="Si5326">
- <!-- pin-based controls -->
  <entry name="RSTb" data="1" />
  <entry name="CMODE" data="1" />
  <entry name="RATE" data="MM" />
- <!-- register-based controls -->
  <entry name="FREE_RUN_EN" data="1" />
  <entry name="CKOUT_ALWAYS_ON" data="0" />
  <entry name="BYPASS_REG" data="0" />
  <entry name="FXDLY" data="0" />
  <entry name="CK_PRIOR2" data="1" />
  <entry name="CK_PRIOR1" data="0" />
  <entry name="CKSEL_REG" data="0" />
  <entry name="DHOLD" data="0" />
  <entry name="SQ_ICAL" data="0" />
  <entry name="BWSEL_REG" data="7" />
  <entry name="AUTOSEL_REG" data="2" />
  <entry name="HIST_DEL" data="12" />
  <entry name="ICMOS" data="3" />
  <entry name="SLEEP" data="0" />
  <entry name="SFOUT2_REG" data="0" />
```

```
<entry name="SFOUT1_REG" data="2" />
<entry name="FOSREFSEL" data="2" />
<entry name="HLOG_2" data="0" />
<entry name="HLOG_1" data="0" />
<entry name="HIST_AVG" data="18" />
<entry name="DSBL2_REG" data="1" />
<entry name="DSBL1_REG" data="0" />
<entry name="PD_CK2" data="0" />
<entry name="PD_CK1" data="0" />
<entry name="CLAT" data="0" />
<entry name="FLAT" data="0" />
<entry name="FLAT_VALID" data="1" />
<entry name="FOS_EN" data="0" />
<entry name="FOS_THR" data="1" />
<entry name="VALTIME" data="1" />
<entry name="LOCKT" data="4" />
<entry name="CK2_BAD_PIN" data="1" />
<entry name="CK1_BAD_PIN" data="1" />
<entry name="LOL_PIN" data="1" />
<entry name="INT_PIN" data="0" />
<entry name="INCDEC_PIN" data="1" />
<entry name="CK1_ACTV_PIN" data="1" />
<entry name="CKSEL_PIN" data="1" />
<entry name="CK_ACTV_POL" data="1" />
<entry name="CK_BAD_POL" data="1" />
<entry name="LOL_POL" data="1" />
<entry name="INT_POL" data="1" />
<entry name="LOS2_MSK" data="1" />
<entry name="LOS1_MSK" data="1" />
<entry name="LOSX_MSK" data="1" />
<entry name="FOS2_MSK" data="1" />
<entry name="FOS1_MSK" data="1" />
<entry name="LOL_MSK" data="1" />
<entry name="NC1_HS" data="6" />
<entry name="NC1_LS" data="3" />
<entry name="NC2_LS" data="1" />
<entry name="N2_LS" data="DBF" />
<entry name="N2_HS" data="7" />
<entry name="N31" data="3C7" />
<entry name="N32" data="374" />
<entry name="CLKIN2RATE" data="0" />
<entry name="CLKIN1RATE" data="0" />
<entry name="LOS1_EN" data="3" />
```

```
  <entry name="LOS2_EN" data="3" />
  <entry name="FOS1_EN" data="1" />
  <entry name="FOS2_EN" data="1" />
  <entry name="INDEPENDENTSKEW1" data="0" />
  <entry name="INDEPENDENTSKEW2" data="0" />
- <!-- Run the ICAL to start the internal self-calibration after the new settings are
loaded. -->
  <entry name="ICAL" data="1" />
  </settings>
```

APPENDIX B—APPLICATION BOARD DESIGN EXAMPLE

The purpose of this appendix is to provide guidance to users attempting to use the Si5326-VTSS-EVB as an example for designing an application board with a Vitesse VSCxxxxEV and an Si5326.

One issue that needs to be considered is startup and initialization. The Si5326-VTSS-EVB supplies the clock to the VSCxxxxEV board, and the VSCxxxxEV can then be used to program the Si5326-VTSS-EVB for different options and frequency plans. As shown in Figure 4, “Si5326-VTSS-EVB Block Diagram,” on page 5, the Si5326-VTSS-EVB has an MCU that loads the Si5326 at power up so that the Si5326 can provide a clock to the VSCxxxxEV device. If the MCU were to be removed, there would be a problem because the Si5326 cannot generate a clock until it has been programmed, and the VSCxxxxEV cannot load the Si5326 until it gets a clock. This means that all designs must load the Si5324 from some other source, such as an MCU or FPGA. Once the Si5326 has been initialized, the VSCxxxxEV can be used to change the Si5326's programming.

The other source that loads the Si5326 can be an MCU, a CPLD, or some other similar device. Though the Si5326-VTSS-EVB uses SPI as its serial port, I^2C can also be used, and the same concepts would apply. For further information on how a small and inexpensive MCU can be dedicated to this task, see “AN428: Jump-Start: In-System, Flash-Based Programming for Silicon Labs’ Timing Products”.

The Si5326-VTSS-EVB uses an Si530 as its XAXB reference source because drift during holdover may be an issue in some applications. Crystals with a total drift of 20 ppm or less are available, which may be acceptable in some applications. For a list of qualified crystals, see “AN591: Crystal Selection for the Si5315, Si5317, and other Si53xx Any-Frequency Jitter Attenuating Clocks”, which can be downloaded from www.silabs.com.

Most applications will have no need to implement a USB interface. In these cases, the serial number device is not needed. The EEPROM contents contain the power-up Si5326 register map. However, most applications will choose to put this information into the flash of the EEPROM.

Care must be taken so that the VSCxxxxEV is held in reset until after the output of the Si5326 is available and stable. This manual provides a description of one way that this can be implemented with a CPLD. To assist, the CPLD source code files are provided below.

```
`timescale 1ns / 100ps
//////////////////////////////////////////////////////////////////
/////////////////
// Create Date:    16 May 08
// Design Name:
// Module Name:    CPLD for the Vitesse SyncE Add On Board
// Description:    Mar 08 initial release
// Revision: Rev 1
// Revision 26 Mar 08 - initial release
//          16 May 08 - added force so that subsequent LOL's do
not issue reset
//                    - added IRQ; a simple open drain buffer
// Additional Comments:
//////////////////////////////////////////////////////////////////
/////////////////
module MCU_CPLD
(            // inputs from the MCU:
 mcu_mosi, Addr, mcu_ss_n, mcu_sclk, cpld_rst_n,
             // inputs from DUT:
 lol, dut_sdo, irq_in,
             // inputs from SyncE:
 v_spi_en_n, v_spi_clk, v_spi_mosi,
                        // misc inputs:
 rst_from_max811_n,
             // outputs to MCU:
 mcu_miso,
                        // outputs to DUT:
 dut_sdi, dut_sclk, dut_ss_n, dut_rst_n,
                        // outputs to SyncE:
 late_reset_n, v_spi_miso, v_irq_out_n,
                        // misc outputs:
 v_master, mcu_master, to_max811_n, flop_not
);
input mcu_mosi, mcu_ss_n, mcu_sclk, cpld_rst_n, lol, dut_sdo,
v_spi_en_n, irq_in,
      v_spi_clk, v_spi_mosi, rst_from_max811_n;
input [2:0] Addr;
output mcu_miso, dut_sdi, dut_sclk, dut_ss_n, dut_rst_n,
late_reset_n, v_spi_miso,
       v_irq_out_n, v_master, mcu_master, to_max811_n, flop_not;

 // internal stuff:
 wire   mcu_ss;               // positive true version of
mcu_ss_n
 assign mcu_ss = ~mcu_ss_n;
 wire v_spi_en;               // positive true version of
v_spi_en_n
 assign v_spi_en = ~v_spi_en_n;

 wire flop;            // create an RS flip flop that gates away
LOL from the
 wire flop_not;        // reset logic after the power up sequenc
```

```
has completed.
 wire cpld_rst;        // create a positive true version of
cpld_rst_n
 assign cpld_rst = ~cpld_rst_n;
 assign flop     = ~(cpld_rst | flop_not);
 assign flop_not = ~(rst_from_max811_n | flop);

 // first do the interrupt request from the DUT to the main
board:
 // invert the signal and make it open drain
 assign v_irq_out_n = (irq_in) ? 0'b0 : 1'bz;

 // do the reset and delayed reset functions:
 // pass thru the reset from the DUT.
 assign dut_rst_n = cpld_rst_n;

 // OR LOL with cpld_rst whenever cpld_rst is active
 // after cpld_rst is negated, gate away LOL so it can cause a
reset to the MAX811
 assign to_max811_n = ~(cpld_rst | (lol & flop_not));

 assign late_reset_n = (rst_from_max811_n) ? 1'bz : 1'b0;  //
open collector

 // mux the two SPI busses to the DUT:
 assign dut_ss_n = (Addr == 0)             ? mcu_ss_n :
v_spi_en_n;
 assign dut_sdi  = ((Addr == 0) && mcu_ss) ? mcu_mosi :
v_spi_mosi;
 assign dut_sclk = ((Addr == 0) && mcu_ss) ? mcu_sclk :
v_spi_clk;
 assign v_spi_miso = (~mcu_ss && v_spi_en) ? dut_sdo : 1'bz;
 assign mcu_miso = ((Addr == 0) && mcu_ss) ? dut_sdo : 1'bz;

 assign mcu_master = mcu_ss;     // to an LED
 assign v_master   = v_spi_en;   // to an LED
endmodule
```

```
#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments
NET "Addr<0>"  LOC = "P36" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "Addr<1>"  LOC = "P37" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "Addr<2>"  LOC = "P38" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "cpld_rst_n"  LOC = "P30" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "dut_rst_n"  LOC = "P3" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "dut_sclk"  LOC = "P19" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "dut_sdi"  LOC = "P21" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "dut_sdo"  LOC = "P20" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "dut_ss_n"  LOC = "P23" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "flop_not"  LOC = "P39" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "irq_in"  LOC = "P44" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "late_reset_n"  LOC = "P29" | IOSTANDARD = LVCMOS33  | KEEPER
;
NET "lol"  LOC = "P22" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "mcu_master"  LOC = "P6" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "mcu_miso"  LOC = "P34" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "mcu_mosi"  LOC = "P33" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "mcu_sclk"  LOC = "P32" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "mcu_ss_n"  LOC = "P31" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "rst_from_max811_n"  LOC = "P28" | IOSTANDARD = LVCMOS33  |
KEEPER ;
NET "to_max811_n"  LOC = "P8" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "v_irq_out_n"  LOC = "P2" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "v_master"  LOC = "P27" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "v_spi_clk"  LOC = "P13" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "v_spi_en_n"  LOC = "P12" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "v_spi_miso"  LOC = "P16" | IOSTANDARD = LVCMOS33  | KEEPER ;
NET "v_spi_mosi"  LOC = "P14" | IOSTANDARD = LVCMOS33  | KEEPER ;

#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE
```

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Added new Vitesse EVBs.
- Added "Appendix B—Application Board Design Example" on page 26.
- Simplified "7.Installing Software for the Direct Control of the Si5326-VTSS-EVB" on page 10.
- Changed “any-rate” to “any-frequency” throughout.

NOTES:

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