

P-Channel 1.8-V (G-S) MOSFET

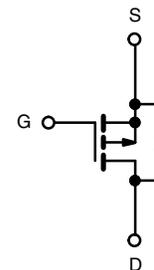
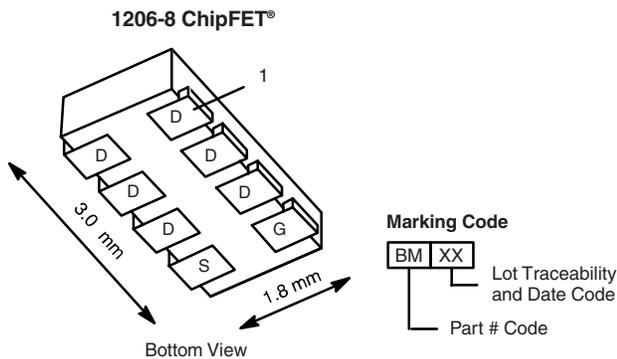
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 8	0.033 at $V_{GS} = - 4.5$ V	- 7.1	14
	0.043 at $V_{GS} = - 2.5$ V	- 6.2	
	0.060 at $V_{GS} = - 1.8$ V	- 5.3	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET



RoHS
COMPLIANT
HALOGEN
FREE
Available



P-Channel MOSFET

Ordering Information: Si5445BDC-T1-E3 (Lead (Pb)-free)
Si5445BDC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V_{DS}	- 8		V	
Gate-Source Voltage	V_{GS}	± 8			
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_A = 25$ °C	- 7.1	- 5.2	A
		$T_A = 85$ °C	- 5.2	- 3.7	
Pulsed Drain Current	I_{DM}	± 20			
Continuous Source Current ^a	I_S	- 2.1	- 1.1		
Maximum Power Dissipation ^a	P_D	$T_A = 25$ °C	2.5	1.3	W
		$T_A = 85$ °C	1.3	0.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 5$ s	45	50	°C/W
		Steady State	85	95	
Maximum Junction-to-Foot (Drain)	R_{thJF}	17	20		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.45		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -8\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -8\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -5.2\text{ A}$		0.027	0.033	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -4.5\text{ A}$		0.035	0.043	
		$V_{GS} = -1.8\text{ V}, I_D = -1.7\text{ A}$		0.050	0.060	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -5\text{ V}, I_D = -5.2\text{ A}$		18		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5.2\text{ A}$		14	21	nC
Gate-Source Charge	Q_{gs}		1.8			
Gate-Drain Charge	Q_{gd}		3.3			
Gate Resistance	R_g	$f = 1\text{ MHz}$		8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$		12	20	ns
Rise Time	t_r		22	35		
Turn-Off Delay Time	$t_{d(off)}$		75	115		
Fall Time	t_f		50	75		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		75	115	nC
Reverse Recovery Charge	Q_{rr}			40	60	

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted

