

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
- 20	0.022 at V _{GS} = - 4.5 V	- 12 ^a	20 nC
	0.029 at V _{GS} = - 2.5 V	- 12 ^a	
	0.041 at V _{GS} = - 1.8 V	- 12 ^a	

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- New thermally Enhanced PowerPAK[®] ChipFET[®] Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile

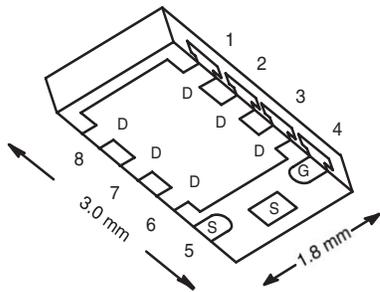


RoHS
COMPLIANT

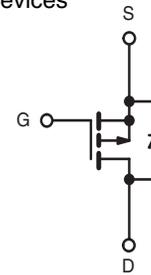
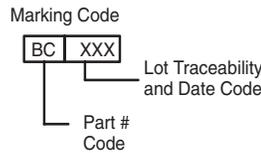
APPLICATIONS

- Load Switch, Battery Switch, PA Switch and Charger Switch for Portable Devices

PowerPAK ChipFET Single



Bottom View



Ordering Information: Si5481DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 12 ^a
		T _C = 70 °C	- 12 ^a
		T _A = 25 °C	- 9.7 ^{b, c}
		T _A = 70 °C	- 7.8 ^{b, c}
Pulsed Drain Current	I _{DM}	- 20	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	- 14.8
		T _A = 25 °C	- 2.6 ^{b, c}
Maximum Power Dissipation	P _D	T _C = 25 °C	17.8
		T _C = 70 °C	11.4
		T _A = 25 °C	3.1 ^{b, c}
		T _A = 70 °C	2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	
Soldering Recommendations (Peak Temperature) ^{d, e}		260	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	30	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.5	7	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W.



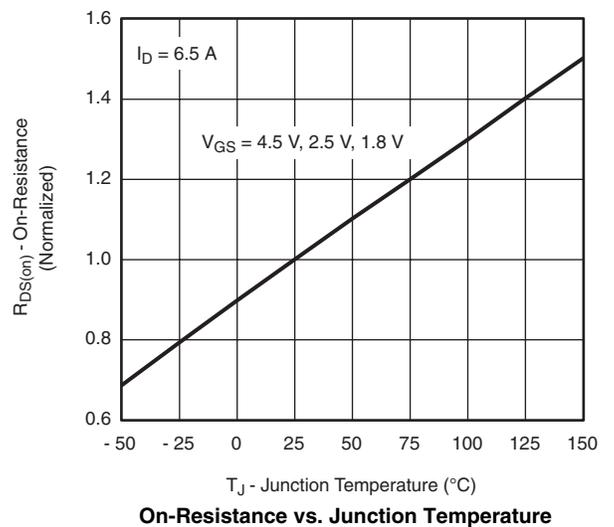
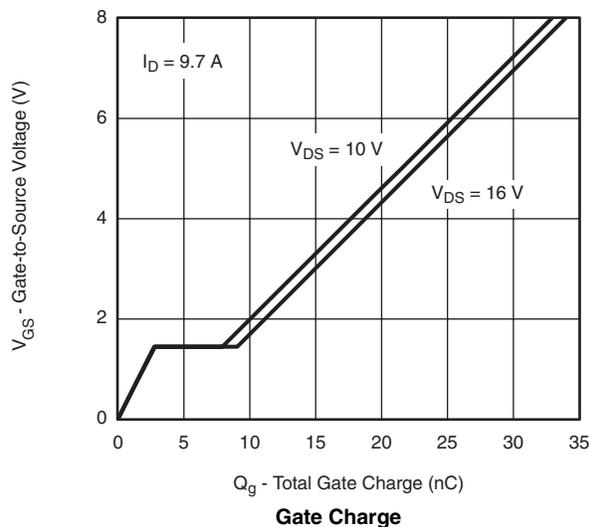
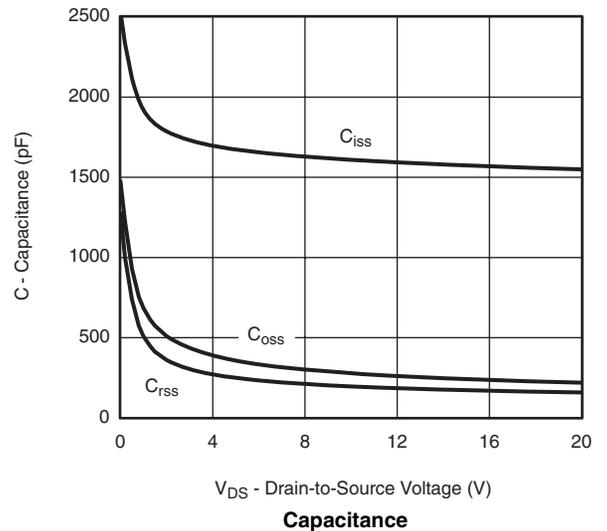
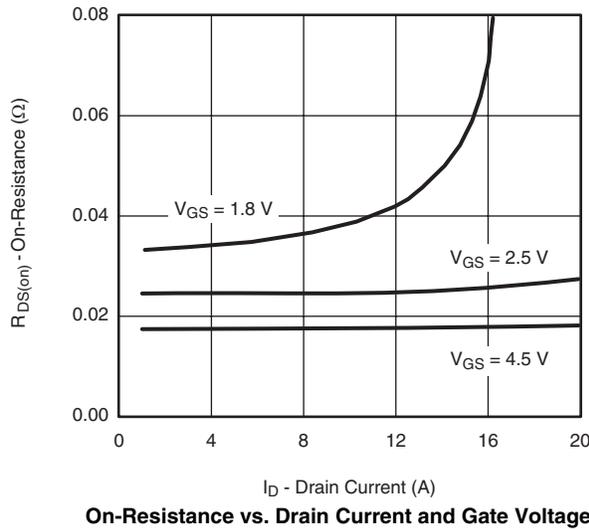
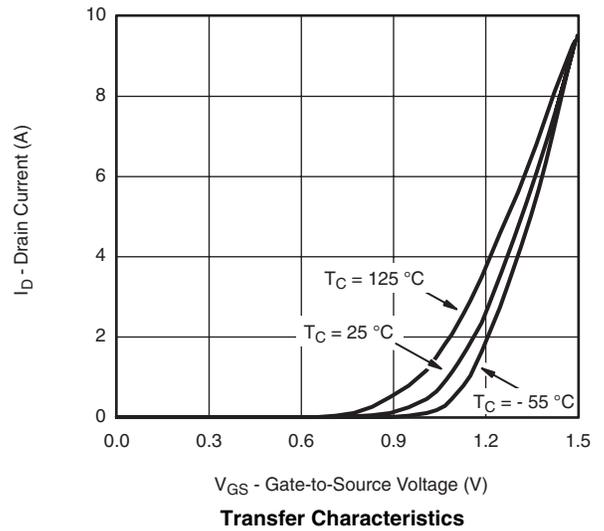
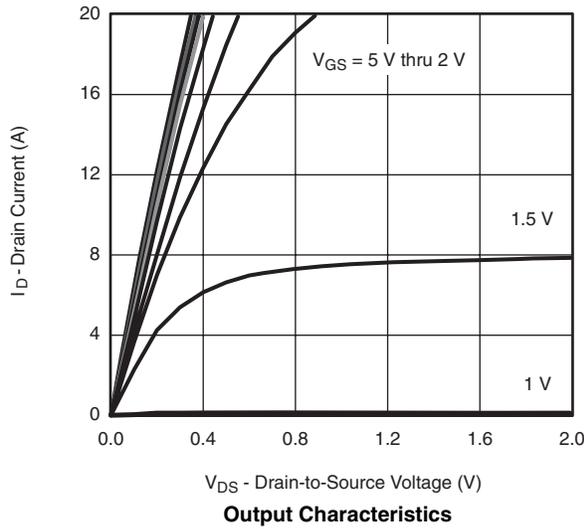
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-15.5		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = -4.5\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -6.5\text{ A}$		0.018	0.022	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -5.7\text{ A}$		0.024	0.029	
		$V_{GS} = -1.8\text{ V}, I_D = 2.4\text{ A}$		0.033	0.041	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -6.5\text{ A}$		25		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1610		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -9.7\text{ A}$		33	50	nC
				20	30	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -9.7\text{ A}$		2.8		
Gate-Drain Charge	Q_{gd}			5.1		
Gate Resistance	R_g	$f = 1\text{ MHz}$		8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong -7.8\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		13	20	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			90	135	
Fall Time	t_f			167	250	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.3\text{ }\Omega$ $I_D \cong -7.8\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		6	15	
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			90	135	
Fall Time	t_f			167	250	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-14.8	A
Pulse Diode Forward Current ^a	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = -7.8\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -7.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			17	30	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			16		

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

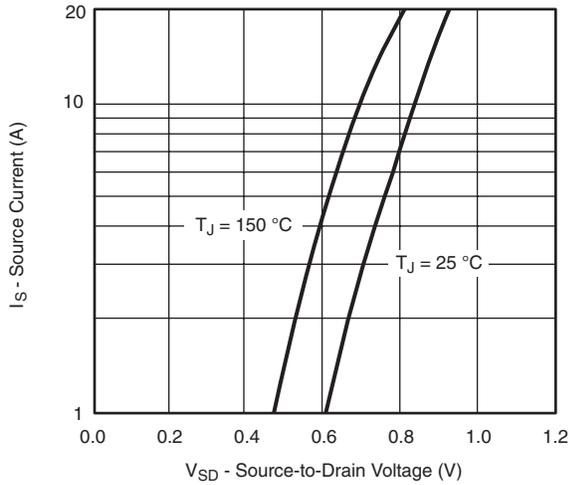
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted

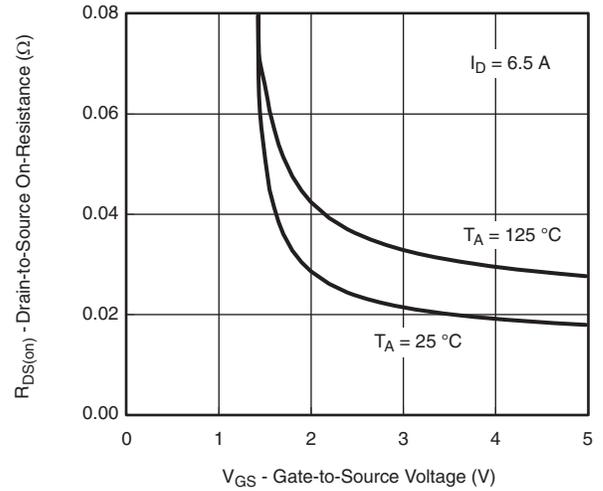




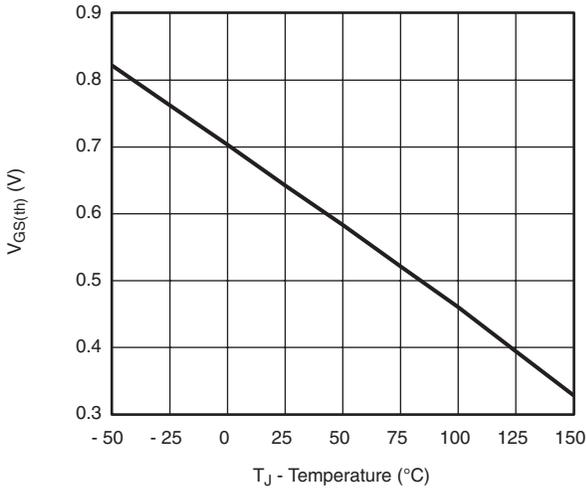
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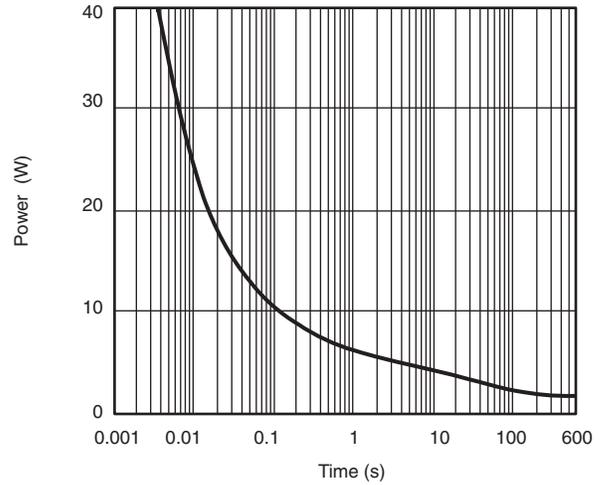
Source-Drain Diode Forward Voltage



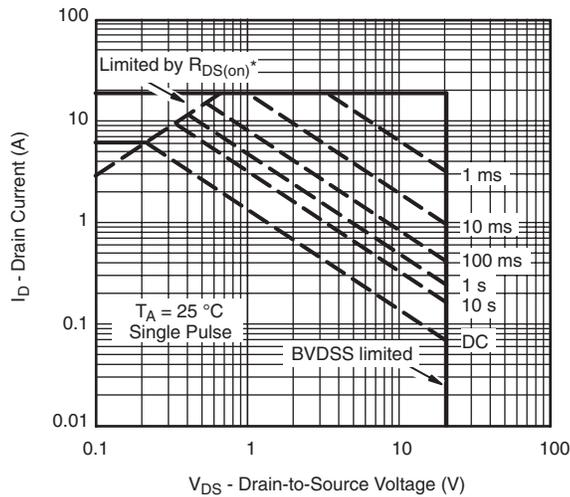
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

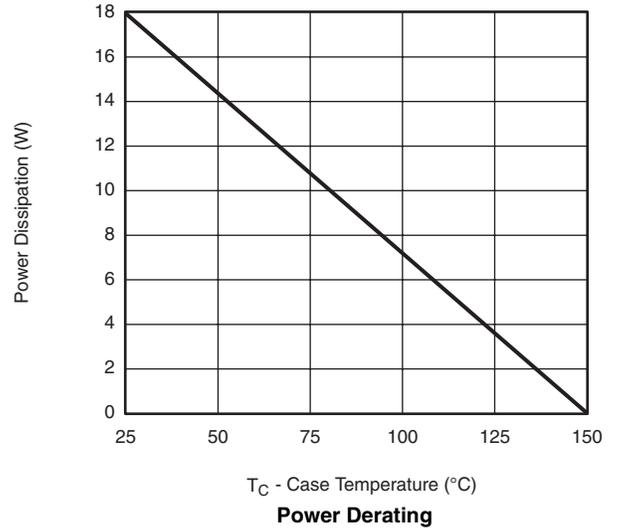
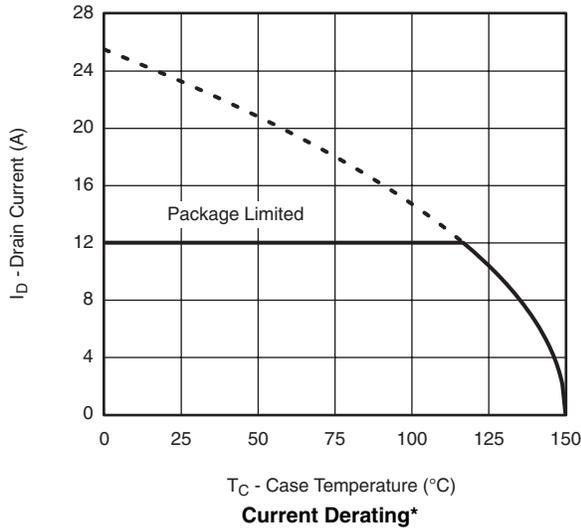


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



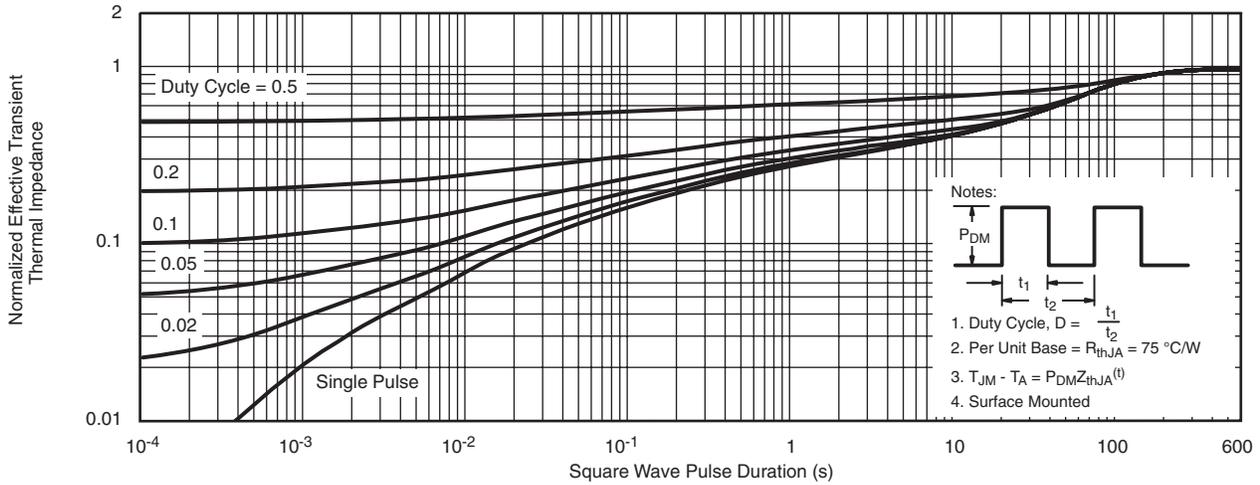
* The power dissipation P_D is based on $T_{J(\max)} = 150\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si5481DU

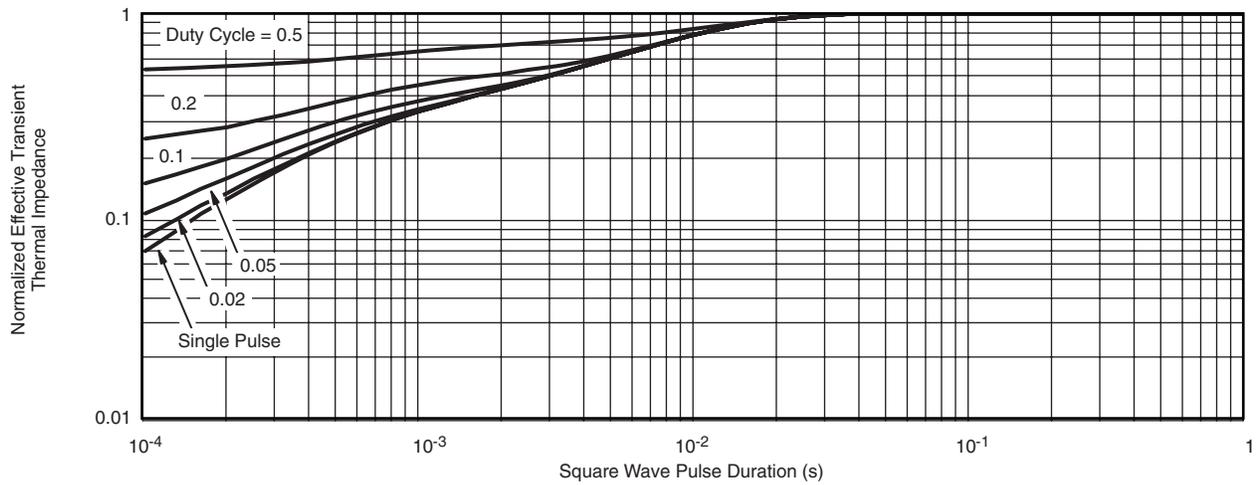
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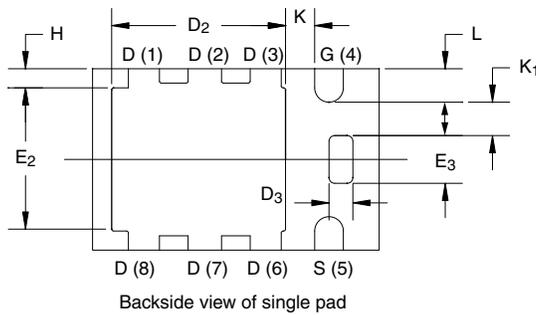
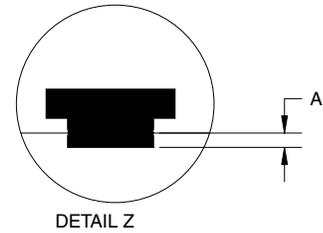
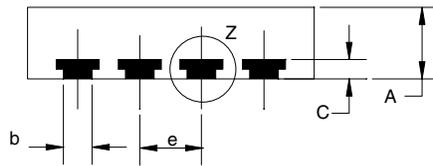
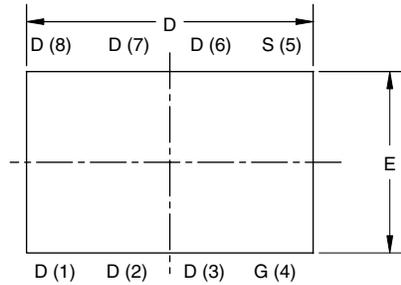
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

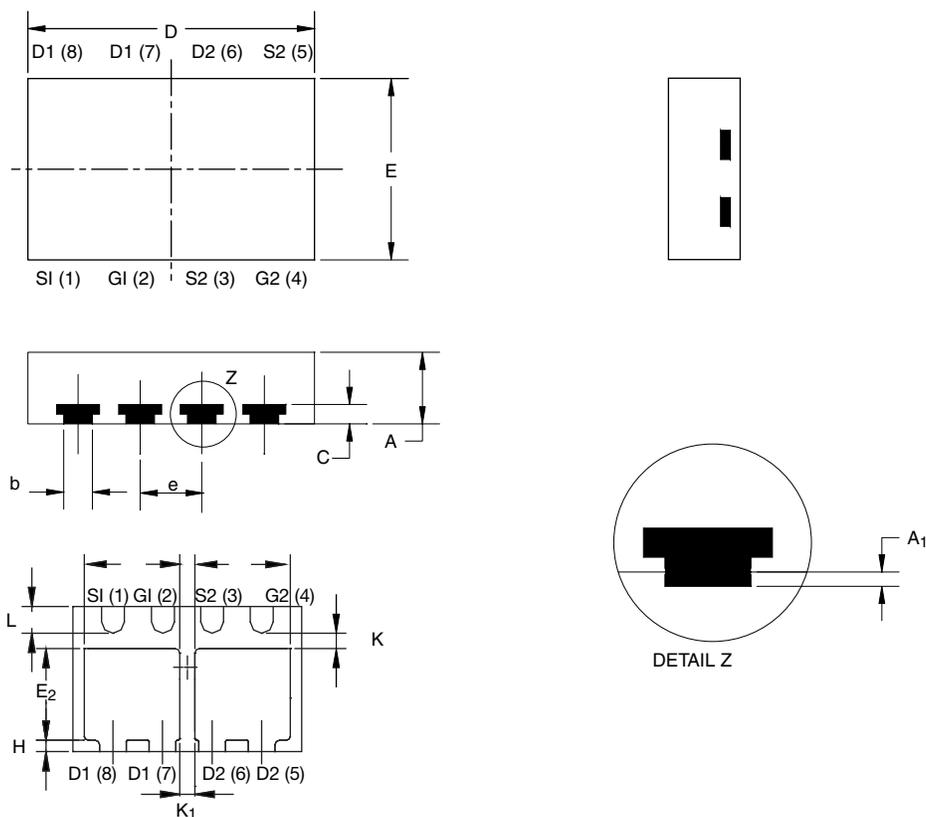
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73777>.

PowerPAK® ChipFET® SINGLE PAD



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.75	1.87	2.00	0.069	0.074	0.079
D ₃	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	1.38	1.50	1.63	0.054	0.059	0.064
E ₃	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K ₁	0.30	-	-	0.012	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

PowerPAK® ChipFET® DUAL PAD



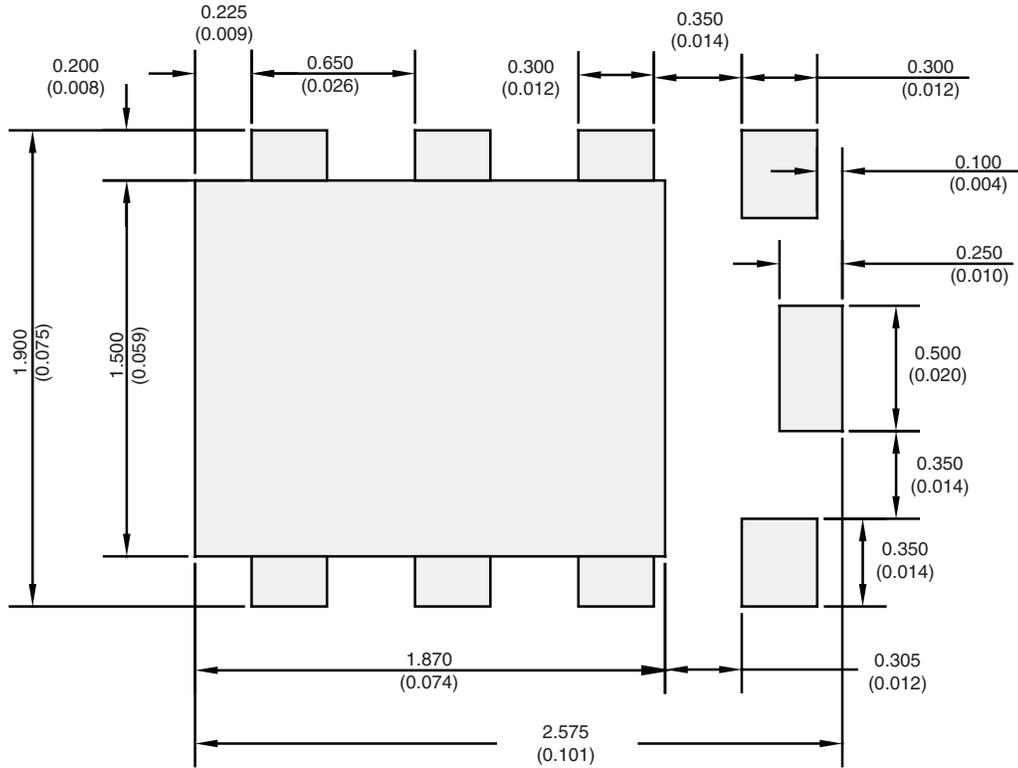
Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.07	1.20	1.32	0.042	0.047	0.052
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K ₁	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

ECN: C10-0618-Rev. C, 19-Jul-09

DWG: 5940

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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