

Complementary 20-V (D-S) MOSFET

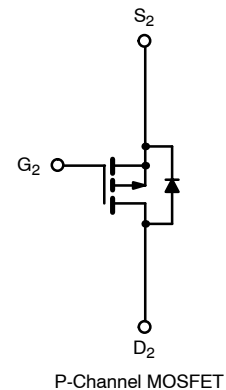
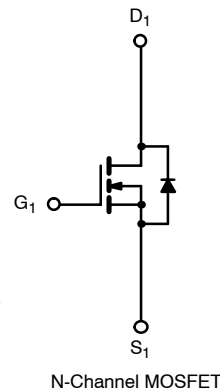
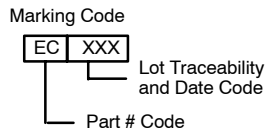
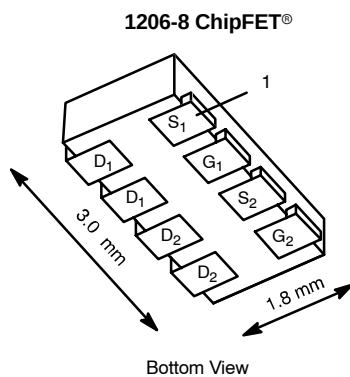
PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.040 @ $V_{GS} = 4.5$ V	5.9
		0.045 @ $V_{GS} = 2.5$ V	5.6
		0.052 @ $V_{GS} = 1.8$ V	5.2
P-Channel	-20	0.086 @ $V_{GS} = -4.5$ V	-4.1
		0.121 @ $V_{GS} = -2.5$ V	-3.4
		0.171 @ $V_{GS} = -1.8$ V	-2.9

FEATURES

- TrenchFET® Power MOSFETS
- Ultra Low $r_{DS(on)}$ and Excellent Power Handling In Compact Footprint

APPLICATIONS

- Load Switching for Portable Devices



Ordering Information: Si5515DC-T1—E3

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter		Symbol	N-Channel		P-Channel		Unit
			5 secs	Steady State	5 secs	Steady State	
Drain-Source Voltage		V _{DS}	20		-20		V
Gate-Source Voltage		V _{GS}	± 8				
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	5.9	4.4	-4.1	-3	A
	T _A = 85°C		4.2	3.1	-2.9	-2.2	
Pulsed Drain Current		I _{DM}	20		-15		
Continuous Source Current (Diode Conduction) ^a		I _S	1.8	0.9	-1.8	-0.9	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.1	1.1	2.1	1.1	W
	T _A = 85°C		1.1	0.6	1.1	0.6	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150				°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260				

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	50	60	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.4		1.0	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.4		-1.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V	N-Ch P-Ch			±100 ±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch			-1	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85°C	N-Ch			5	
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 85°C	P-Ch			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	20			A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-15			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.4 A	N-Ch		0.032	0.040	Ω
		V _{GS} = -4.5 V, I _D = -3.0 A	P-Ch		0.069	0.086	
		V _{GS} = 2.5 V, I _D = 4.1 A	N-Ch		0.036	0.045	
		V _{GS} = -2.5 V, I _D = -2.5 A	P-Ch		0.097	0.121	
		V _{GS} = 1.8 V, I _D = 1.9 A	N-Ch		0.042	0.052	
		V _{GS} = -1.8 V, I _D = -0.6 A	P-Ch		0.137	0.171	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.4 A	N-Ch		22		S
		V _{DS} = -10 V, I _D = -3 A	P-Ch		8		
Diode Forward Voltage ^a	V _{SD}	I _S = 0.9 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V
		I _S = -0.9 A, V _{GS} = 0 V	P-Ch		-0.8	-1.2	
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.4 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -3 A	N-Ch		5	7.5	nC
Gate-Source Charge	Q _{gs}		P-Ch		5.5	8.5	
			N-Ch		0.85		
Gate-Drain Charge	Q _{gd}		P-Ch		0.91		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	N-Ch		20	30	ns
			P-Ch		18	30	
Rise Time	t _r		N-Ch		36	55	
			P-Ch		32	50	
Turn-Off Delay Time	t _{d(off)}		N-Ch		30	45	
			P-Ch		42	65	
Fall Time	t _f		N-Ch		12	20	
			P-Ch		26	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.9 A, di/dt = 100 A/μs	N-Ch		45	90	
		I _F = -0.9 A, di/dt = 100 A/μs	P-Ch		30	60	

Notes

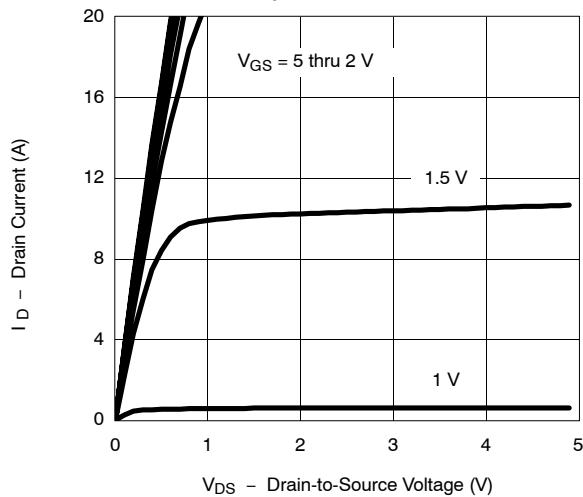
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%,
b. Guaranteed by design, not subject to production testing.



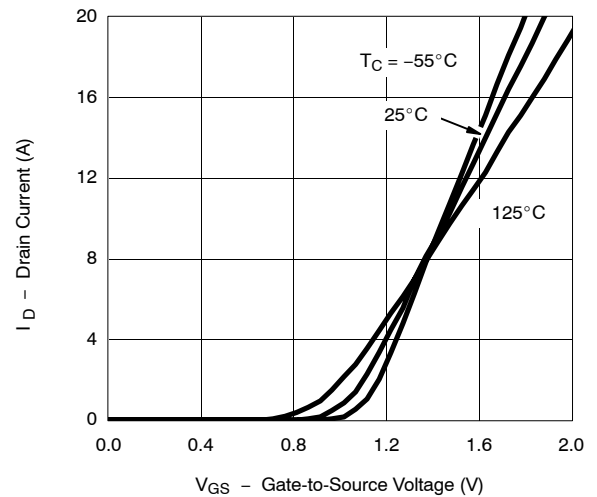
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL

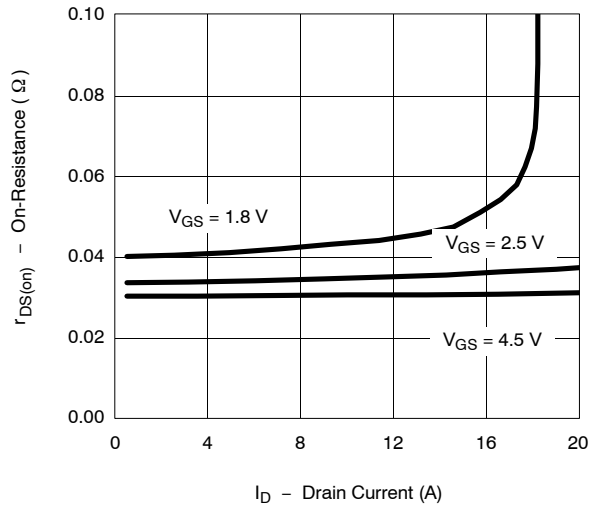
Output Characteristics



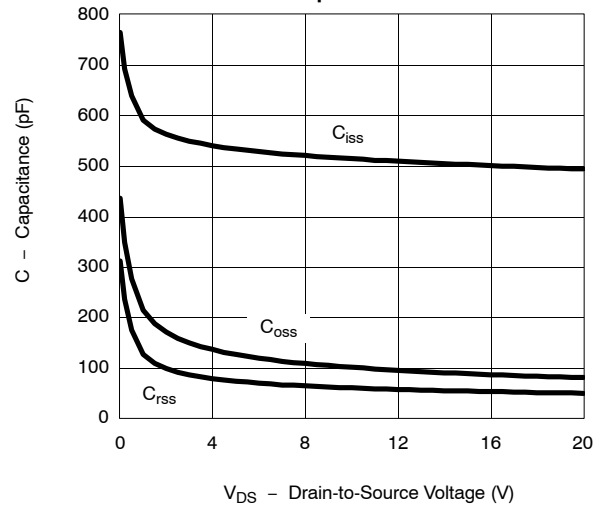
Transfer Characteristics



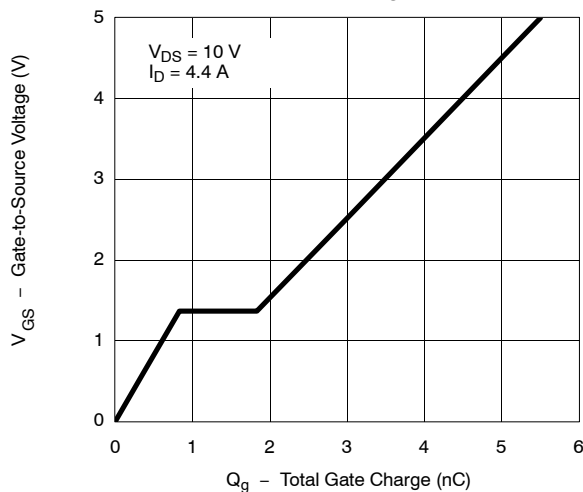
On-Resistance vs. Drain Current



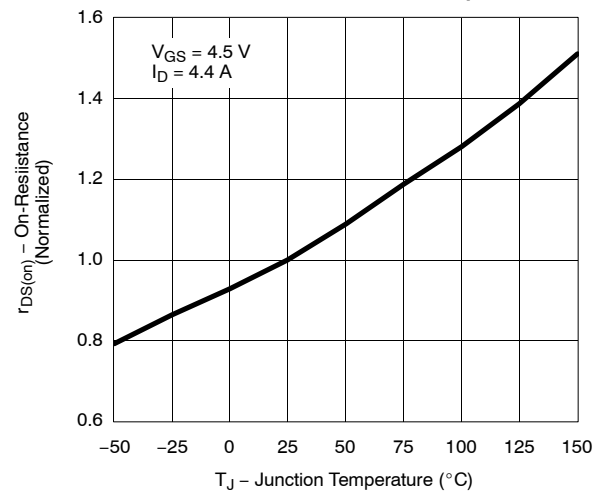
Capacitance



Gate Charge

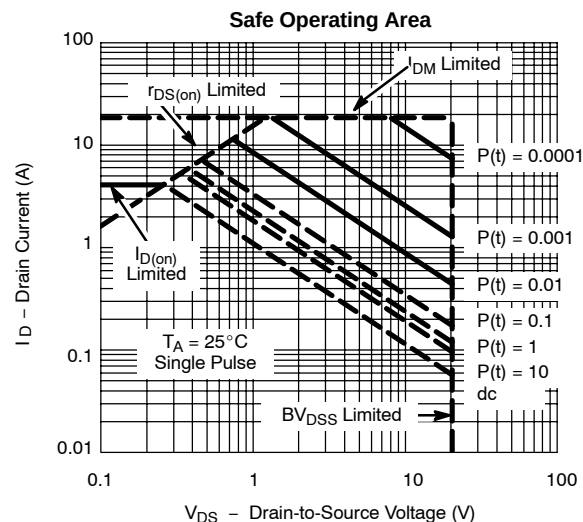
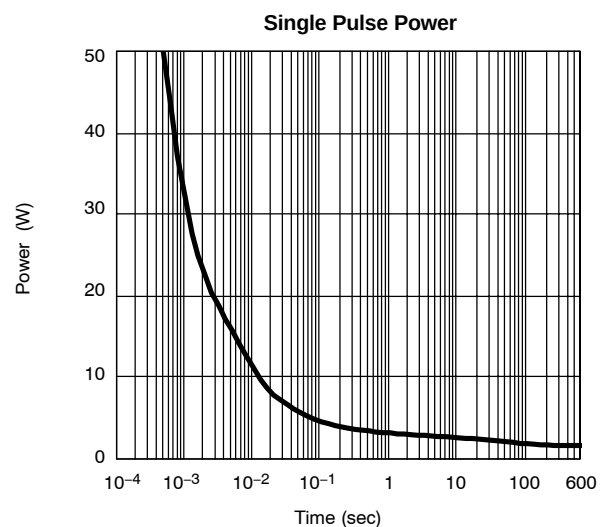
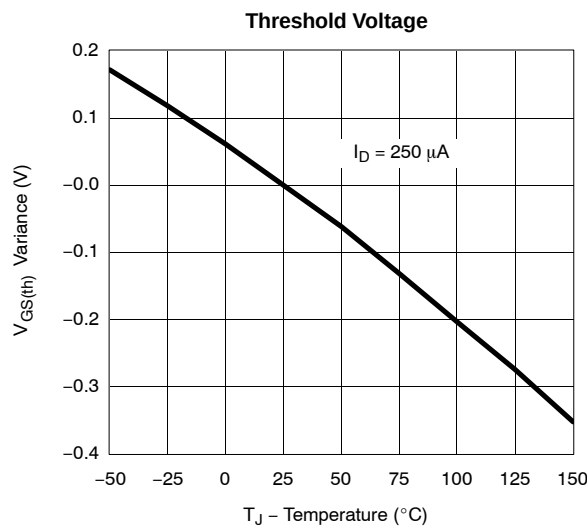
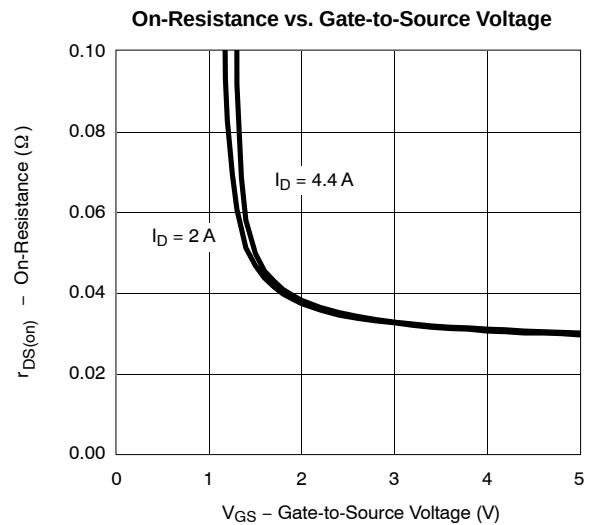
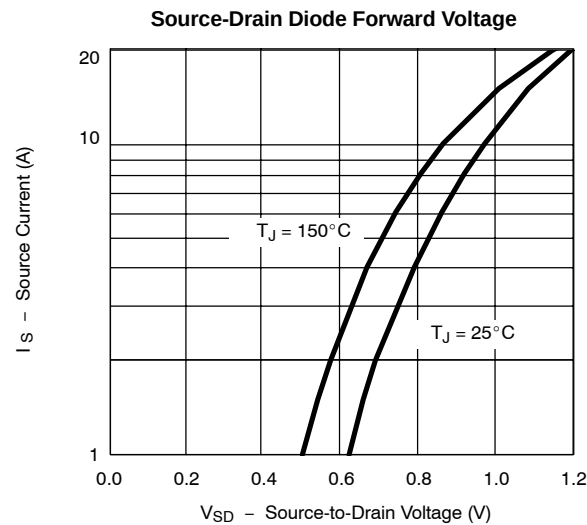


On-Resistance vs. Junction Temperature





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) **N-CHANNEL**

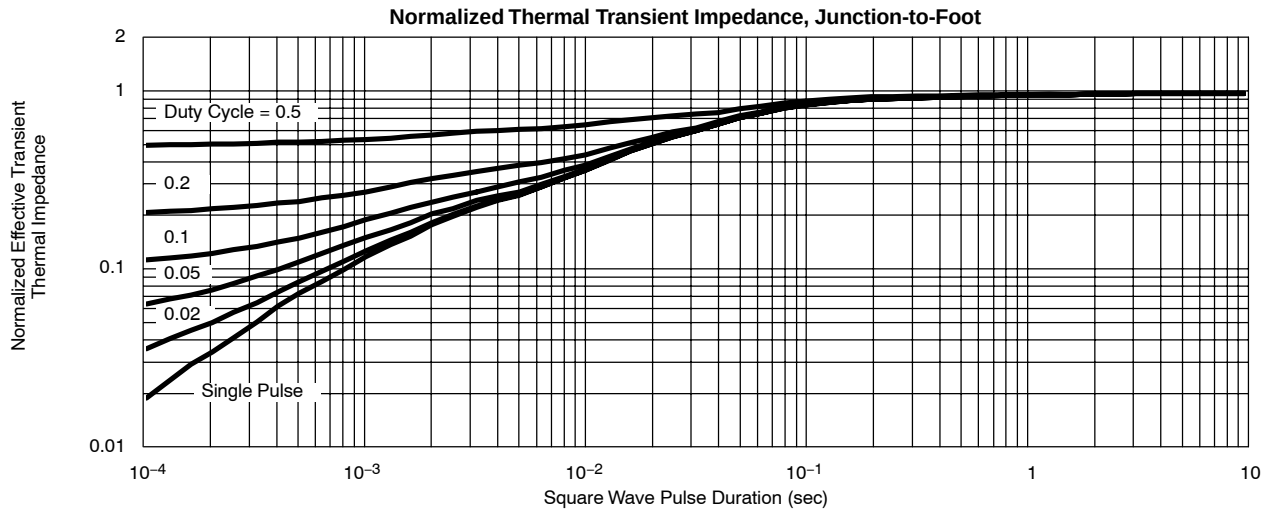
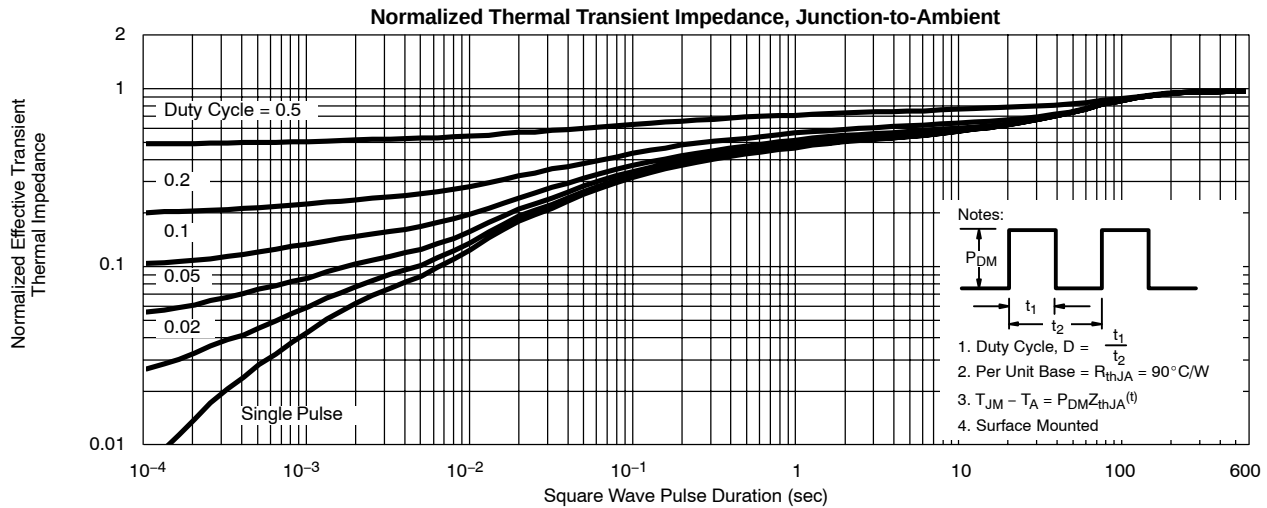


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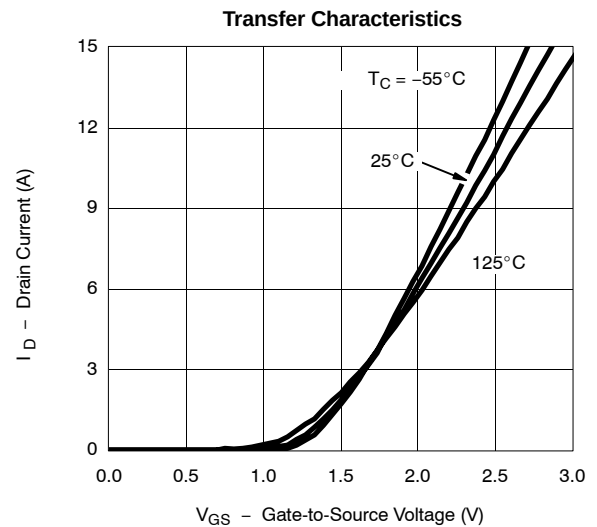
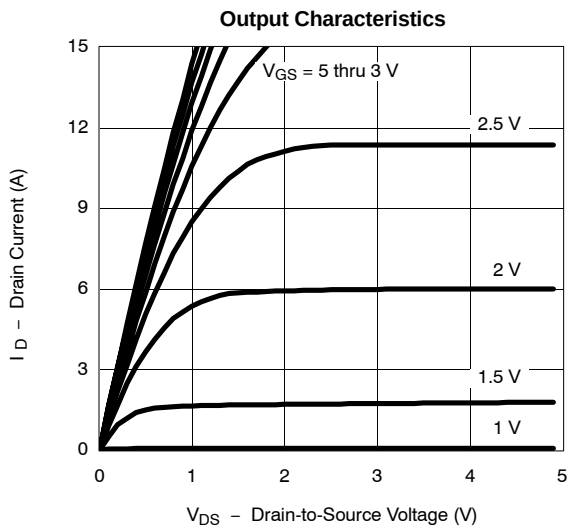
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



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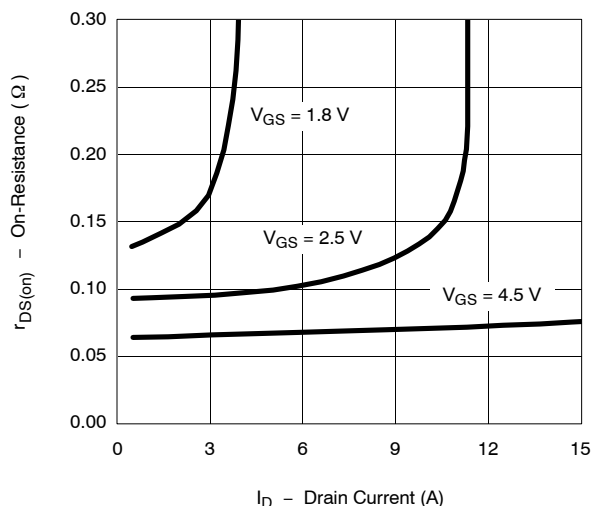
P-CHANNEL



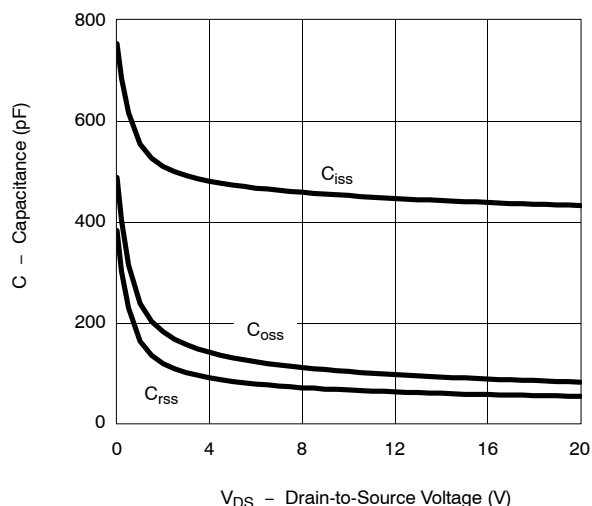
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL

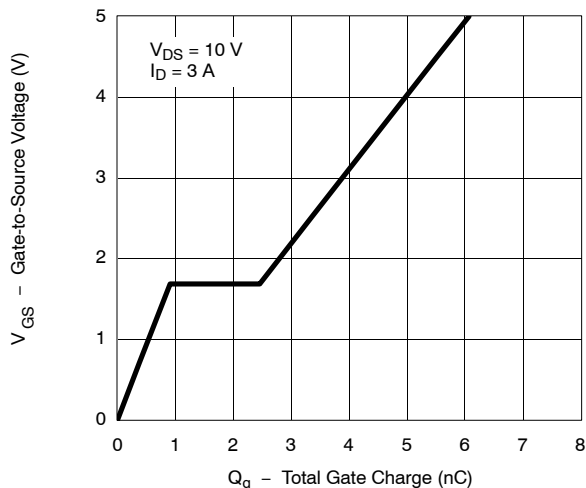
On-Resistance vs. Drain Current



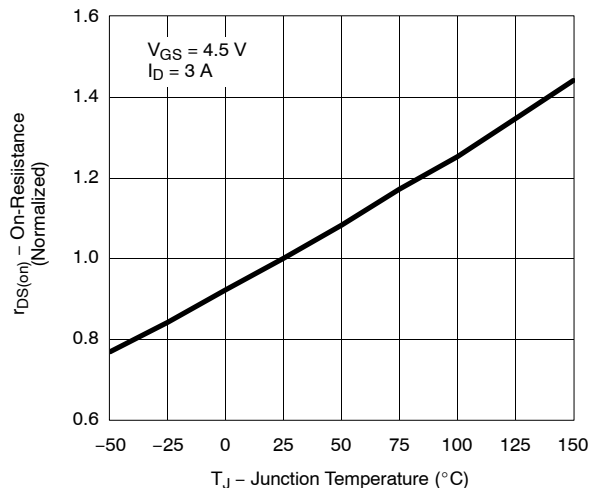
Capacitance



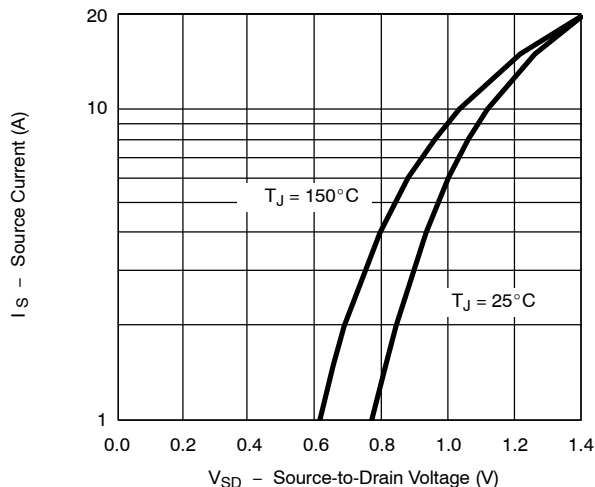
Gate Charge



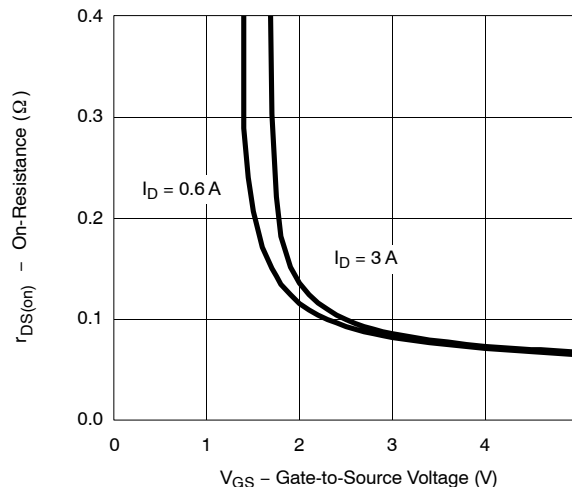
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



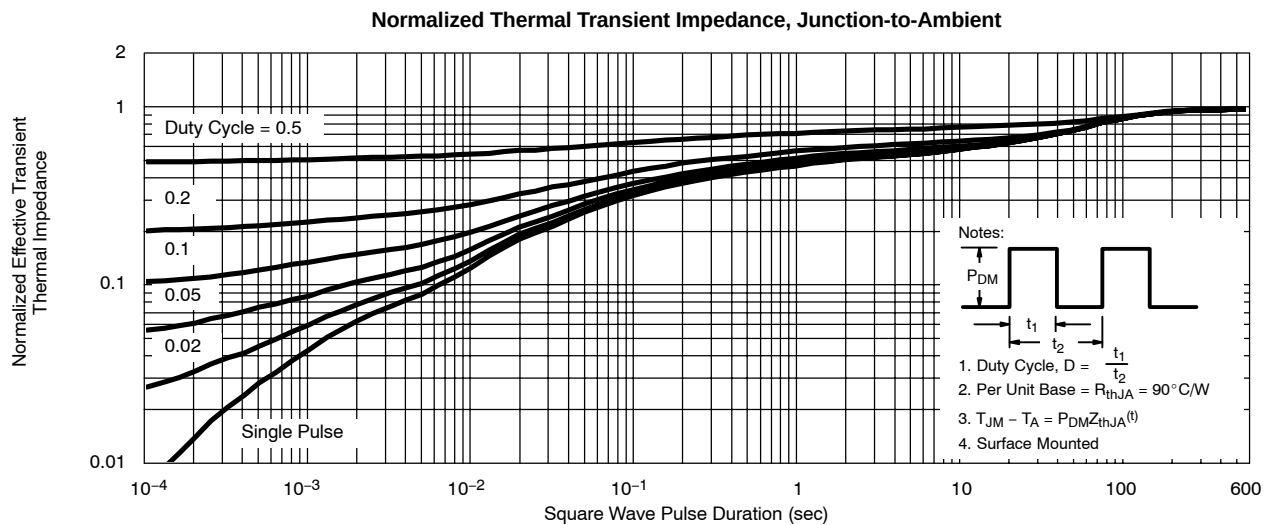
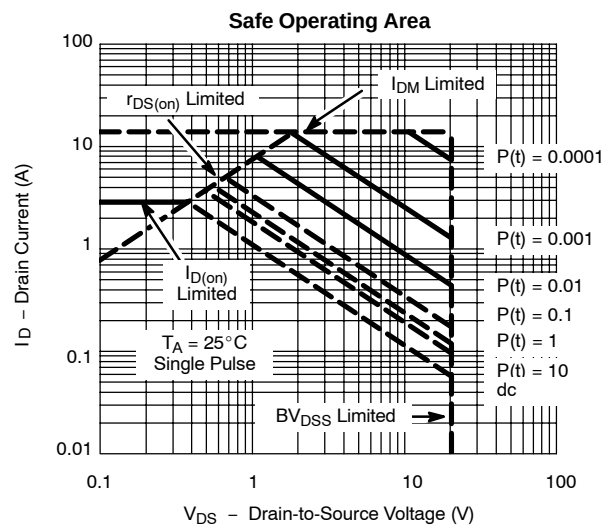
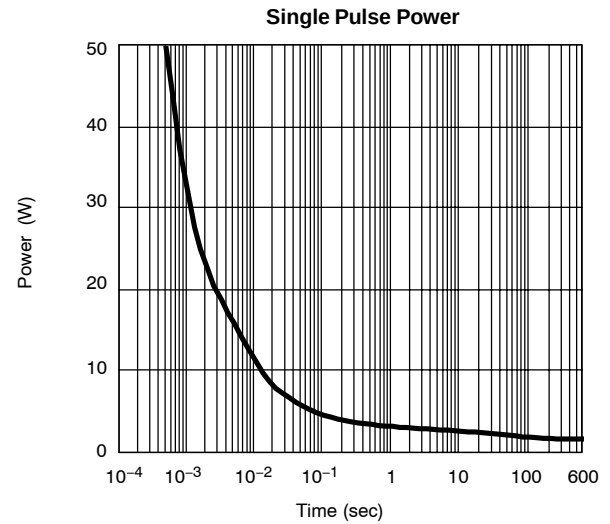
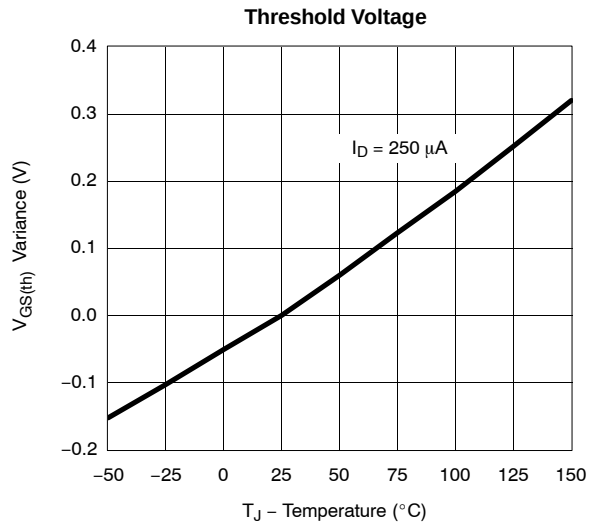
On-Resistance vs. Gate-to-Source Voltage





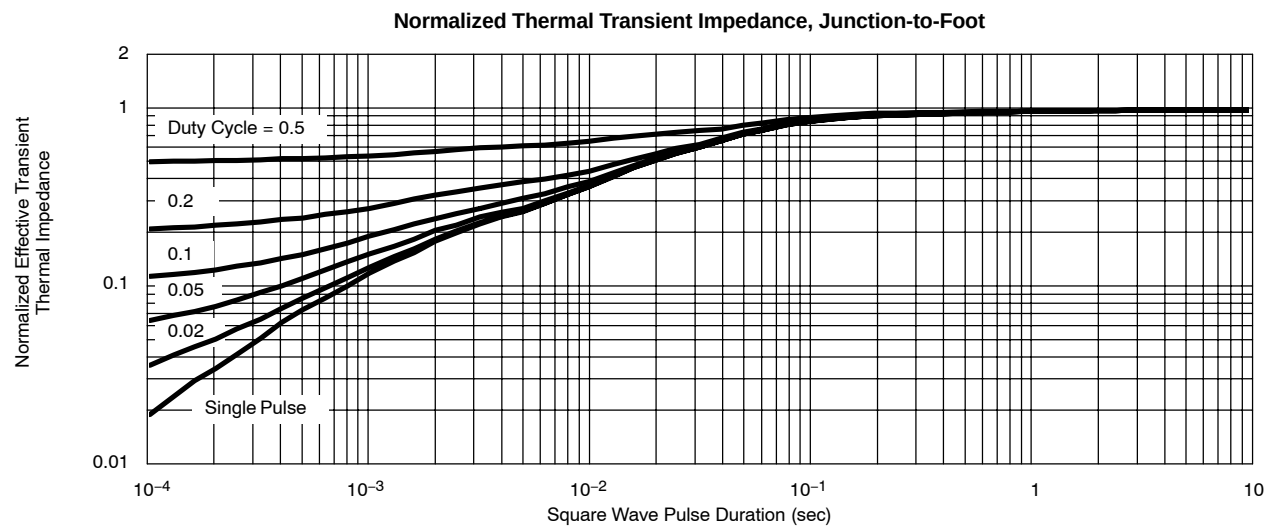
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

P-CHANNEL





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