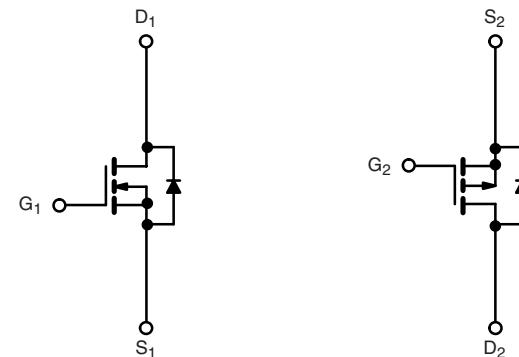
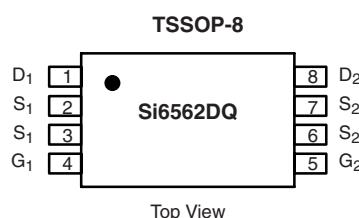


N- and P-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.030 at V _{GS} = 4.5 V	± 4.5
		0.040 at V _{GS} = 2.5 V	± 3.9
P-Channel	- 20	0.050 at V _{GS} = - 4.5 V	± 3.5
		0.085 at V _{GS} = - 2.5 V	± 2.7

FEATURES

- Halogen-free Option Available
- TrenchFET® Power MOSFETs: 2.5 V Rated


RoHS*
COMPLIANT


Ordering Information: Si6562DQ-T1
Si6562DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	- 20	V
Gate-Source Voltage	V _{GS}	± 12	± 12	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	± 4.5	A
	T _A = 70 °C		± 3.6	
Pulsed Drain Current	I _{DM}	± 30	± 30	
Continuous Source Current (Diode Conduction) ^a	I _S	1.25	- 1.25	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	1.0	W
	T _A = 70 °C		0.64	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes:

a. Surface Mounted on FR4 board, t ≤ 10 s.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	N-Ch	0.6			V
		$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	P-Ch	-0.6			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 12 \text{ V}$	N-Ch			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0 \text{ V}$	N-Ch			1	μA
		$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$	P-Ch			-1	
		$V_{DS} = 20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$	N-Ch			25	
		$V_{DS} = -20 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$	P-Ch			-25	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 4.5 \text{ V}$	N-Ch	30			A
		$V_{DS} \geq -5 \text{ V}$, $V_{GS} = -4.5 \text{ V}$	P-Ch	-30			
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$, $I_D = 4.5 \text{ A}$	N-Ch		0.023	0.030	Ω
		$V_{GS} = -4.5 \text{ V}$, $I_D = -3.5 \text{ A}$	P-Ch		0.040	0.050	
		$V_{GS} = 2.5 \text{ V}$, $I_D = 3.9 \text{ A}$	N-Ch		0.030	0.040	
		$V_{GS} = -2.5 \text{ V}$, $I_D = -2.7 \text{ A}$	P-Ch		0.060	0.085	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$	N-Ch		20		S
		$V_{DS} = -10 \text{ V}$, $I_D = -3.5 \text{ A}$	P-Ch		10		
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25 \text{ A}$, $V_{GS} = 0 \text{ V}$	N-Ch		0.65	1.2	V
		$I_S = -1.25 \text{ A}$, $V_{GS} = 0 \text{ V}$	P-Ch		0.72	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 4.5 \text{ A}$ P-Channel $V_{DS} = -15 \text{ V}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -3.5 \text{ A}$	N-Ch		13	25	nC
Gate-Source Charge	Q_{gs}		P-Ch		14.5	25	
Gate-Drain Charge	Q_{gd}		N-Ch		3.0		
Gate-Drain Charge	Q_{gd}		P-Ch		3.5		
Turn-On Delay Time	$t_{d(\text{on})}$	N-Channel $V_{DD} = 10 \text{ V}$, $R_L = 10 \Omega$ $I_D \geq 1 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_G = 6 \Omega$ P-Channel $V_{DD} = -10 \text{ V}$, $R_L = 10 \Omega$ $I_D \geq -1 \text{ A}$, $V_{GEN} = -10 \text{ V}$, $R_G = 6 \Omega$	N-Ch		22	50	ns
Rise Time	t_r		P-Ch		27	50	
Turn-Off Delay Time	$t_{d(\text{off})}$		N-Ch		40	80	
Fall Time	t_f		P-Ch		30	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$	N-Ch		50	100	ns
		$I_F = -1.25 \text{ A}$, $dl/dt = 100 \text{ A}/\mu\text{s}$	P-Ch		57	100	

Notes:

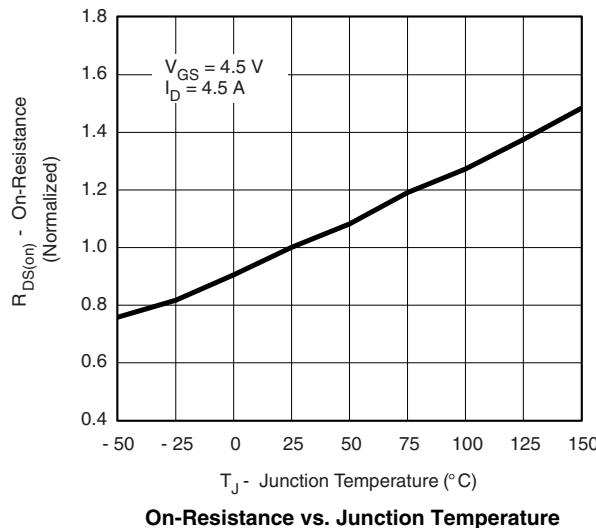
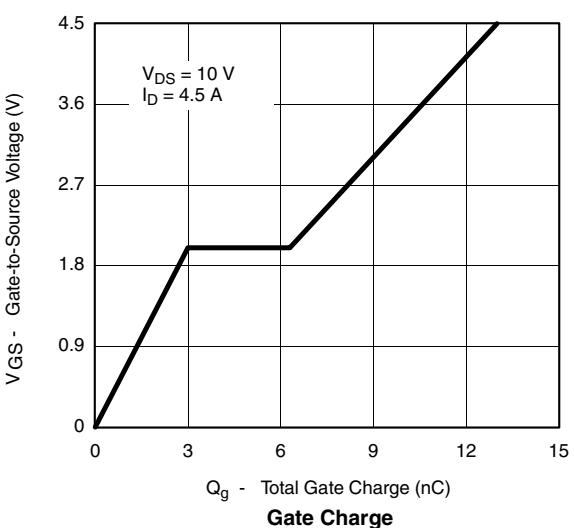
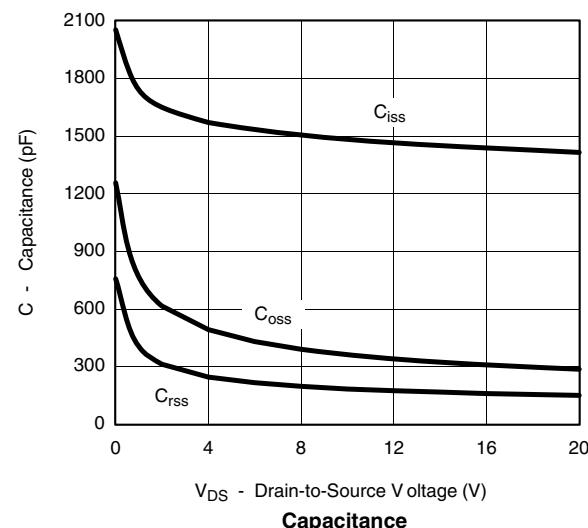
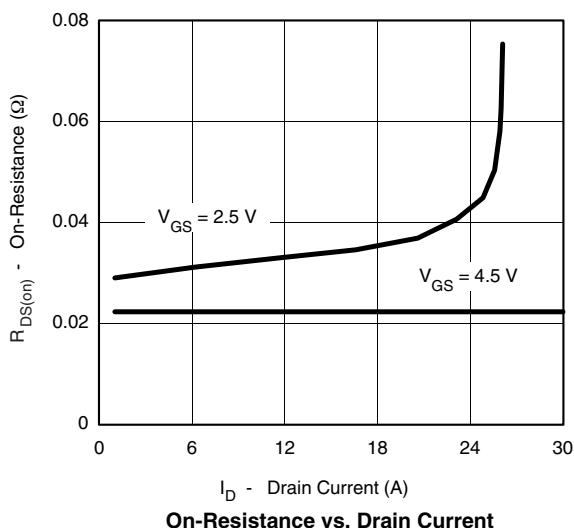
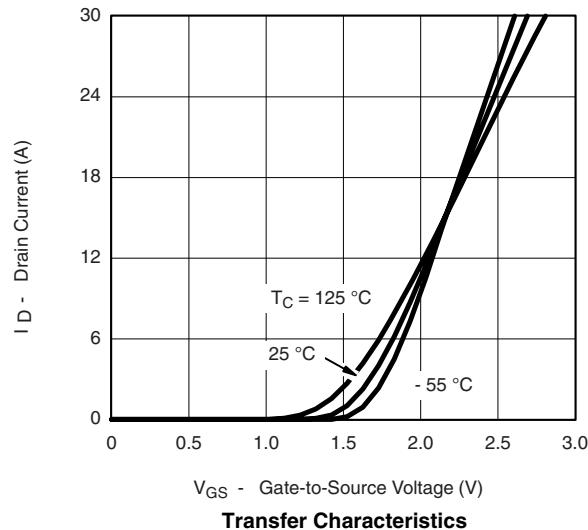
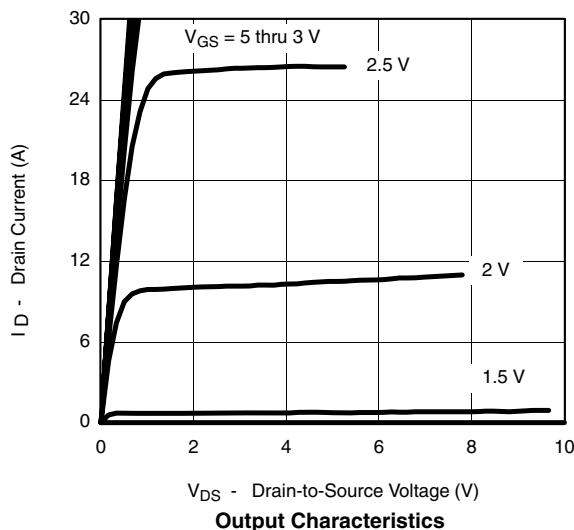
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

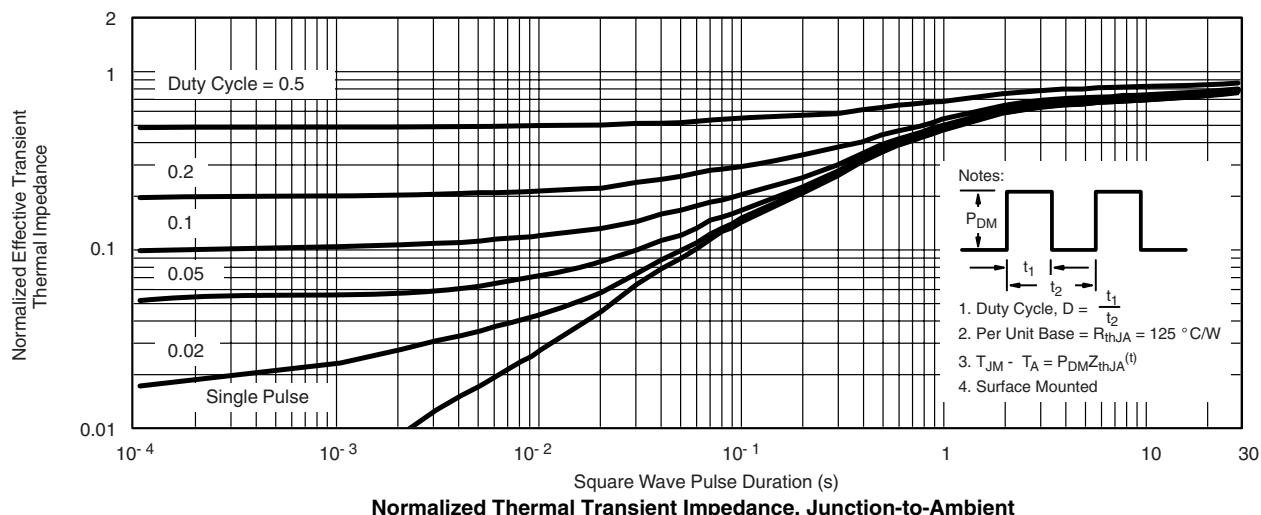
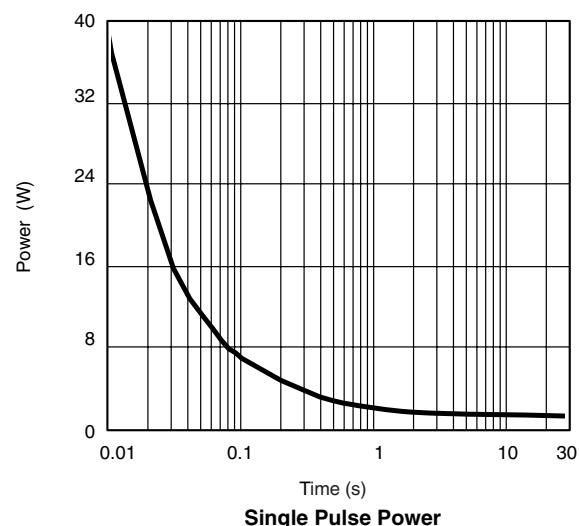
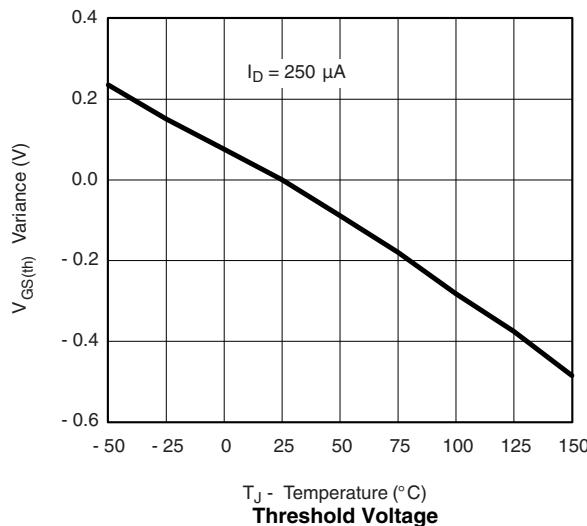
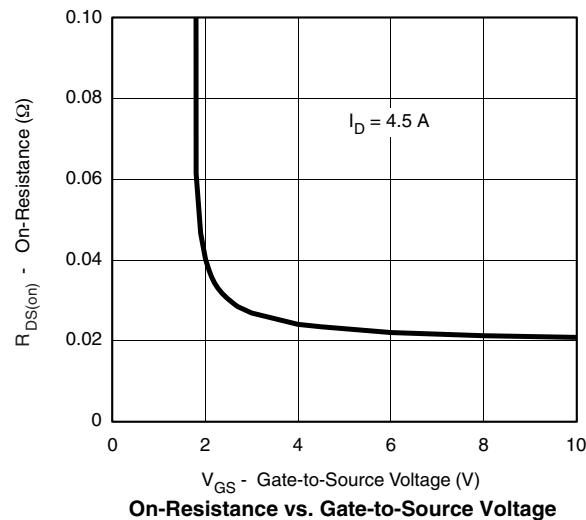
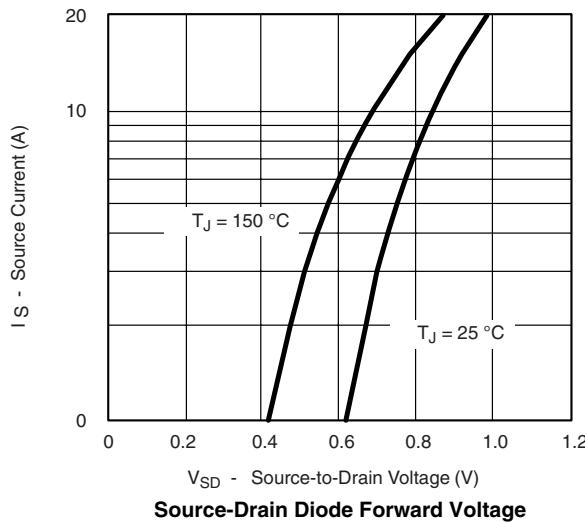
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

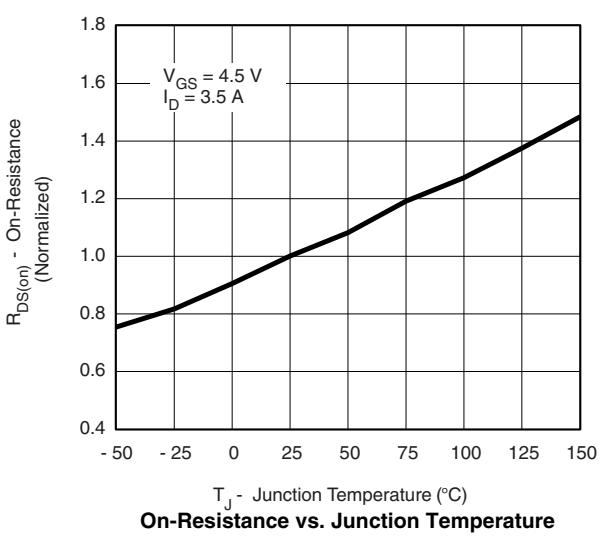
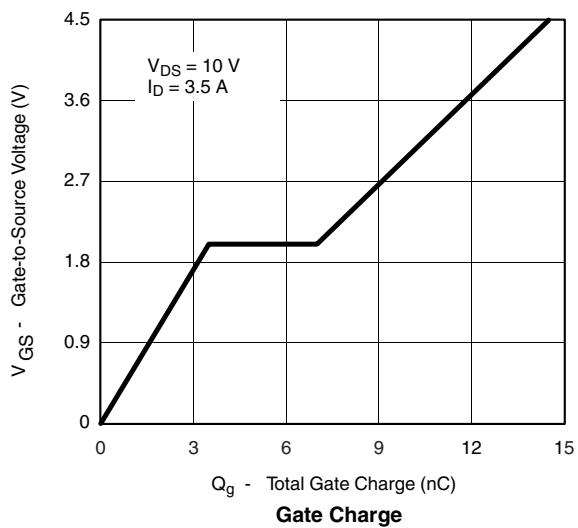
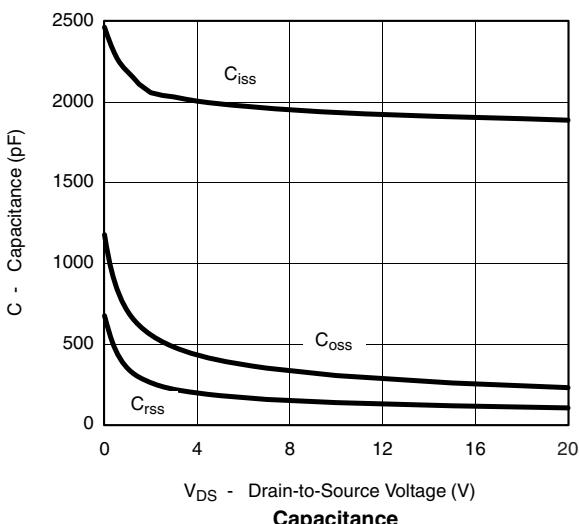
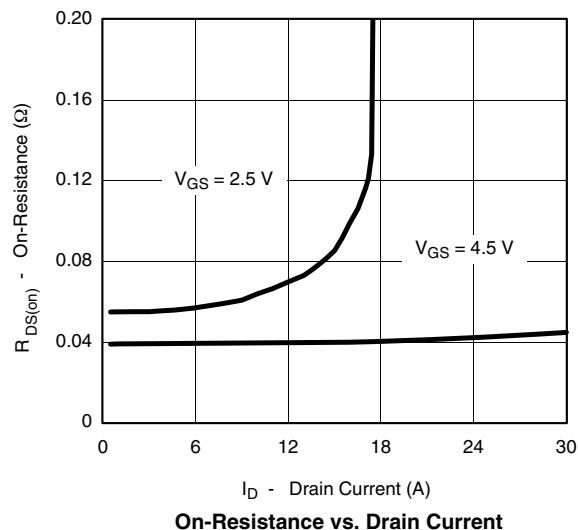
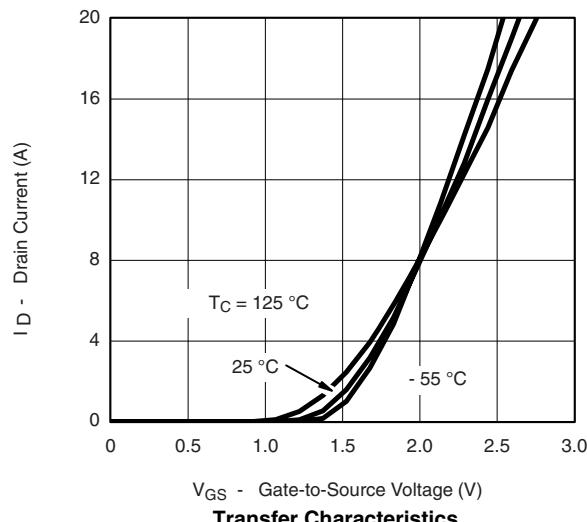
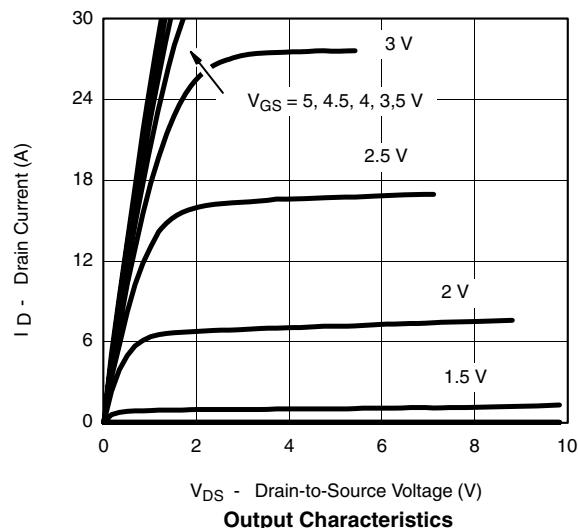
N-CHANNEL TYPICAL CHARACTERISTICS

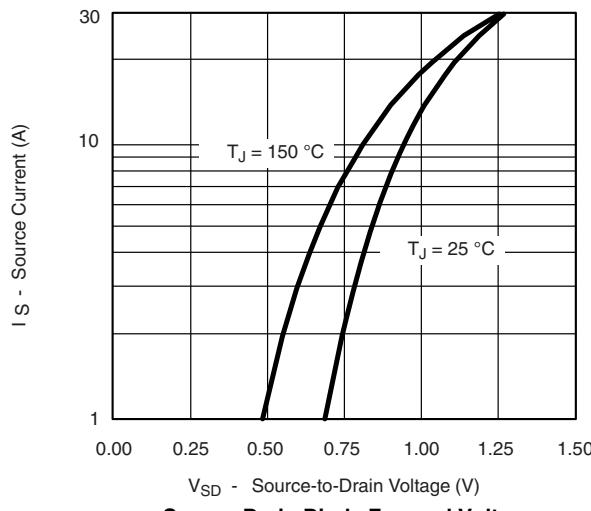
25 °C, unless otherwise noted



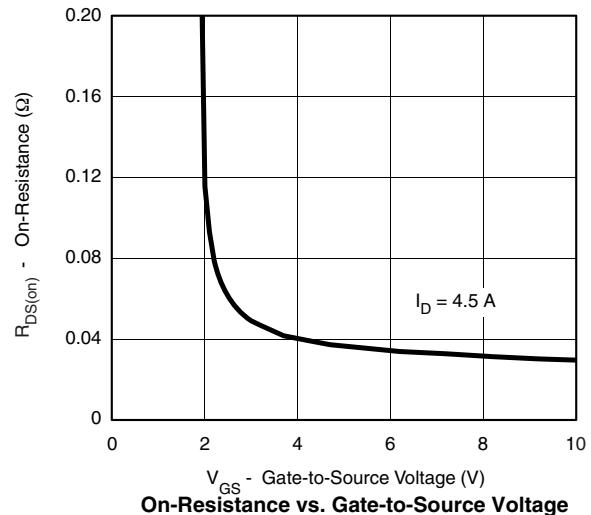
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



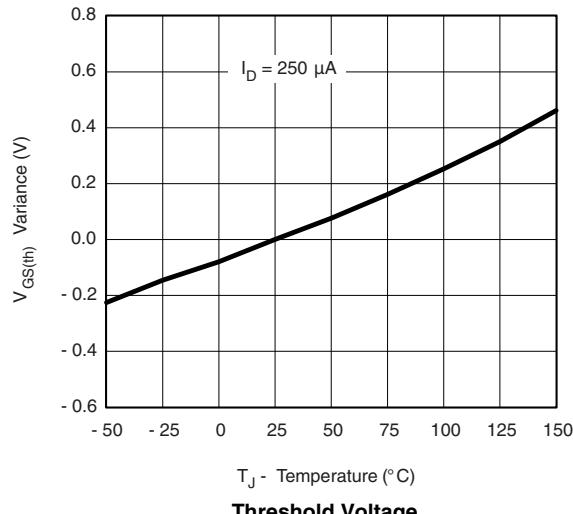
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


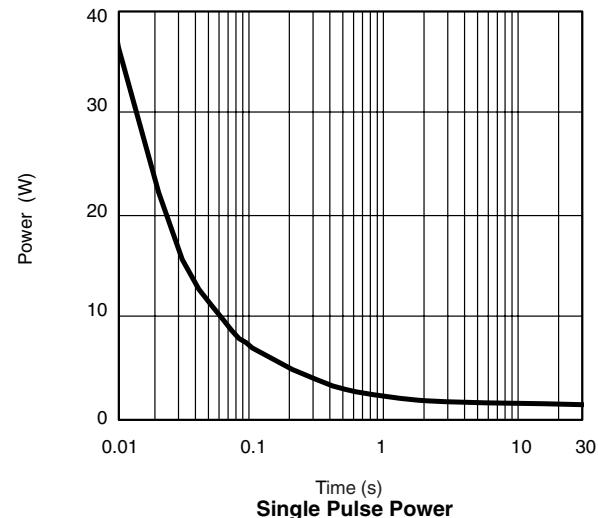
Source-Drain Diode Forward Voltage



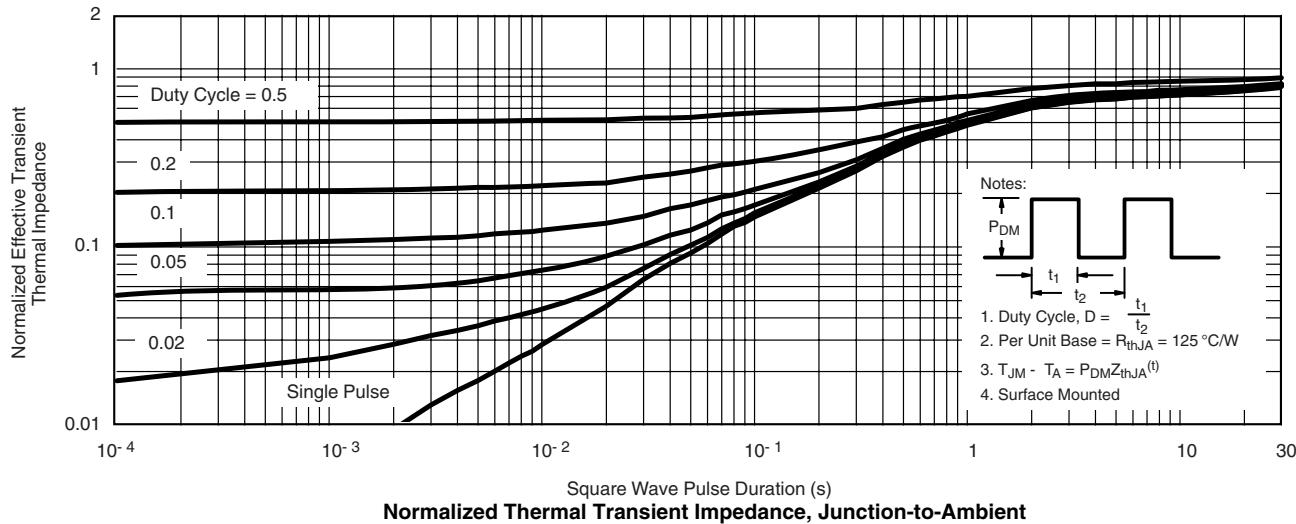
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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