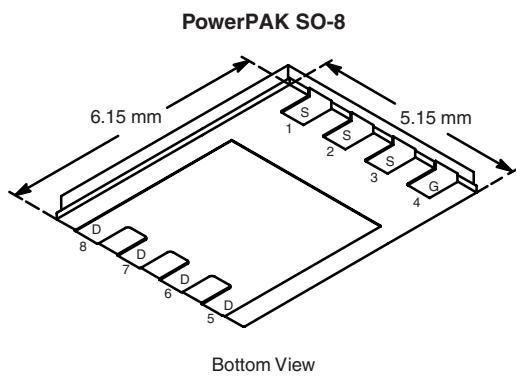


N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
30	0.003 at $V_{GS} = 10$ V	40	54 nC
	0.0035 at $V_{GS} = 4.5$ V	40	

FEATURES

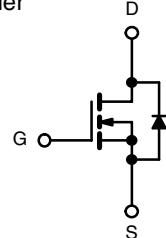
- Halogen-free available
- TrenchFET® Power MOSFET
- PWM Optimized
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested



Ordering Information: Si7380ADP-T1-E3 (Lead (Pb)-free)
Si7380ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- DC/DC Converters
 - Low-Side MOSFET in Synchronous Buck in Desktops
- Secondary Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	30	V	
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150$ °C)	I_D	40	A	
		32		
		31 ^{b, c}		
		25 ^{b, c}		
Pulsed Drain Current	I_{DM}	70		
Continuous Source-Drain Diode Current	I_S	40		
		4.9 ^{b, c}		
Maximum Power Dissipation	P_D	83	W	
		53		
		5.4 ^{b, c}		
		3.4 ^{b, c}		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.5	

Notes:

- Based on $T_C = 25$ °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 65 °C/W.

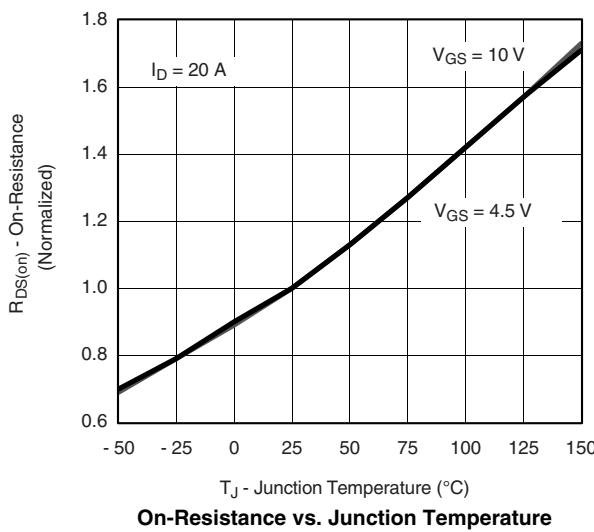
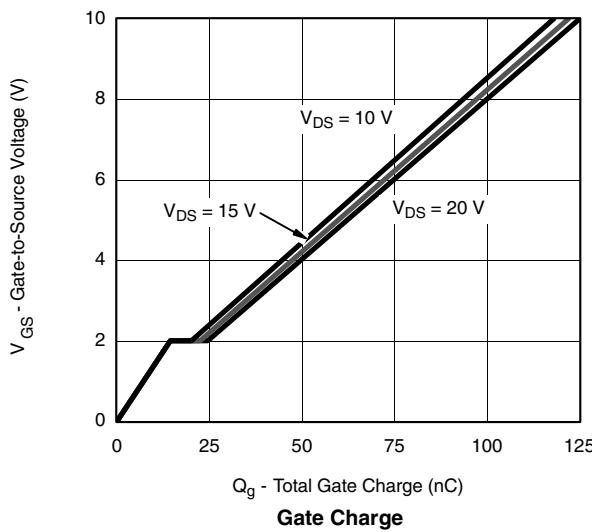
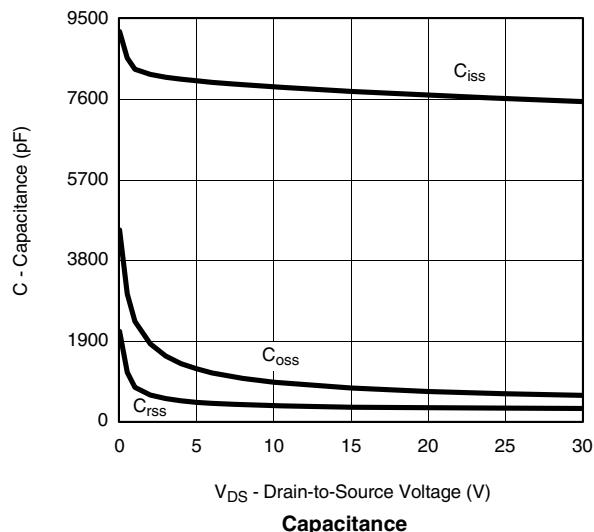
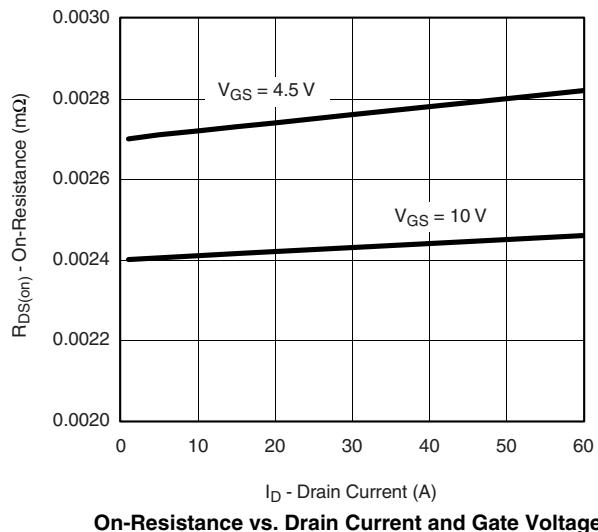
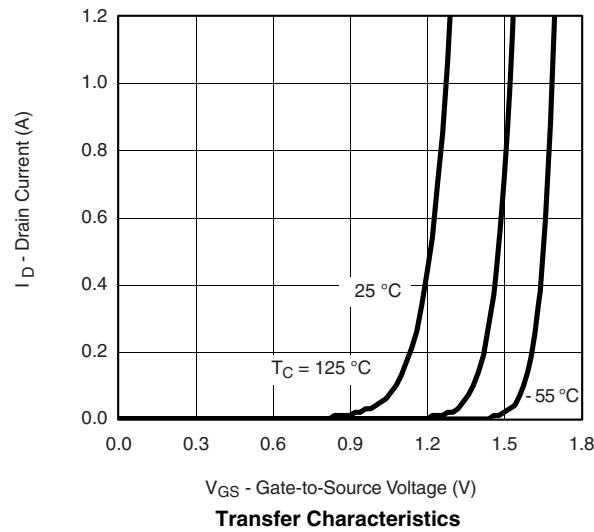
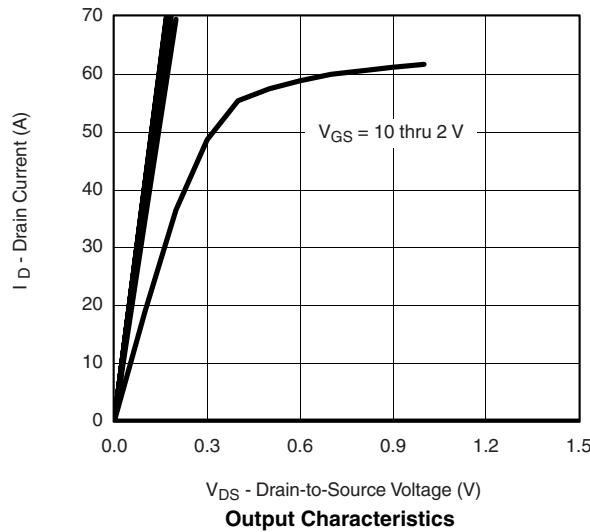
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	30			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		37		$\text{mV}/^\circ\text{C}$	
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			4.3			
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.6		1.6	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA	
		$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$			10		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 10 \text{ V}$	30			A	
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$		0.0024	0.003	Ω	
		$V_{GS} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$		0.0027	0.0035		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 20 \text{ A}$		150		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		7785		pF	
Output Capacitance	C_{oss}			780			
Reverse Transfer Capacitance	C_{rss}			335			
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		122	185	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 15 \text{ A}$		54	85		
Gate-Drain Charge	Q_{gd}			14.5			
Gate Resistance	R_g			8			
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}$, $R_L = 15 \Omega$ $I_D \geq 1 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 6 \Omega$		0.5	1.0	1.5	Ω
Rise Time	t_r				17	25	ns
Turn-Off Delay Time	$t_{d(\text{off})}$				13	20	
Fall Time	t_f				155	235	
					35	55	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			40	A	
Pulse Diode Forward Current ^a	I_{SM}				70		
Body Diode Voltage	V_{SD}	$I_S = 5 \text{ A}$		0.68	1.1	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3 \text{ A}$, $\text{di}/\text{dt} = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$		45	70	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			52	80	nC	
Reverse Recovery Fall Time	t_a			22		ns	
Reverse Recovery Rise Time	t_b			23			

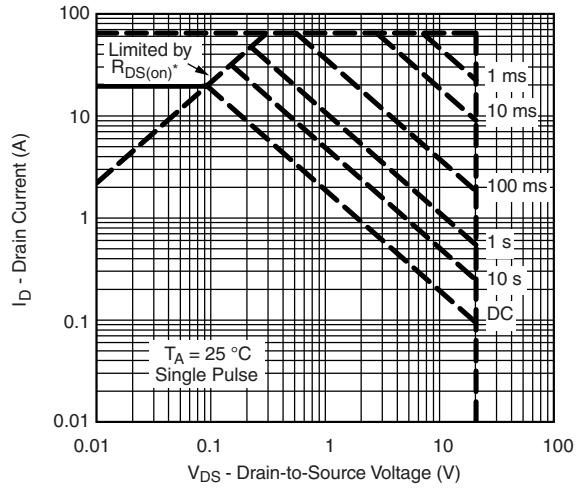
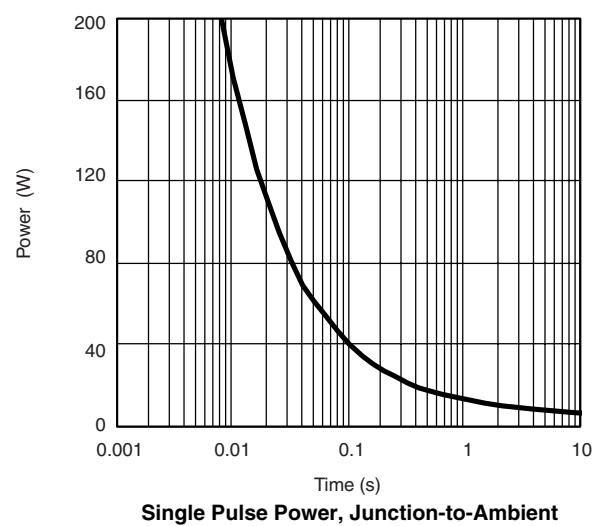
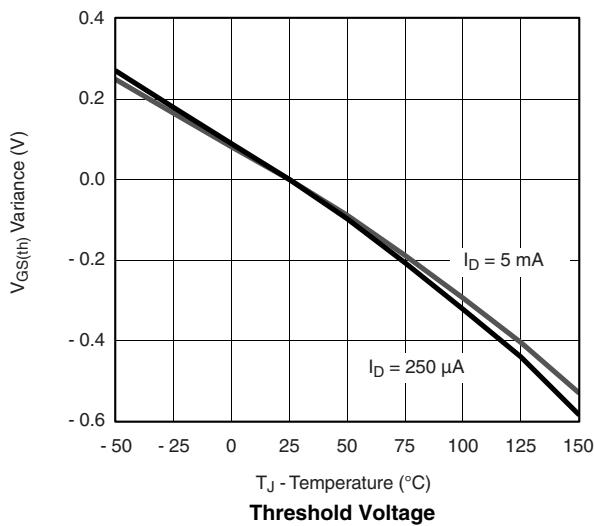
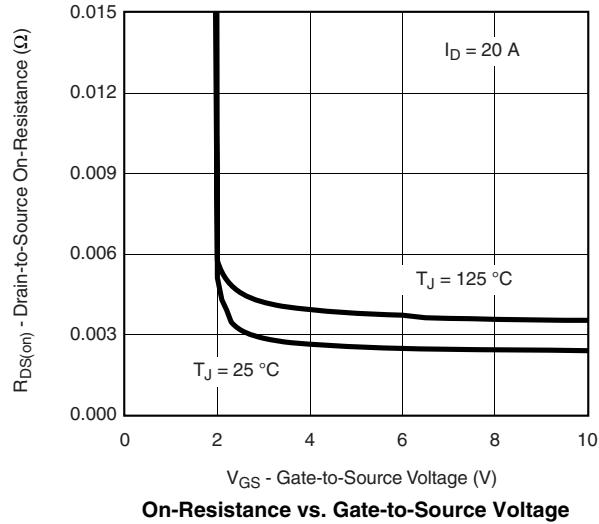
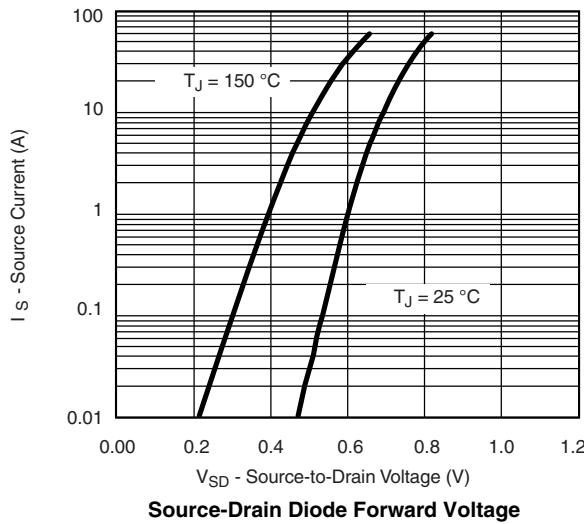
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

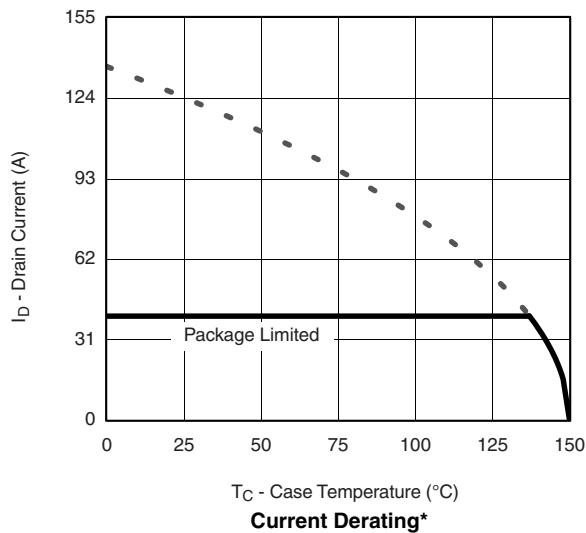
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

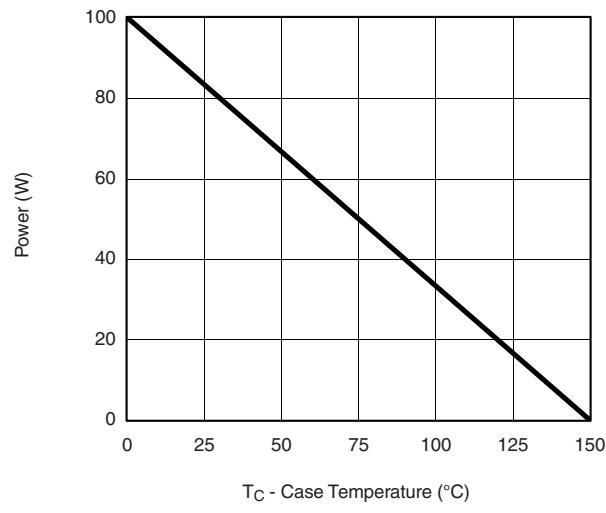
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


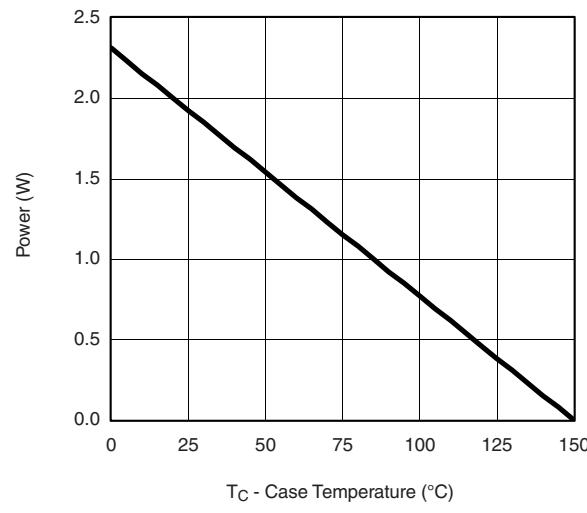
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

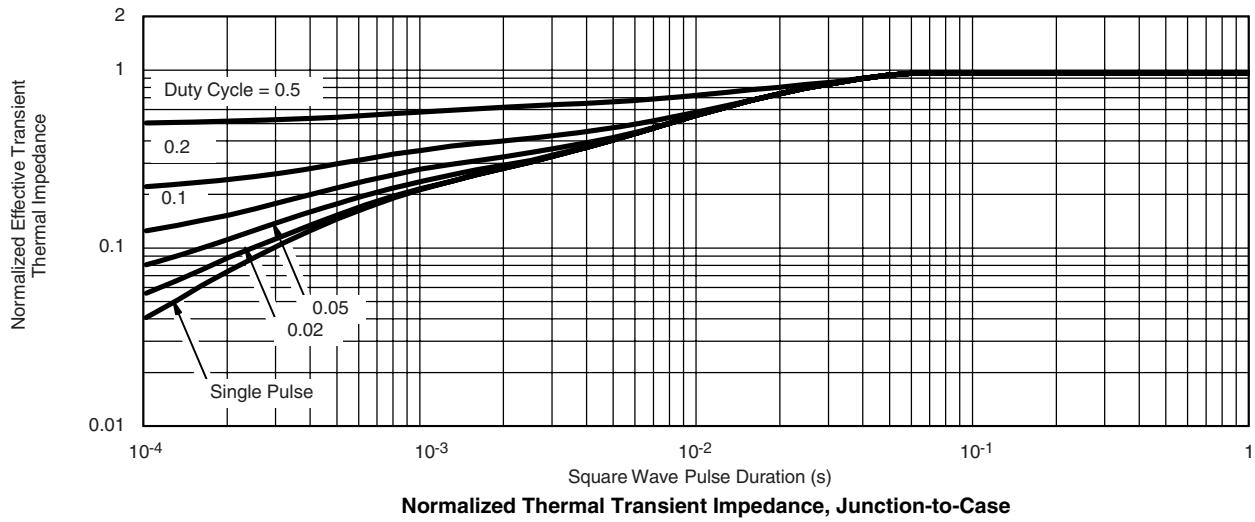
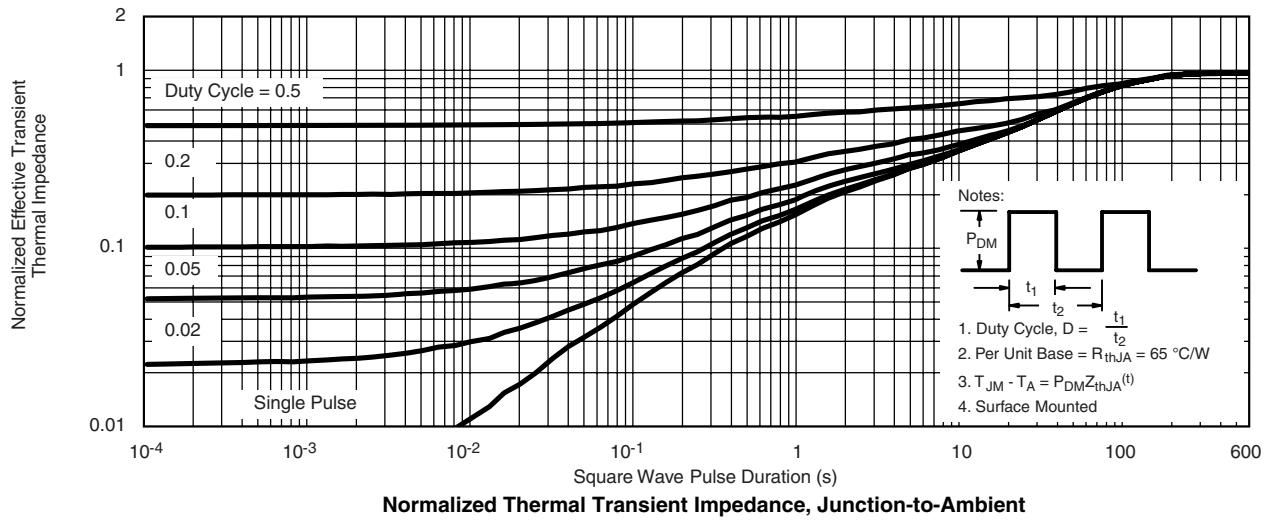
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

 T_C - Case Temperature (°C)

Current Derating*

 T_C - Case Temperature (°C)

Power, Junction-to-Case

 T_C - Case Temperature (°C)

Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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