P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.0057 at V_{GS} = - 10 V	- 24
	0.0095 at V_{GS} = - 4.5 V	- 17

FEATURES

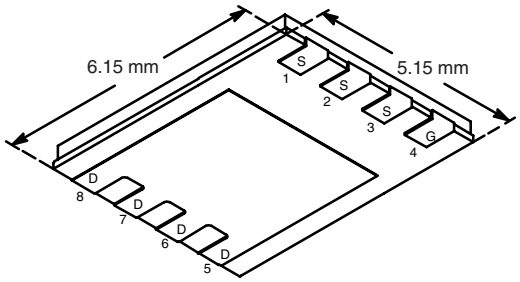
- **Halogen-free According to IEC 61249-2-21 Available**
- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g tested

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

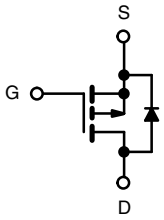
- Battery and Load Switching
  - Notebook Computers
  - Notebook Battery Packs

PowerPAK SO-8



Bottom View

Ordering Information: Si7483ADP-T1-E3 (Lead (Pb)-free)
Si7483ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	- 30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	- 24	- 14	A
	T_A = 70 °C		- 19	- 11	
Pulsed Drain Current		I_{DM}	- 60		
Continuous Source Current (Diode Conduction)[a]		I_S	- 4.5	- 1.6	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	5.4	1.9	W
	T_A = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b,c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	18	23	°C/W
	Steady State		50	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.5	

Notes
a. Surface Mounted on 1" x 1" FR4 board.
b. See Solder Profile (*www.vishay.com/ppg?73257*). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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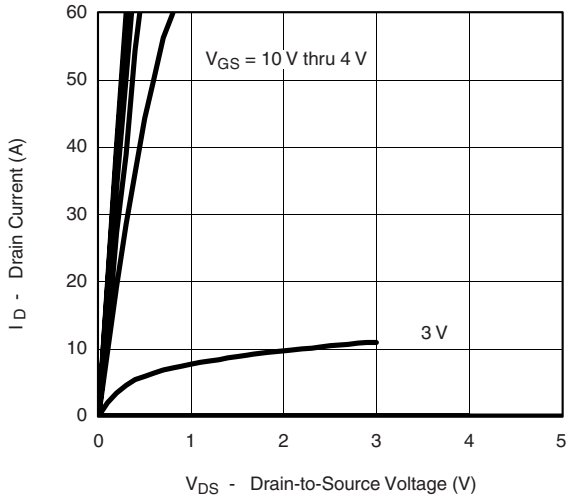
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 µA	- 1.0		- 3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 30 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 30 V, V_{GS} = 0 V, T_J = 70 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = - 5 V, V_{GS} = - 10 V	- 30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 24 A		0.0047	0.0057	Ω
		V_{GS} = - 4.5 V, I_D = - 17 A		0.0075	0.0095	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 24 A		70		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 2.9 A, V_{GS} = 0 V		- 0.73	- 1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 15 V, V_{GS} = - 10 V, I_D = - 24 A		120	180	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			33		
Gate Resistance	R_g		1.6	3.2	4.8	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 15 V, R_L = 15 Ω $I_D \cong$ - 1.0 A, V_{GEN} = - 10 V, R_g = 6 Ω		22	35	ns
Rise Time	t_r			33	50	
Turn-Off Delay Time	$t_{d(off)}$			210	320	
Fall Time	t_f			130	200	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 2.9 A, dI/dt = 100 A/µs		70	130	

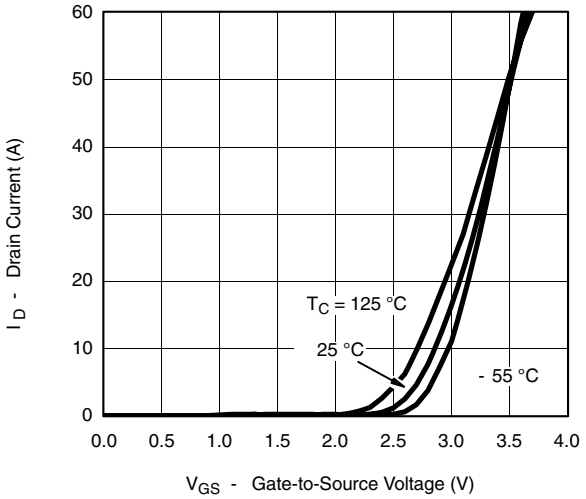
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Output Characteristics



Transfer Characteristics

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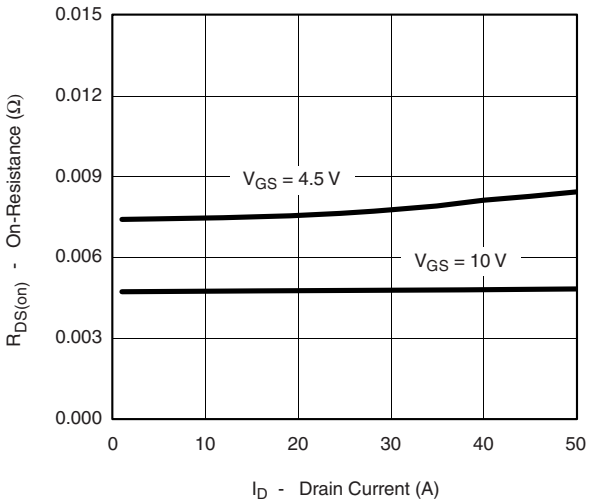
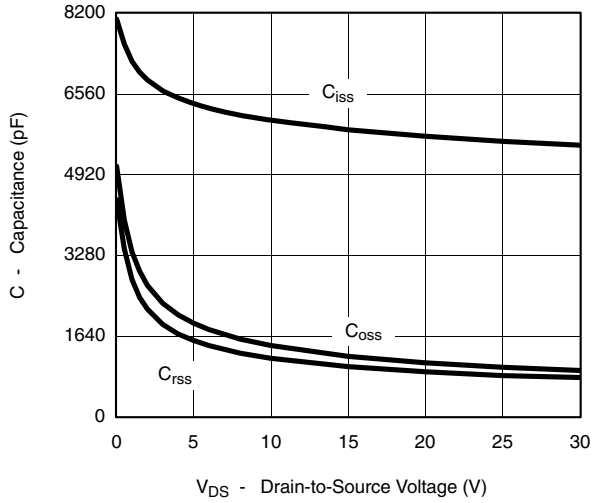
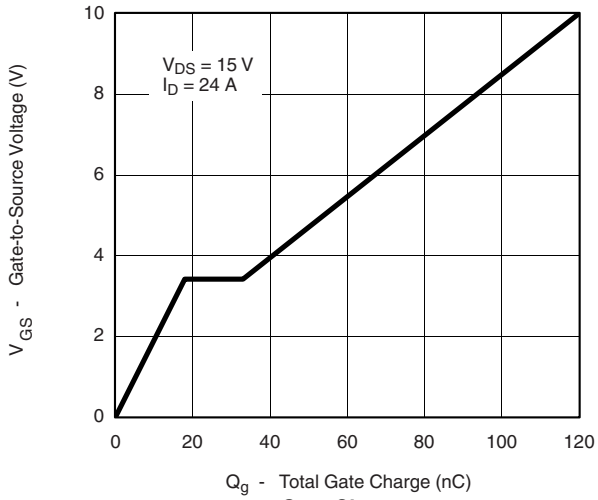


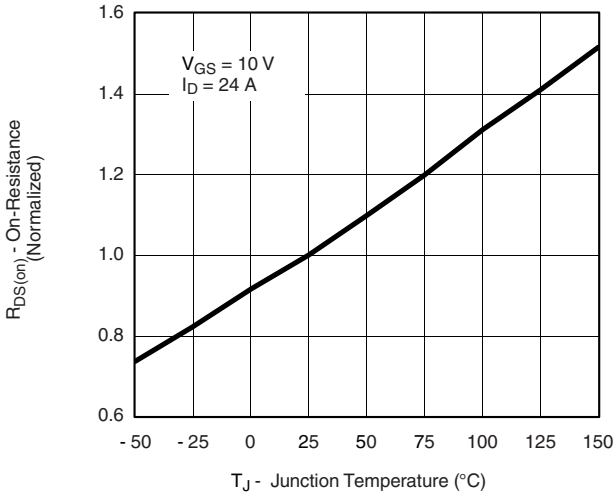
On-Resistance vs. Drain Current



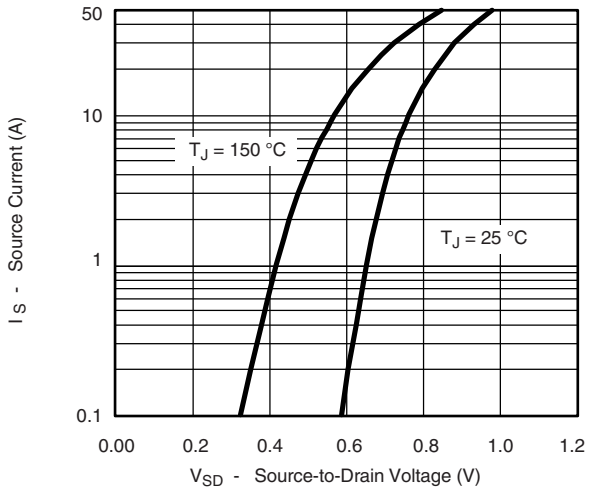
Capacitance



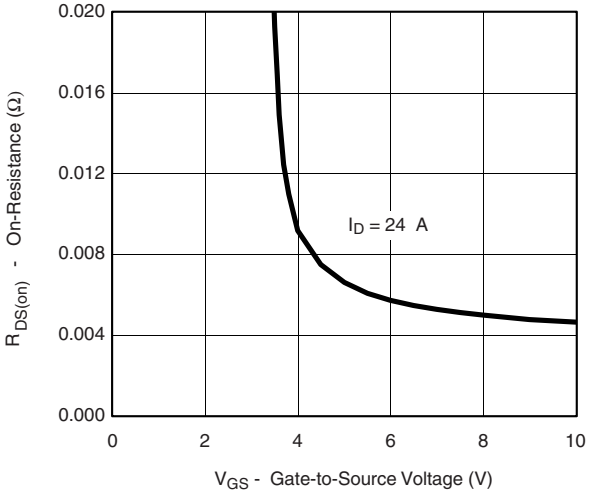
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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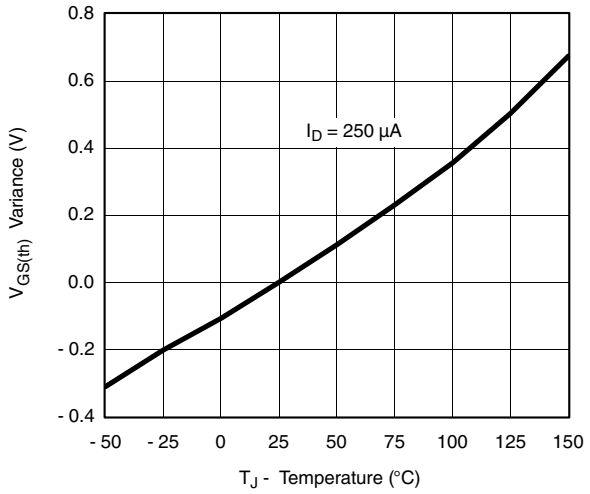
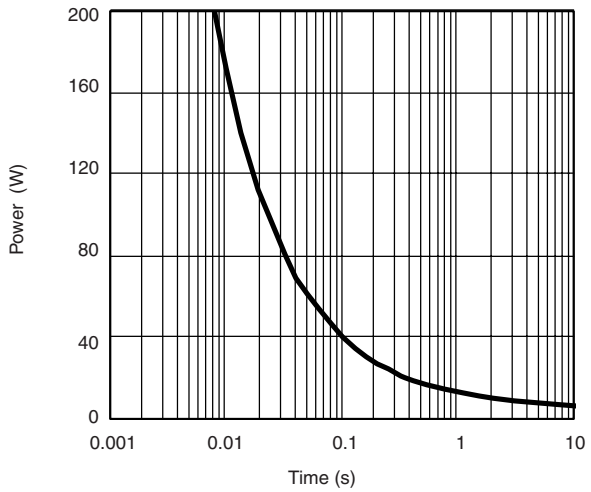
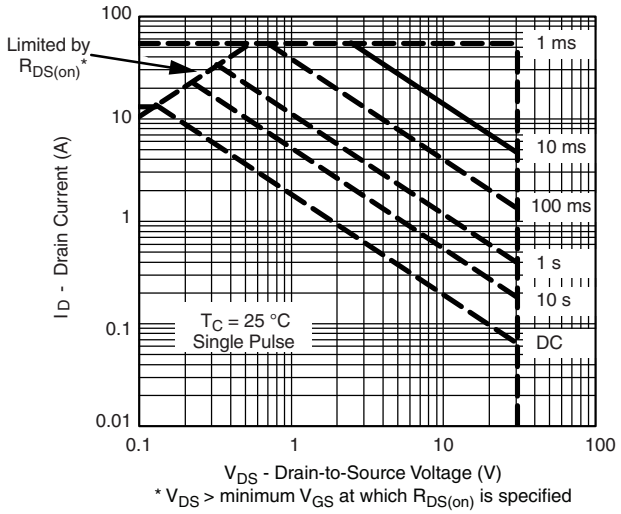


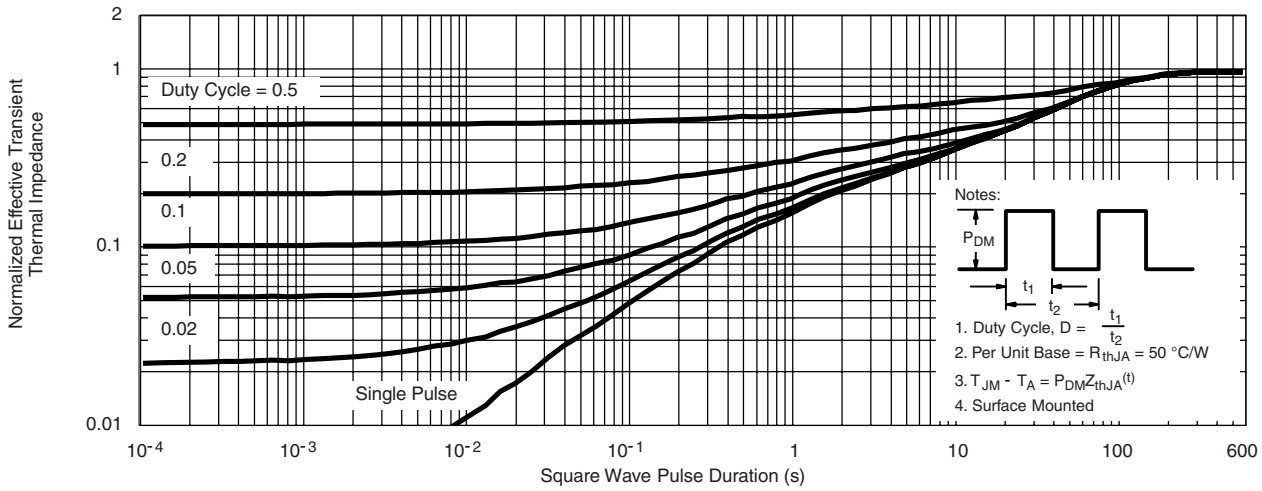
Threshold Voltage



Single Pulse Power



Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

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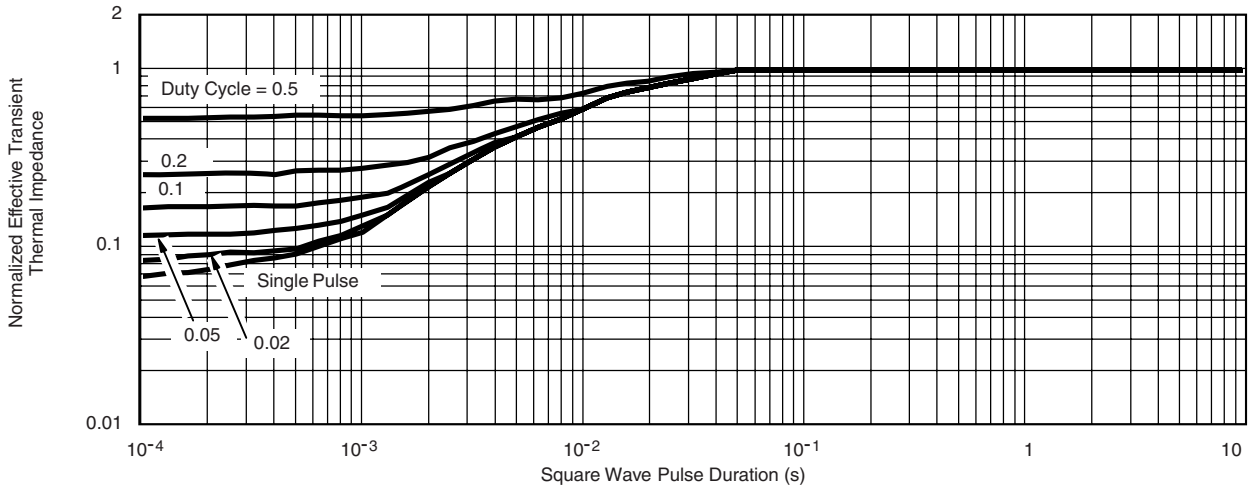

Normalized Thermal Transient Impedance, Junction-to-Case

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