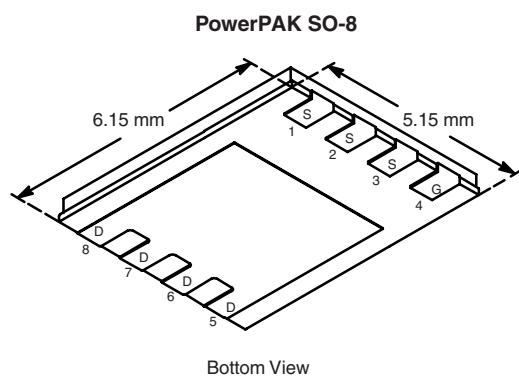


## P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
- 20	0.0073 at $V_{GS} = - 4.5$ V	- 20
	0.0090 at $V_{GS} = - 2.5$ V	- 18
	0.013 at $V_{GS} = - 1.8$ V	- 15



**Ordering Information:** Si7485DP-T1-E3 (Lead (Pb)-free)  
Si7485DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

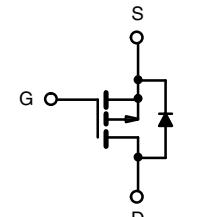
### FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile



### APPLICATIONS

- Battery Switch for Portable Devices



### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	- 20		V
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	- 20	- 12.5	A
$T_A = 70$ °C		- 16.5	- 9.5	
Pulsed Drain Current	$I_{DM}$	- 50		
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	- 4.5	- 1.6	
Maximum Power Dissipation <sup>a</sup>	$P_D$	5	1.8	W
$T_A = 70$ °C		3.2	1.1	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		
Soldering Recommendations (Peak Temperature) <sup>b,c</sup>		260		°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	20	25	°C/W
Steady State		54	68	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.7	2.2	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

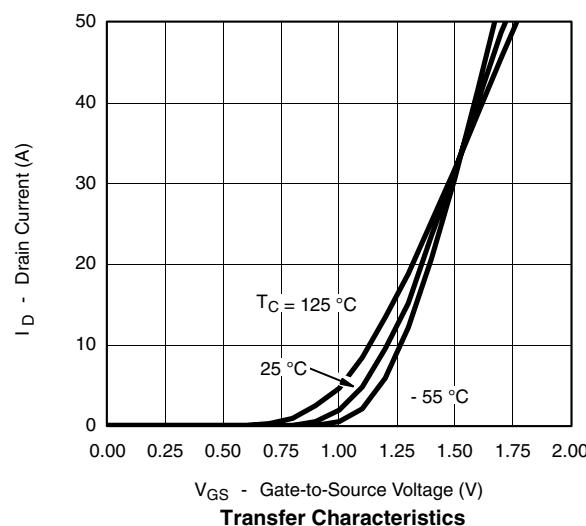
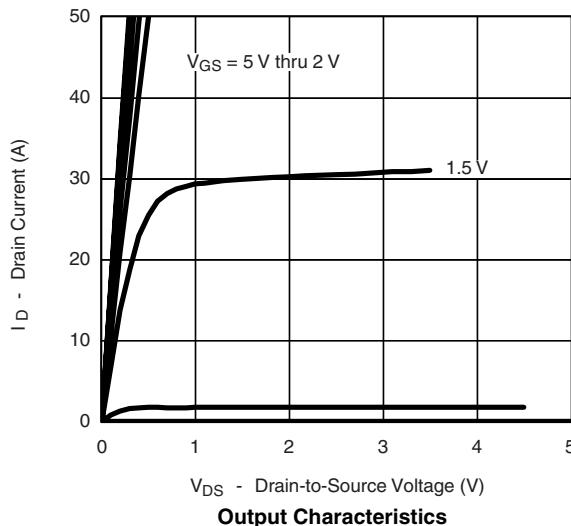
**SPECIFICATIONS**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

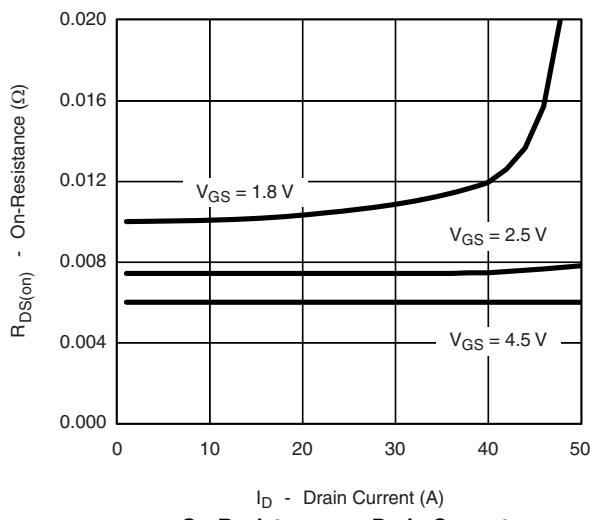
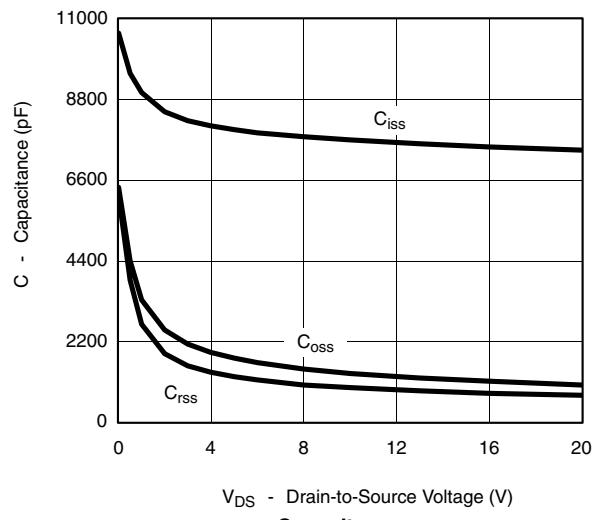
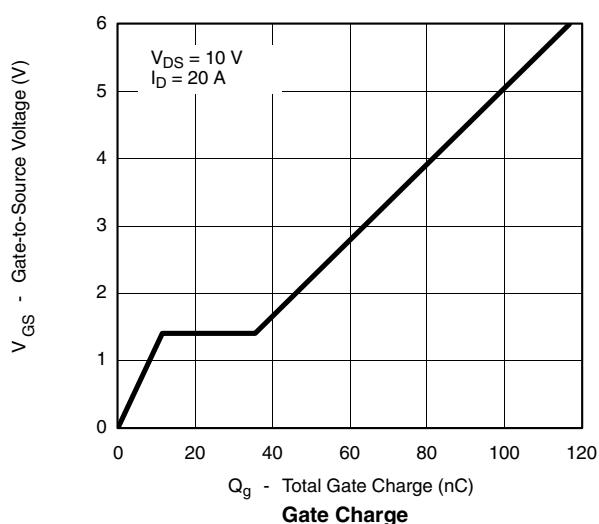
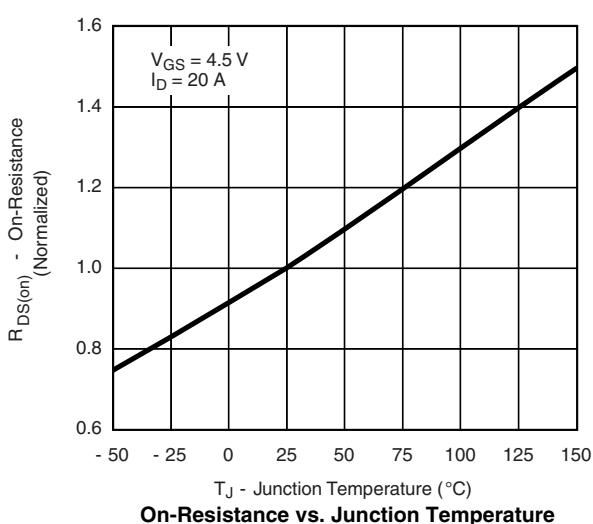
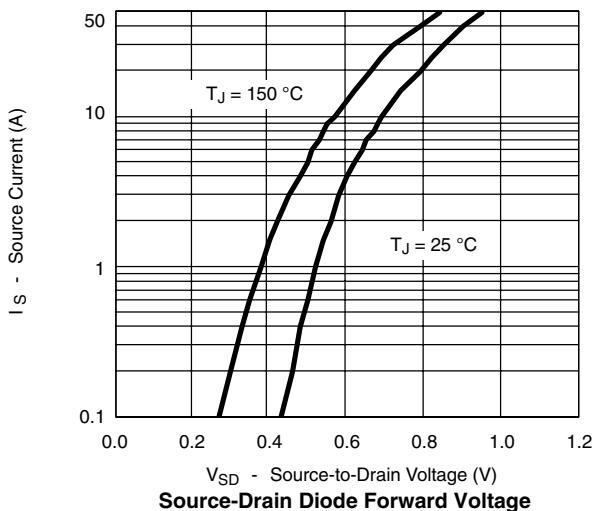
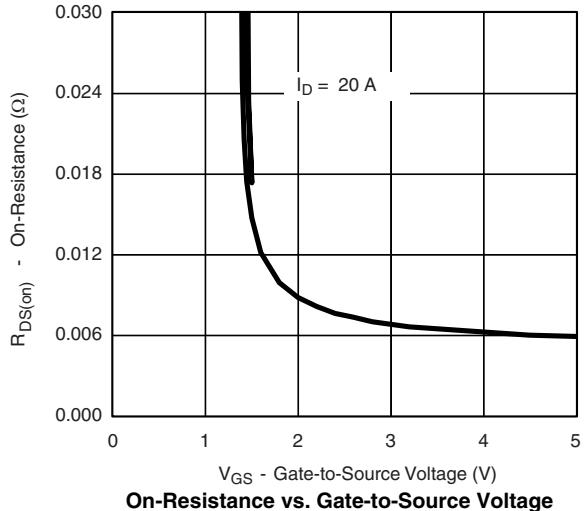
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = -1 \text{ mA}$	-0.4		-0.9	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 8 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-1		$\mu\text{A}$
		$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 70^\circ\text{C}$		-10		
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq -5 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$	-40			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = -4.5 \text{ V}$ , $I_D = -20 \text{ A}$		0.006	0.0073	$\Omega$
		$V_{GS} = -2.5 \text{ V}$ , $I_D = -18 \text{ A}$		0.0074	0.0090	
		$V_{GS} = -1.8 \text{ V}$ , $I_D = -15 \text{ A}$		0.0106	0.013	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15 \text{ V}$ , $I_D = -20 \text{ A}$		80		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -4.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$		-0.62	-1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10 \text{ V}$ , $V_{GS} = -5 \text{ V}$ , $I_D = -20 \text{ A}$		99	150	nC
Gate-Source Charge	$Q_{gs}$			11.5		
Gate-Drain Charge	$Q_{gd}$			29		
Gate Resistance	$R_g$			2.4		$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -10 \text{ V}$ , $R_L = 10 \Omega$ $I_D \equiv -1 \text{ A}$ , $V_{GEN} = -4.5 \text{ V}$ , $R_g = 6 \Omega$		80	120	ns
Rise Time	$t_r$			140	210	
Turn-Off Delay Time	$t_{d(\text{off})}$			360	540	
Fall Time	$t_f$			170	260	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -2.9 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}$		55	80	

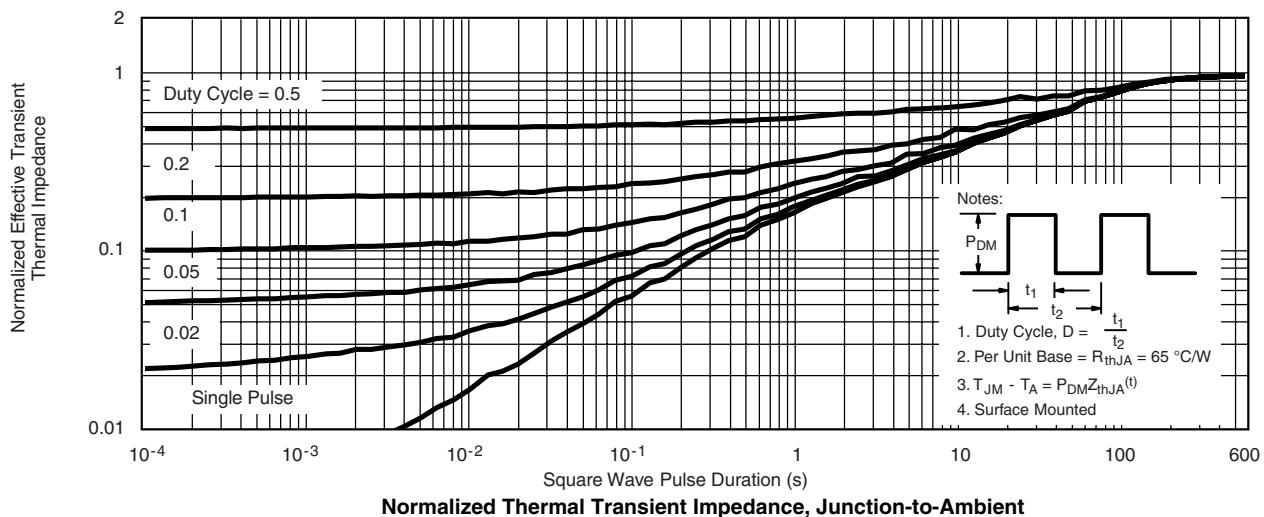
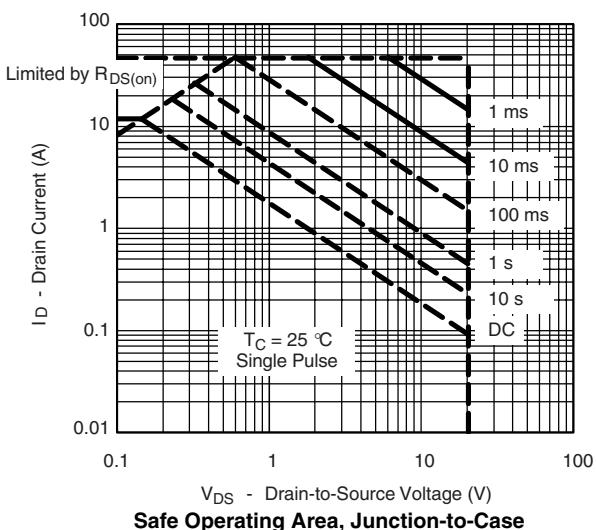
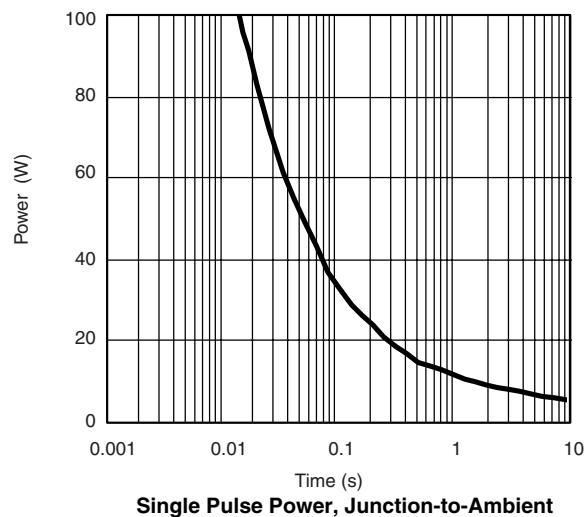
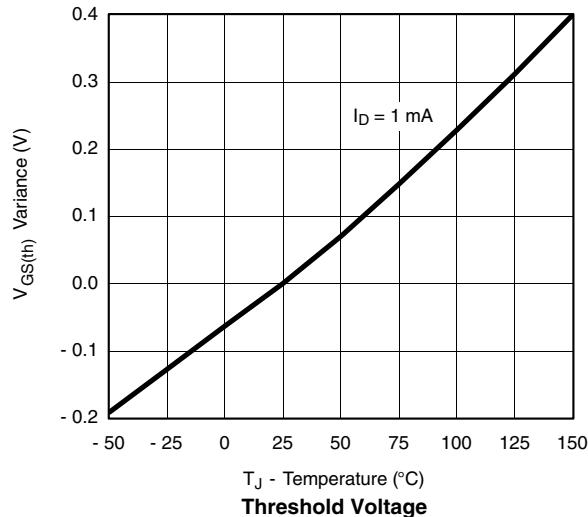
## Notes:

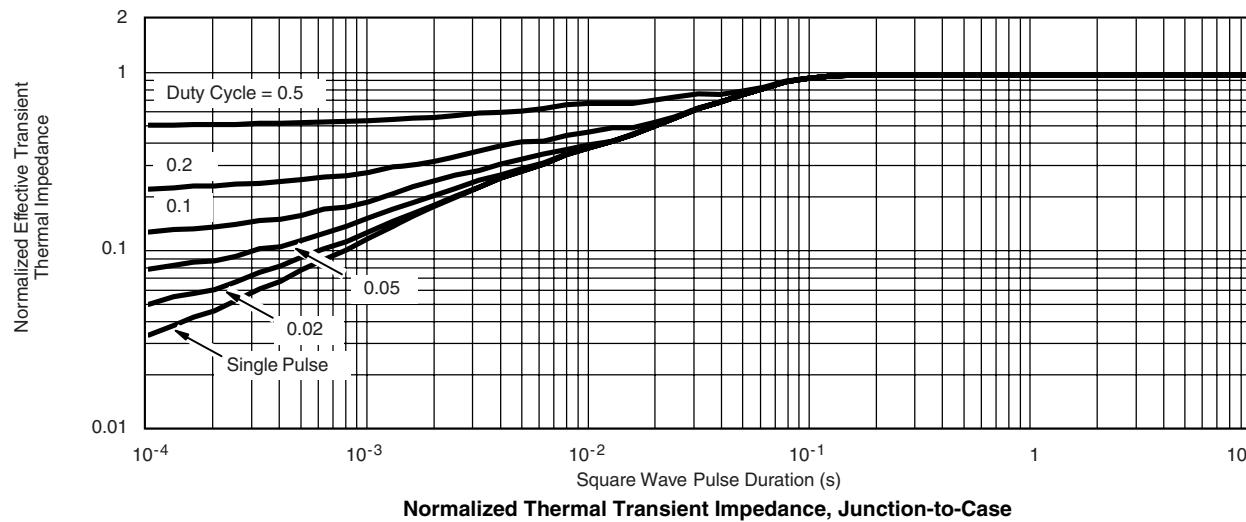
a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2 \%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted


**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


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