

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.019 at $V_{GS} = - 4.5$ V	- 16 ^e	16.2 nC
	0.031 at $V_{GS} = - 2.5$ V	- 16 ^e	

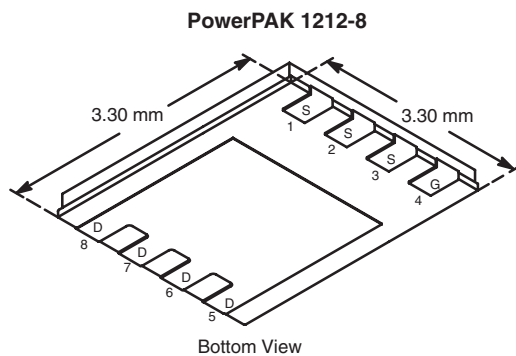
FEATURES

- Halogen-free Option Available
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07 mm Profile
- PWM Optimized
- 100 % R_g and UIS Tested

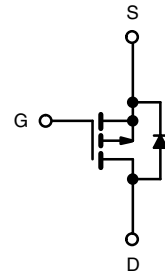

RoHS
COMPLIANT

APPLICATIONS

- DC/DC Buck Converter
- High-Side Application for Asynchronous Buck



Ordering Information: Si7601DN-T1-E3 (Lead (Pb)-free)
Si7601DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	- 16 ^e	A
		- 16 ^e	
		- 11.5 ^{a, b}	
		- 9.2 ^{a, b}	
Pulsed Drain Current	I_{DM}	- 40	A
Continuous Source-Drain Diode Current	I_S	- 16 ^e	
		- 3.15 ^{a, b}	
Avalanche Current	I_{AS}	15	mJ
Single-Pulse Avalanche Energy	E_{AS}	11.25	
Maximum Power Dissipation	P_D	52	W
		33	
		3.8 ^{a, b}	
		2.4 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 50 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{c, d}		260	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Package limited.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	26	33	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 81 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

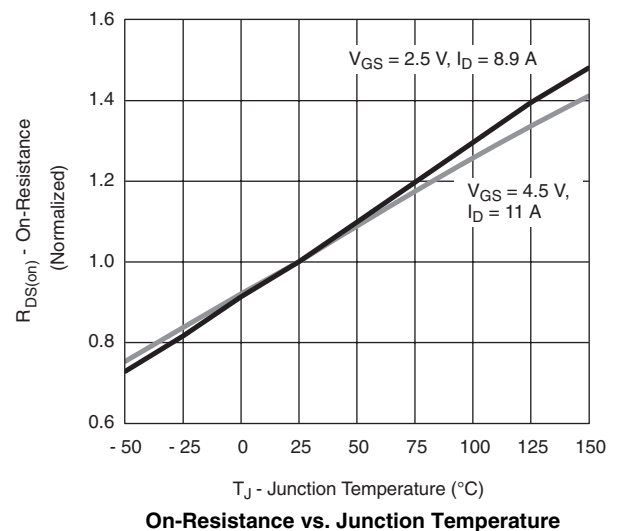
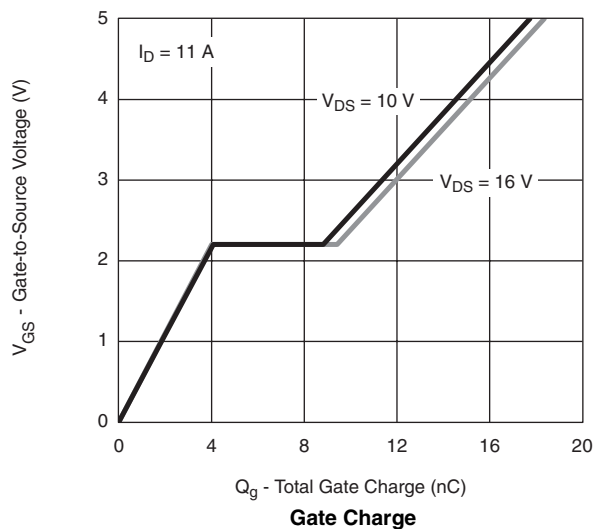
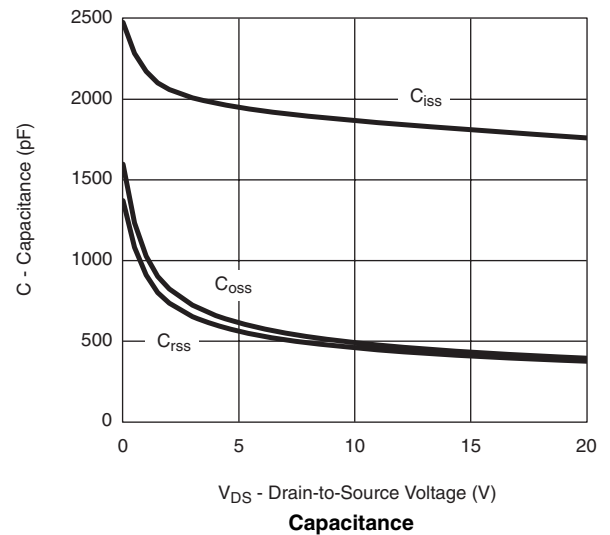
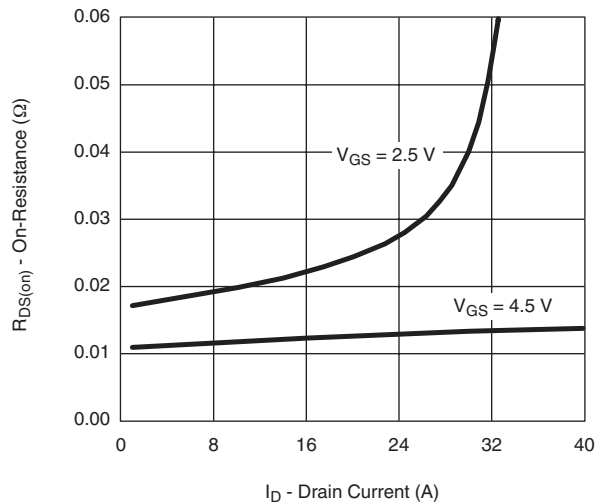
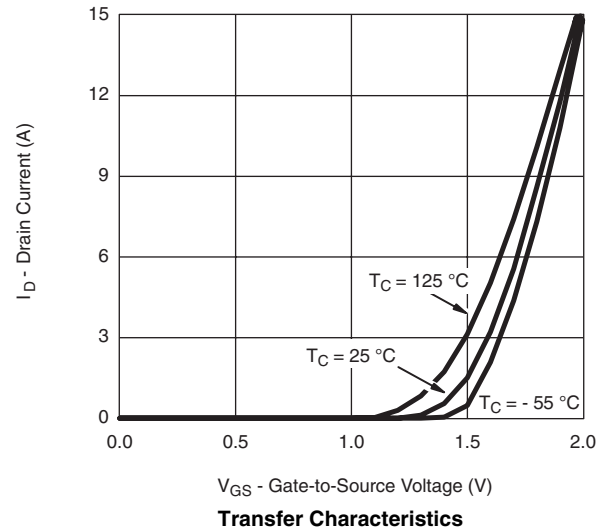
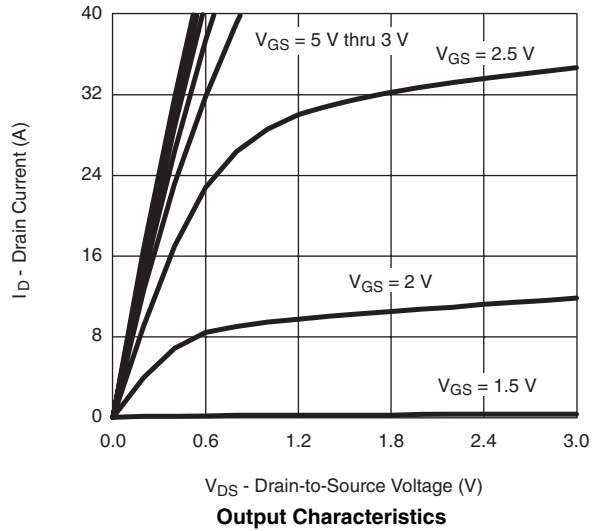
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 16.8		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.63		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.6		- 1.6	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 5 V, V _{GS} = - 4.5 V	- 40			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 11 A		0.016	0.0192	Ω
		V _{GS} = - 2.5 V, I _D = - 8.9 A		0.025	0.0313	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 11 A		31.7		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		1870		pF
Output Capacitance	C _{oss}			490		
Reverse Transfer Capacitance	C _{rss}			460		
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 5 V, I _D = - 11 A		18	27	nC
		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 11 A		16.2	25	
Gate-Source Charge	Q _{gs}			4.1		
Gate-Drain Charge	Q _{gd}			4.8		
Gate Resistance	R _g	f = 1 MHz		6.1	9.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 1.09 Ω I _D ≡ - 9.2 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		18	27	ns
Rise Time	t _r			112	168	
Turn-Off Delay Time	t _{d(off)}			53	80	
Fall Time	t _f			80	120	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 16	A
Pulse Diode Forward Current ^a	I _{SM}				- 40	
Body Diode Voltage	V _{SD}	I _S = - 6 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 5 A, dI/dt = 100 A/μs, T _J = 25 °C		42	63	ns
Body Diode Reverse Recovery Charge	Q _{rr}			25.2	38	nC
Reverse Recovery Fall Time	t _a			14		ns
Reverse Recovery Rise Time	t _b			28		

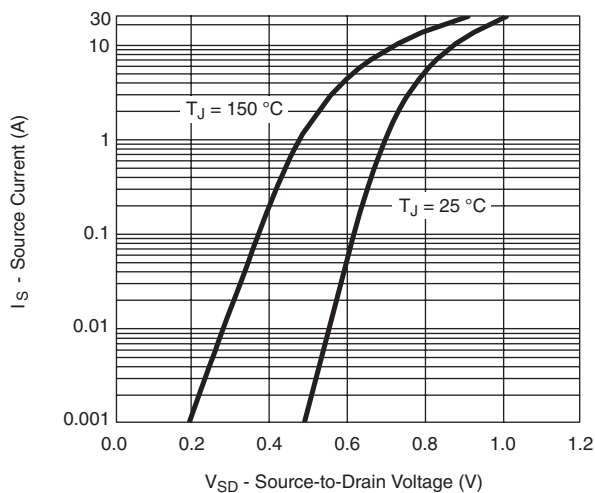
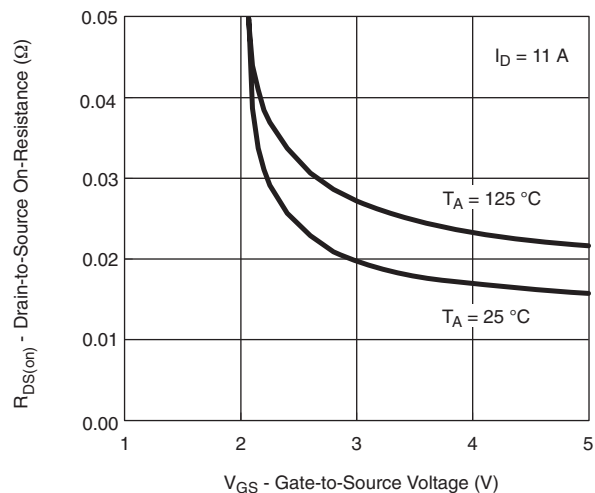
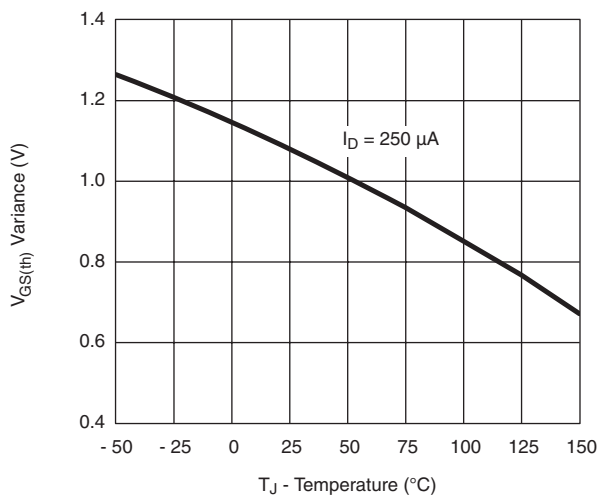
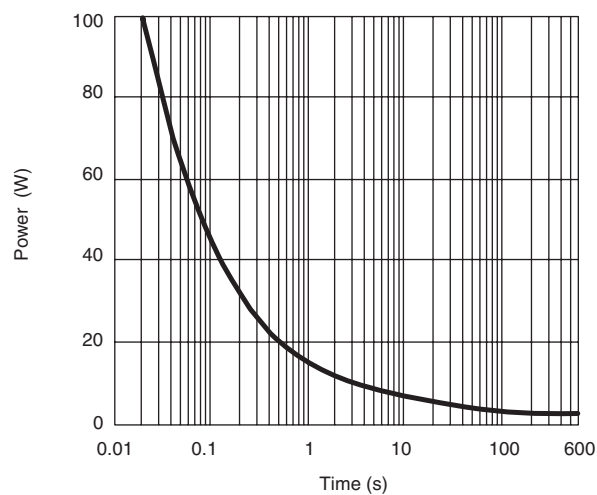
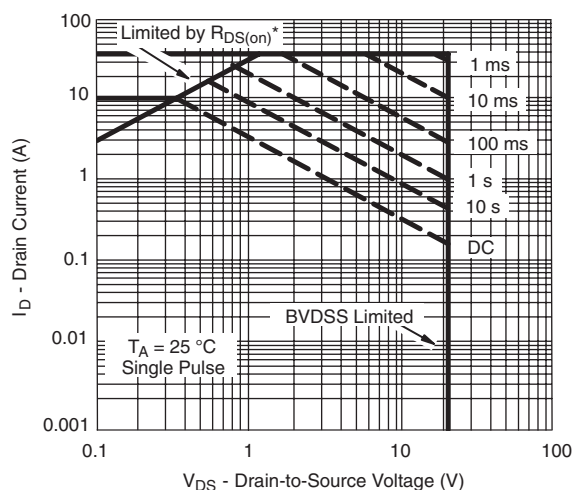
Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

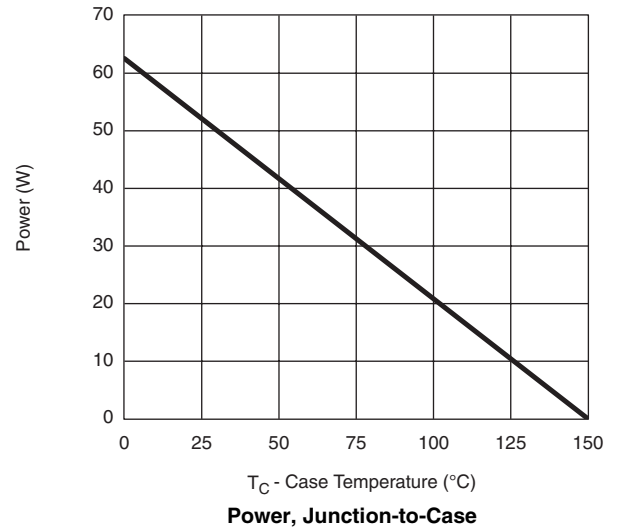
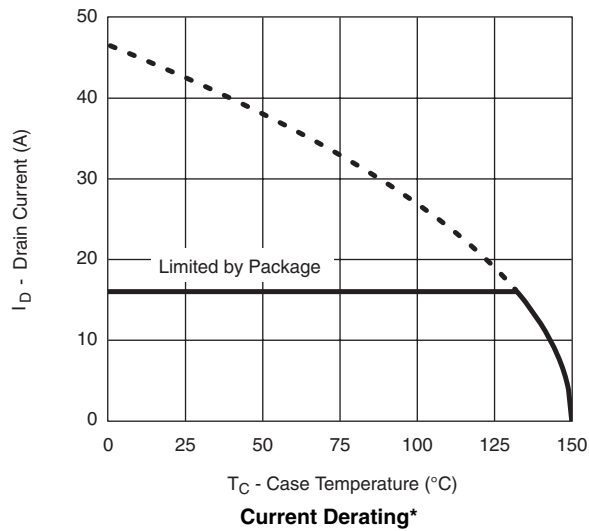
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

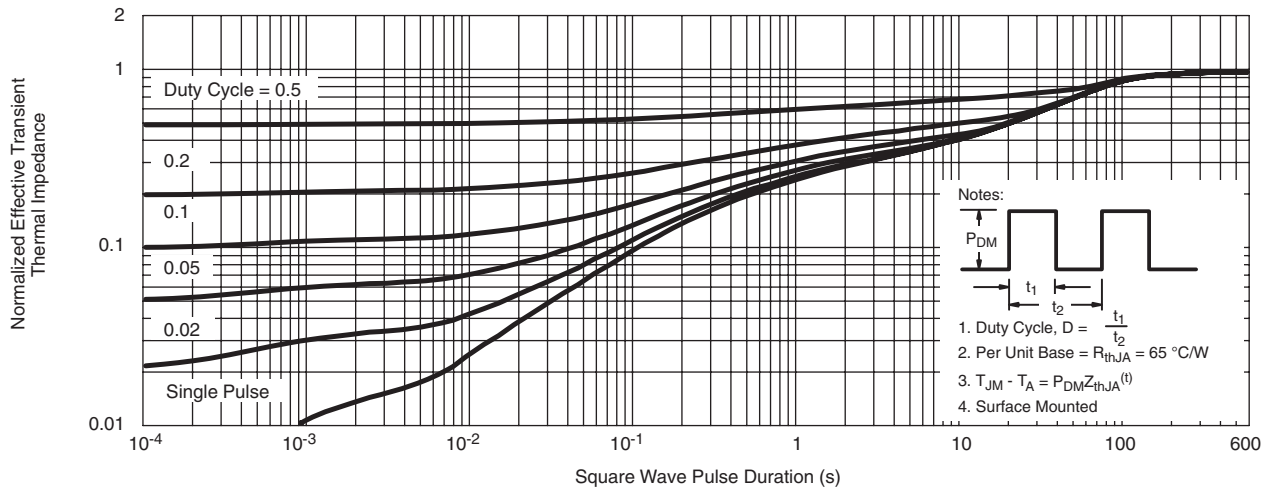
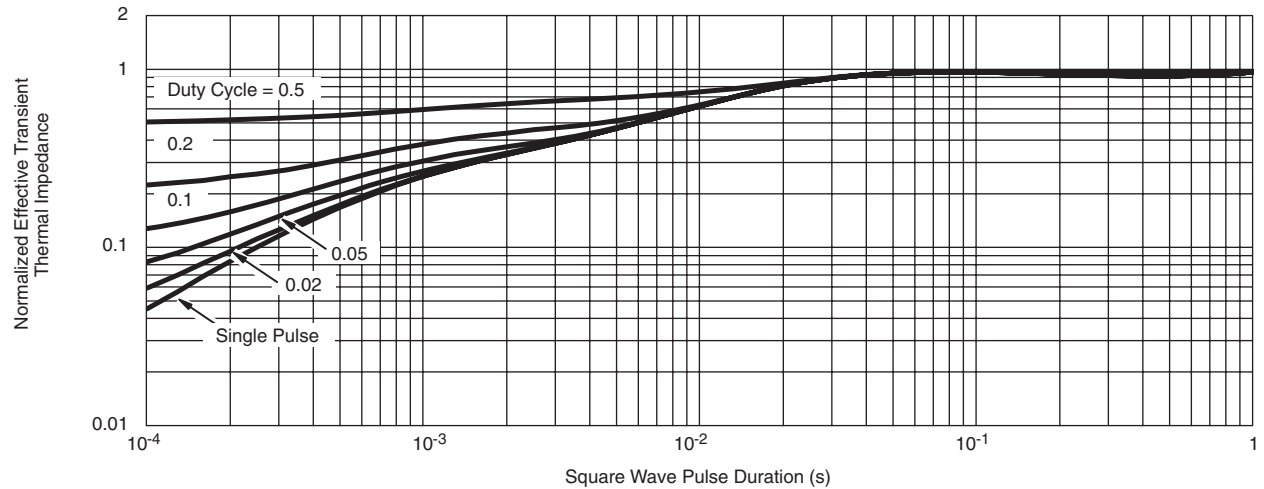
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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