

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.051 at $V_{GS} = - 4.5$ V	- 5.7
	0.067 at $V_{GS} = - 2.5$ V	- 5.0
	0.094 at $V_{GS} = - 1.8$ V	- 4.2

FEATURES

- Halogen-free Option Available
- TrenchFET® Power MOSFETS: 1.8 V Rated
- New Low Thermal Resistance PowerPAK® Package

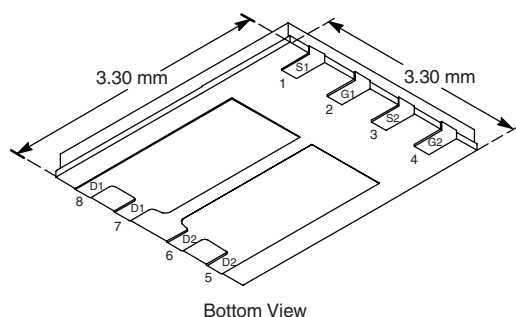


RoHS
COMPLIANT

APPLICATIONS

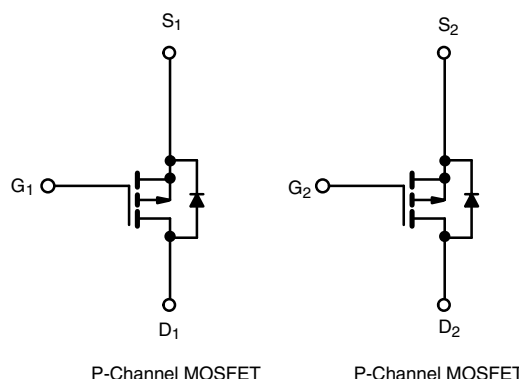
- Portable
- PA Switch
- Battery Switch
- Load Switch

PowerPAK 1212-8



Bottom View

Ordering Information: Si7911DN-T1-E3 (Lead (Pb)-free)
Si7911DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 20		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	- 5.7	- 4.2	A
		- 4.1	- 3.0	
Pulsed Drain Current	I_{DM}	- 20		
Continuous Source Current (Diode Conduction) ^a	I_S	- 2.1	- 1.1	
Maximum Power Dissipation ^a	P_D	2.5	1.3	W
		1.3	0.85	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations ^{b, c}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	40	50	°C/W
		75	94	
Maximum Junction-to-Case	R_{thJC}	5.6	7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

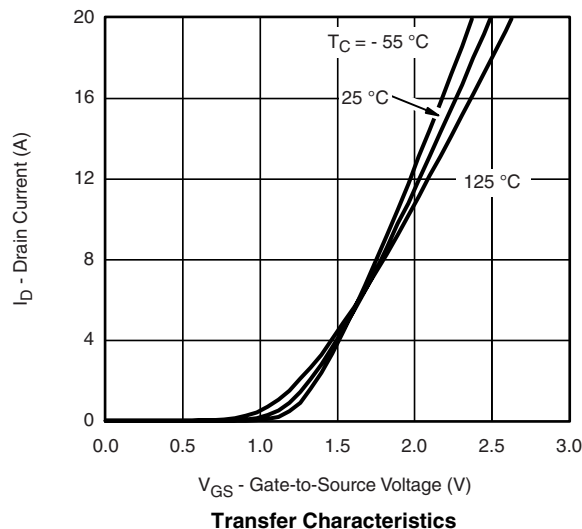
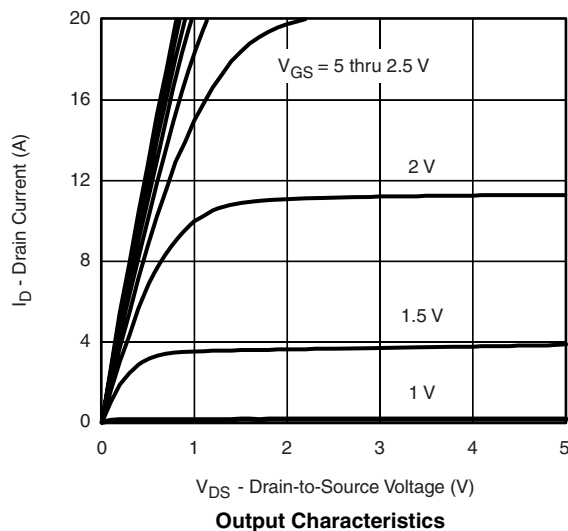
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.40		-1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -5.7\ \text{A}$		0.040	0.051	Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -5.0\ \text{A}$		0.054	0.067	
		$V_{GS} = -1.8\ \text{V}$, $I_D = -1.1\ \text{A}$		0.075	0.094	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -6\ \text{V}$, $I_D = -5.7\ \text{A}$		14		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.3\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -5.7\ \text{A}$		9.5	15	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			2.5		
Gate Resistance	R_g			7.2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -4.5\ \text{V}$, $R_G = 6\ \Omega$		20	30	ns
Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			40	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		25	50	

Notes:

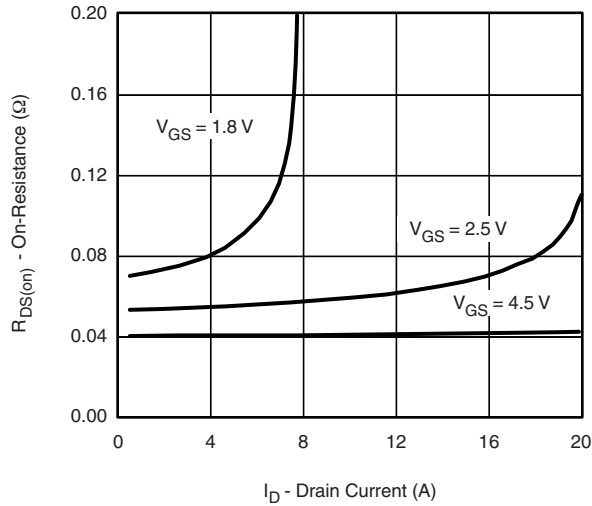
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

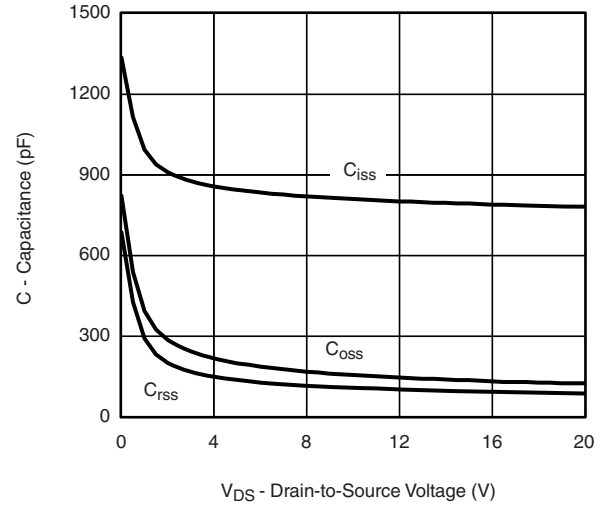
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted

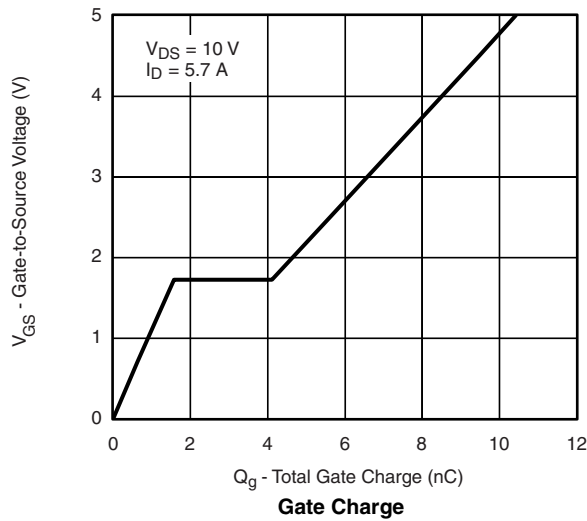
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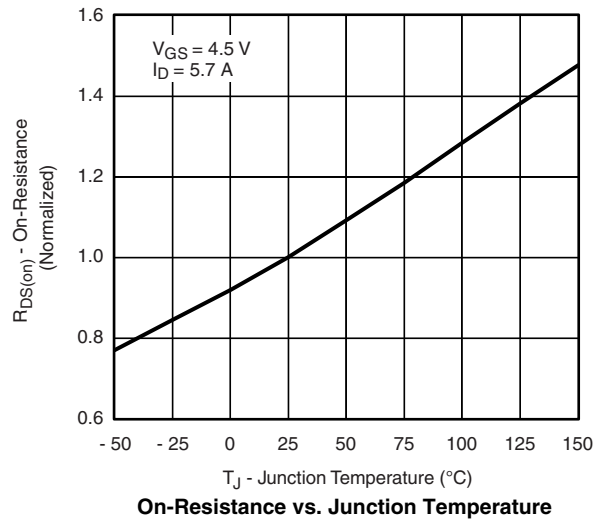
On-Resistance vs. Drain Current



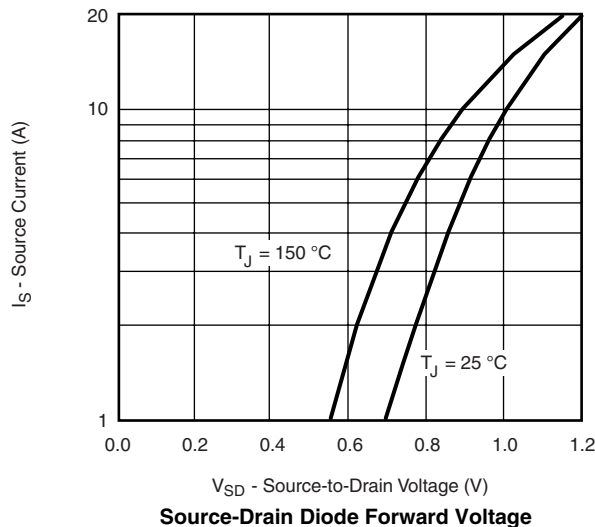
Capacitance



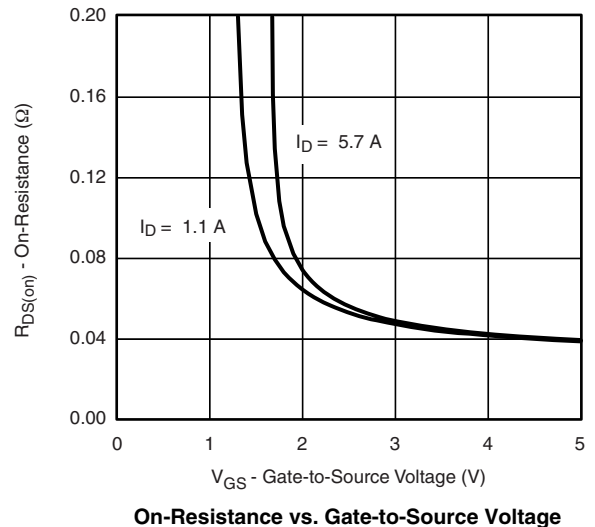
Gate Charge



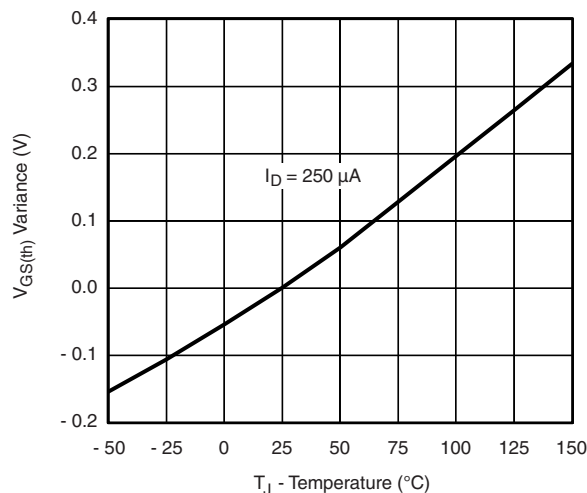
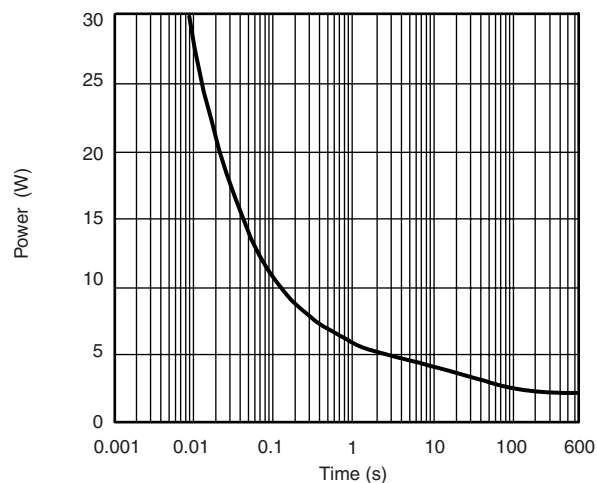
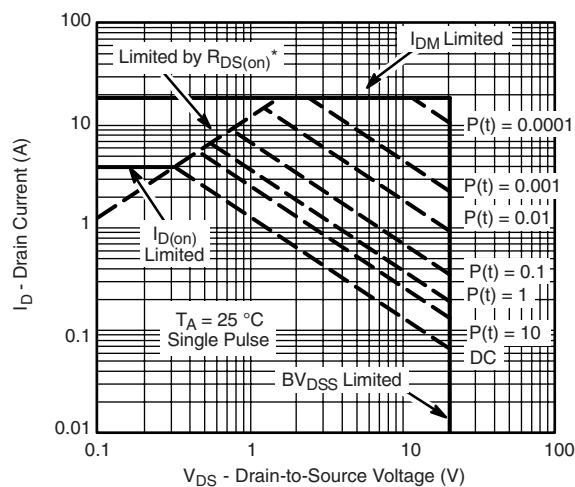
On-Resistance vs. Junction Temperature



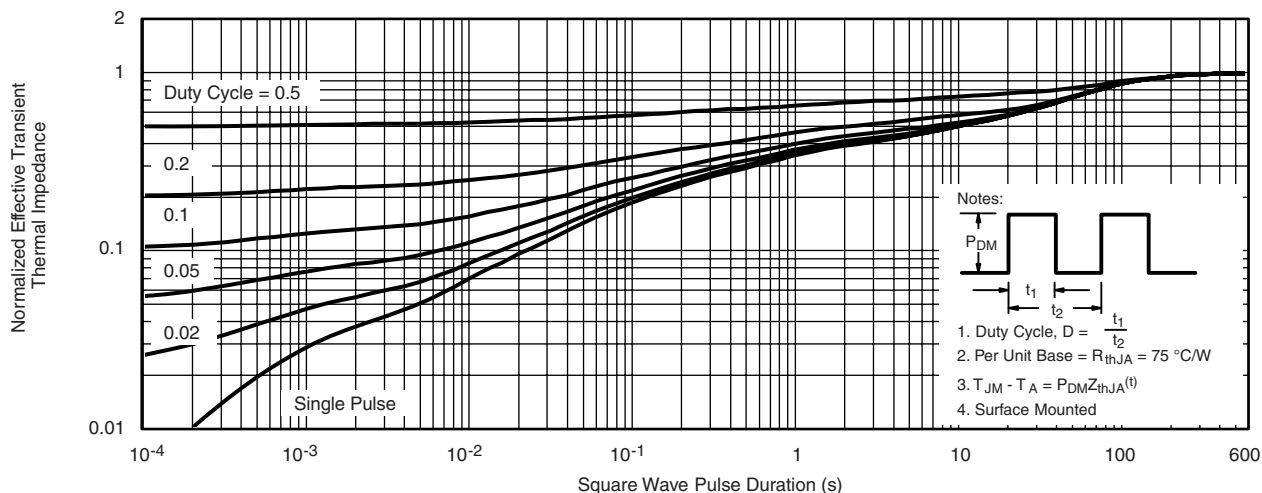
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

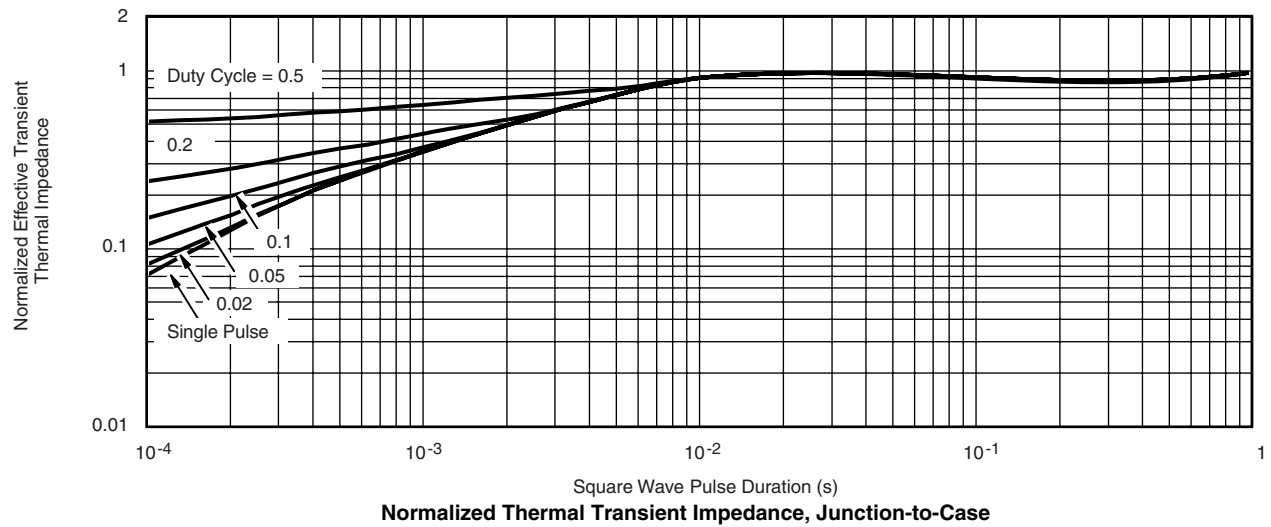
TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Threshold Voltage

Single Pulse Power, Junction-to-Ambient


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



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