

Dual P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 12	0.042 at $V_{GS} = - 4.5$ V	- 6.5
	0.058 at $V_{GS} = - 2.5$ V	- 5.5
	0.082 at $V_{GS} = - 1.8$ V	- 1.2

FEATURES

- Halogen-free Option Available
- TrenchFET® Power MOSFET: 1.8 V Rated

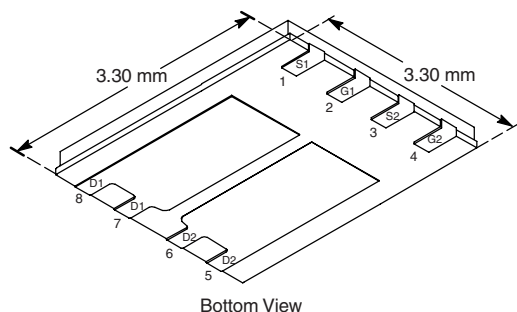
APPLICATIONS

- Load Switch
- PA Switch
- Battery Switch
- Bi-Directional Switch

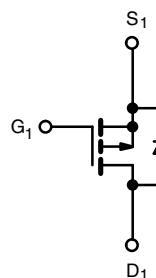


RoHS
COMPLIANT

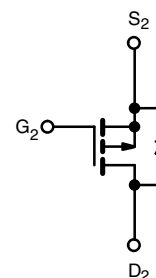
PowerPAK 1212-8



Ordering Information: Si7925DN-T1-E3 (Lead (Pb)-free)
Si7925DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 12		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	- 6.5	- 4.8	A
	T _A = 85 °C		- 4.7	- 3.4	
Pulsed Drain Current		I _{DM}	- 20		
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.1	- 1.1	W
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.5	1.3	
	T _A = 85 °C		1.5	0.69	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	40	$^\circ\text{C/W}$
		Steady State	75	
Maximum Junction-to-Case	R_{thJC}	5.6	7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

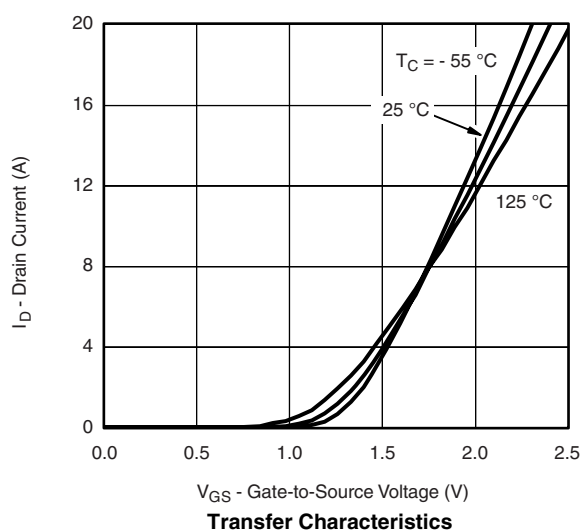
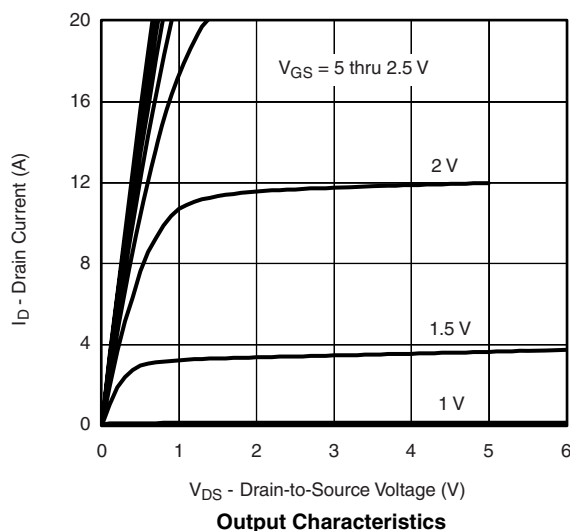
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	- 0.40		- 1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}$, $V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -12\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$			- 5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	- 20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -6.5\text{ A}$		0.033	0.042	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -5.5\text{ A}$		0.046	0.058	
		$V_{GS} = -1.8\text{ V}$, $I_D = -1.2\text{ A}$		0.065	0.082	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -6\text{ V}$, $I_D = -6.5\text{ A}$		19		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.1\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.8	- 1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -6.5\text{ A}$		11	12	nC
Gate-Source Charge	Q_{gs}			1.7		
Gate-Drain Charge	Q_{gd}			2.8		
Gate Resistance	R_g			8.2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}$, $R_L = 6\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_G = 6\text{ }\Omega$		20	30	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			50	75	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		41	80	

Notes:

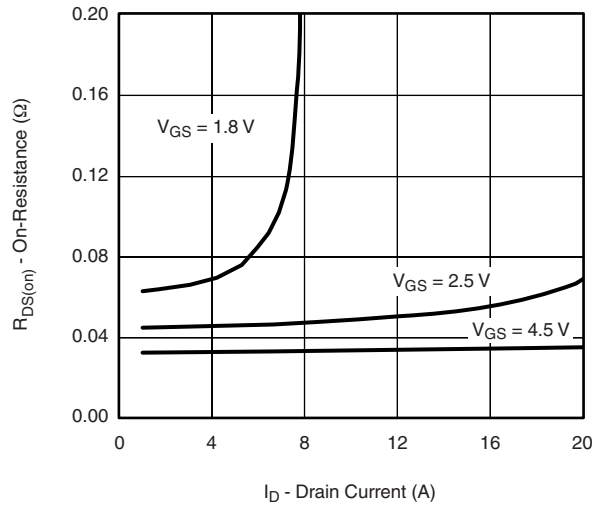
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

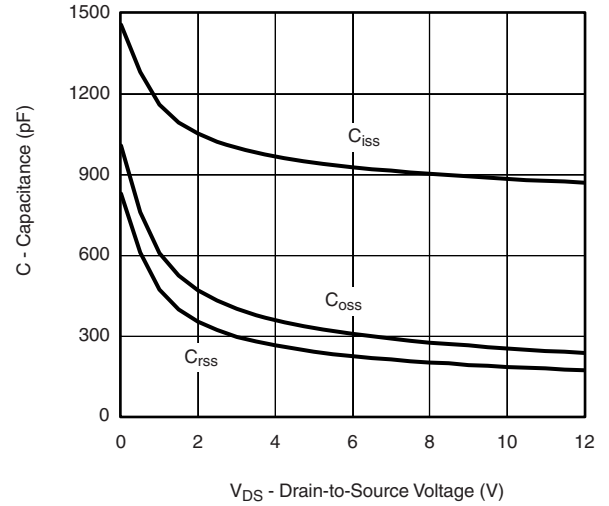
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^{\circ}\text{C}$, unless otherwise noted

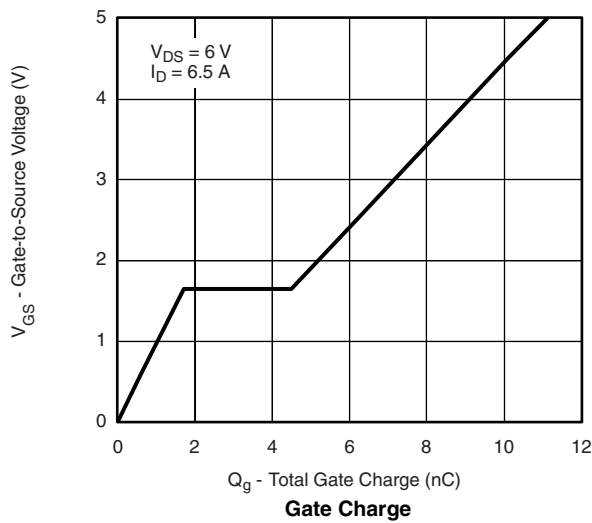
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



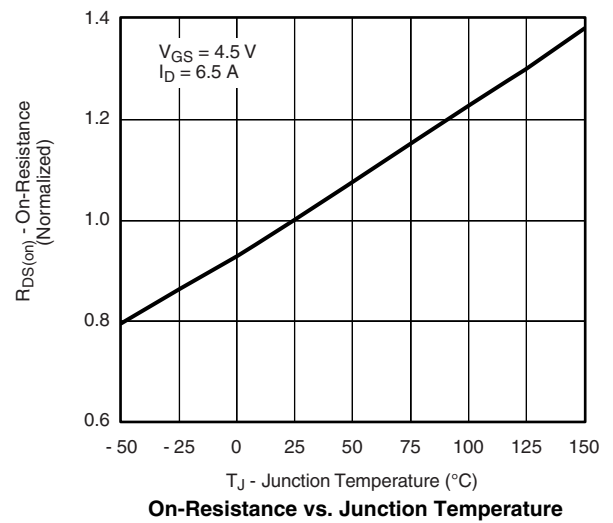
On-Resistance vs. Drain Current



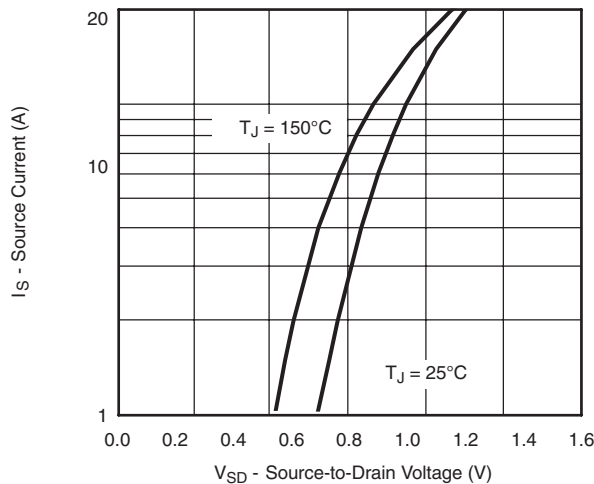
Capacitance



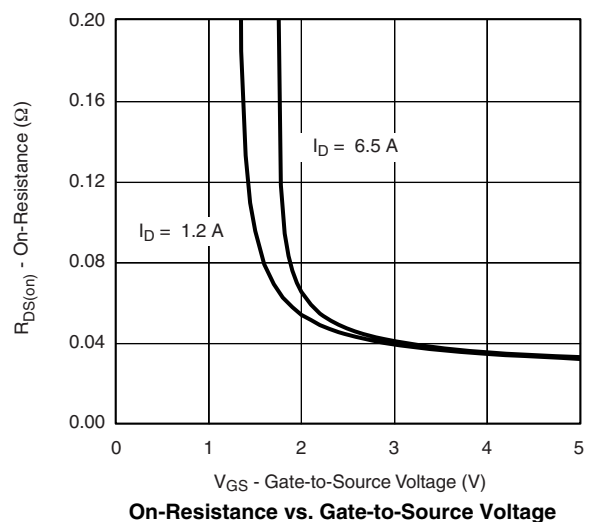
Gate Charge



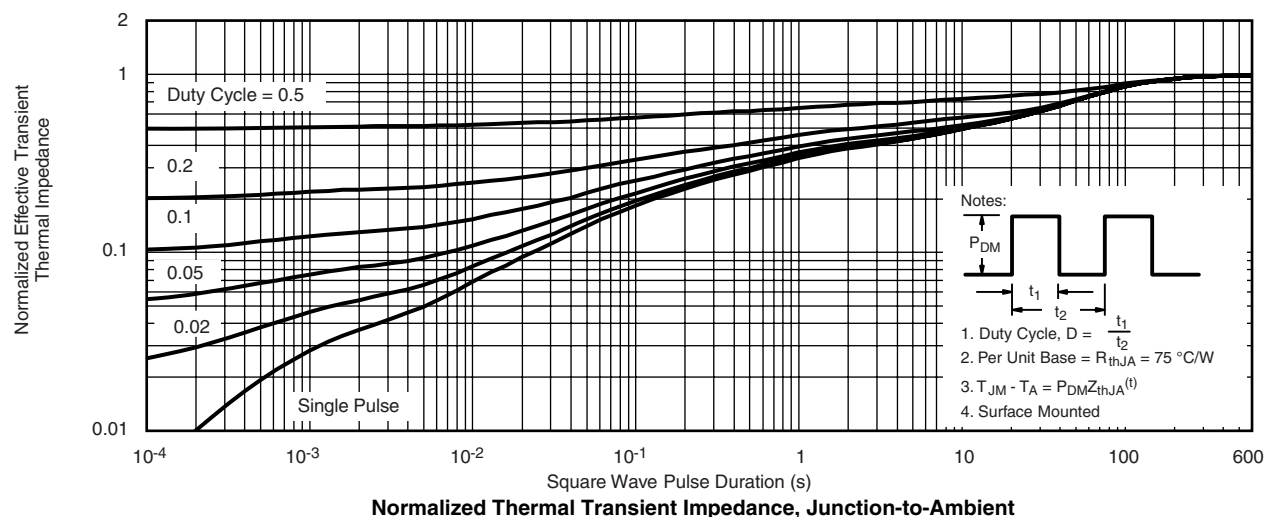
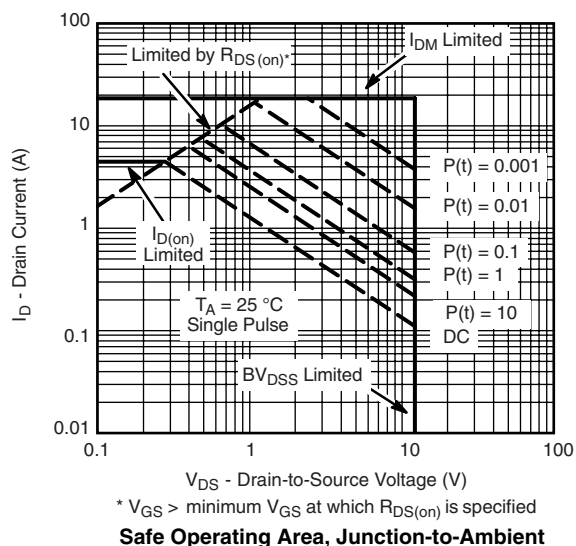
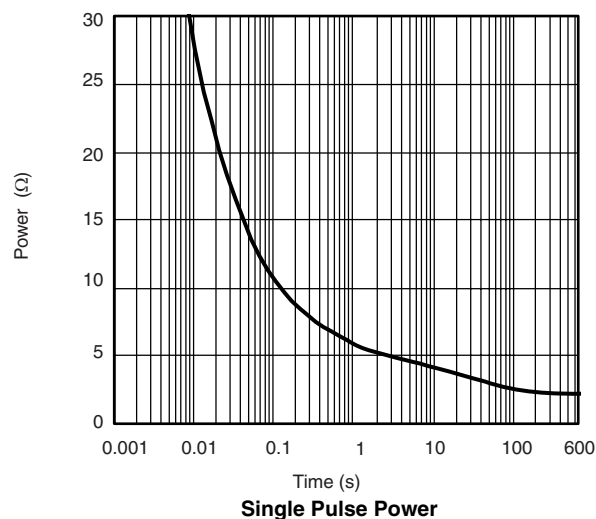
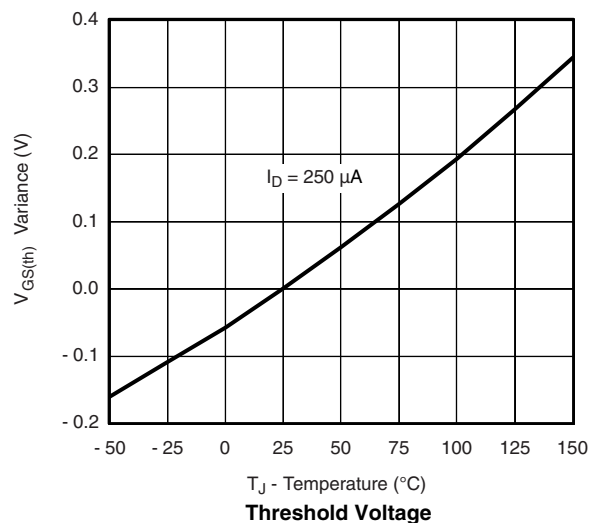
On-Resistance vs. Junction Temperature



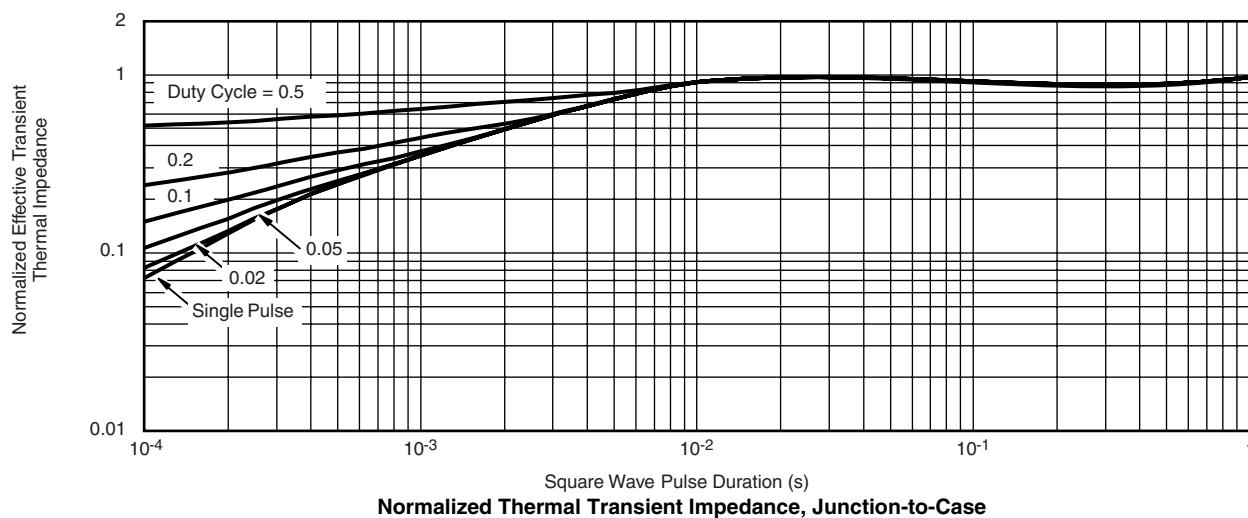
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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