

Dual N-Channel 150-V (D-S) MOSFET

| PRODUCT SUMMARY | | |
|---------------------|---------------------------------|--------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) |
| 150 | 0.150 at V _{GS} = 10 V | 3.3 |
| | 0.168 at V _{GS} = 6 V | 3.1 |

FEATURES

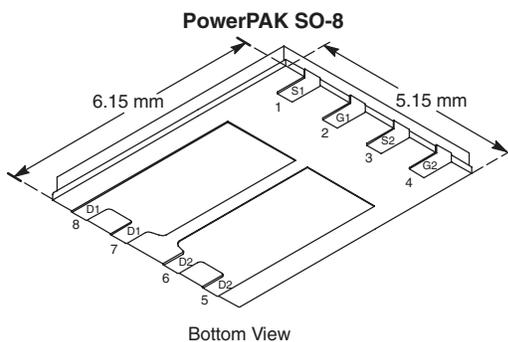
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFETs
- New Low Thermal Resistance PowerPAK[®] Package
- Dual MOSFET for Space Savings
- PWM Optimized for Fast Switching
- Avalanche Rated



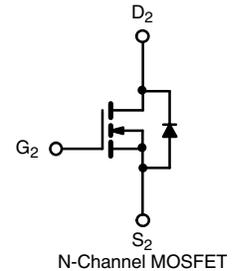
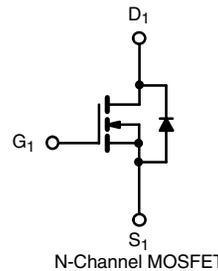
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Primary Side Switch



Ordering Information: Si7946DP-T1-E3 (Lead (Pb)-free)
Si7946DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | | |
|---|-----------------------------------|------------------------|--------------|------|---|
| Parameter | Symbol | 10 s | Steady State | Unit | |
| Drain-Source Voltage | V _{DS} | 150 | | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | | |
| Continuous Drain Current (T _J = 150 °C) ^a | I _D | T _A = 25 °C | 3.3 | 2.1 | A |
| | | T _A = 70 °C | 2.6 | 1.7 | |
| Pulsed Drain Current | I _{DM} | 10 | | | |
| Continuous Source Current (Diode Conduction) ^a | I _S | 2.9 | 1.2 | | |
| Single Avalanche Current | L = 0.1 mH | I _{AS} | 9 | | |
| Single Avalanche Energy | E _{AS} | 4 | | mJ | |
| Maximum Power Dissipation ^a | P _D | T _A = 25 °C | 3.5 | 1.4 | W |
| | | T _A = 70 °C | 2.2 | 0.9 | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | | °C | |
| Soldering Recommendations (Peak Temperature) ^{b, c} | | 260 | | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|-------------------|--------------|---------|------|------|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^a | R _{thJA} | t ≤ 10 s | 26 | 35 | °C/W |
| | | Steady State | 60 | 85 | |
| Maximum Junction-to-Case (Drain) | R _{thJC} | 3.2 | 4.2 | | |

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



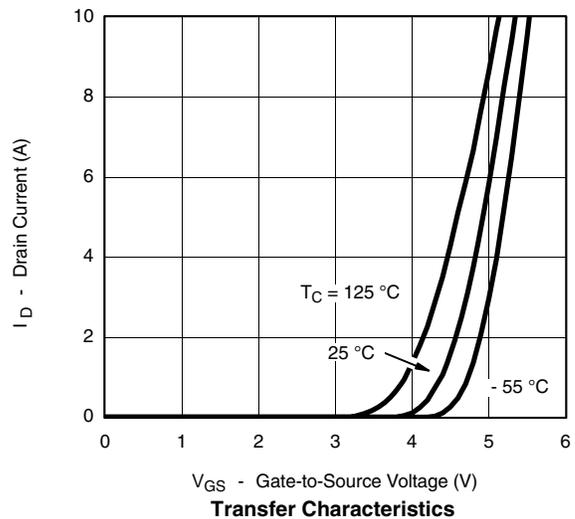
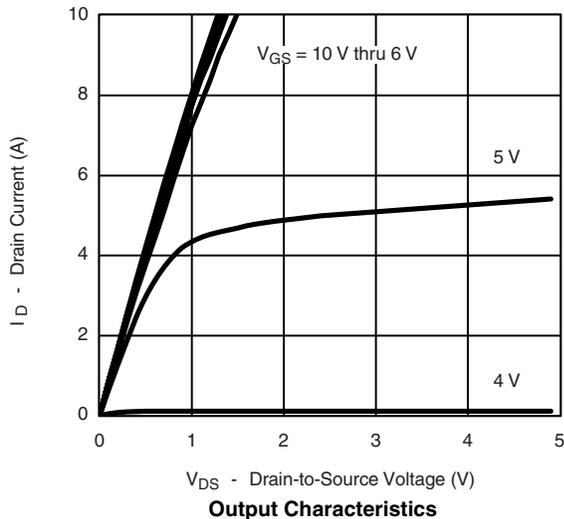
| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|--|--------------|--|------|-------|-----------|---------------|
| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2 | | 4.0 | V |
| Gate-Body Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$ | | | 5 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$ | 10 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 3.3\text{ A}$ | | 0.124 | 0.150 | Ω |
| | | $V_{GS} = 6\text{ V}, I_D = 3.1\text{ A}$ | | 0.137 | 0.168 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 3.3\text{ A}$ | | 9 | | S |
| Diode Forward Voltage ^a | V_{SD} | $I_S = 2.9\text{ A}, V_{GS} = 0\text{ V}$ | | 0.87 | 1.2 | V |
| Dynamic^b | | | | | | |
| Total Gate Charge | Q_g | $V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 3.3\text{ A}$ | | 12.6 | 20 | nC |
| Gate-Source Charge | Q_{gs} | | | 2.8 | | |
| Gate-Drain Charge | Q_{gd} | | | 4.5 | | |
| Gate Resistance | R_g | $f = 1\text{ MHz}$ | | 3.5 | | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 75\text{ V}, R_L = 75\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$ | | 11 | 20 | ns |
| Rise Time | t_r | | | 15 | 25 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 30 | 45 | |
| Fall Time | t_f | | | 20 | 30 | |
| Source-Drain Reverse Recovery Time | t_{rr} | $I_F = 2.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$ | | 62 | 100 | |

Notes:

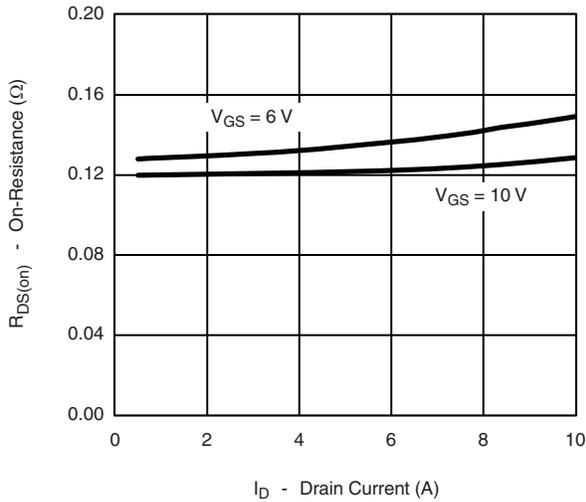
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

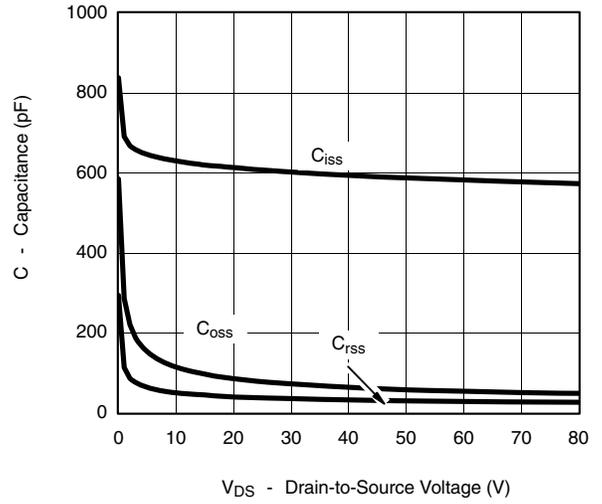
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



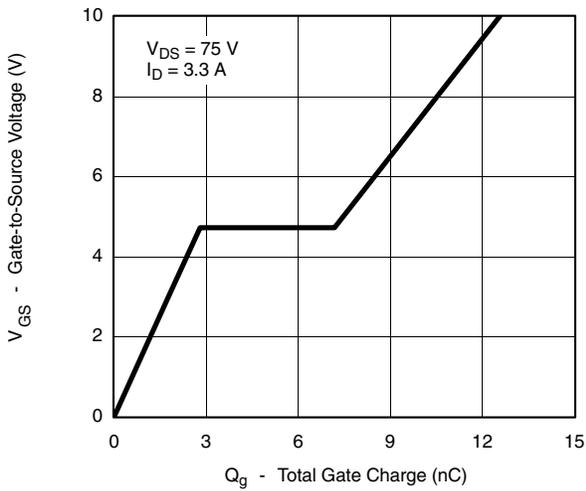
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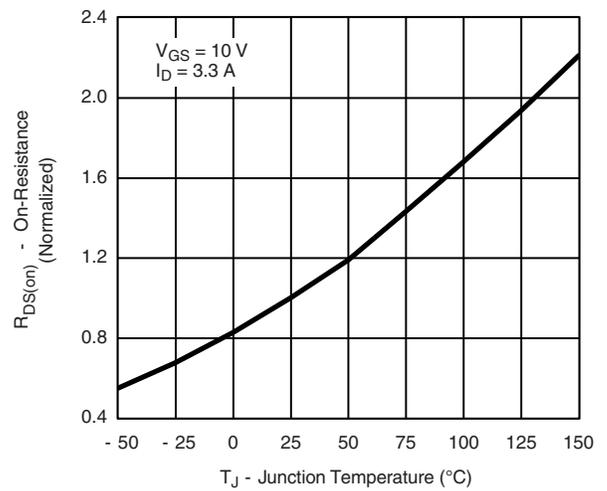
On-Resistance vs. Drain Current



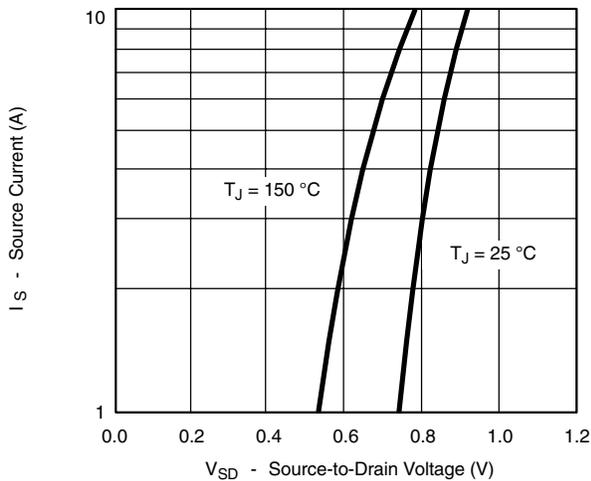
Capacitance



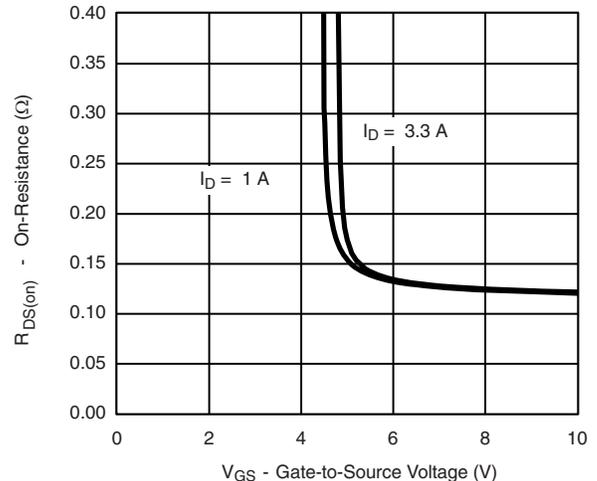
Gate Charge



On-Resistance vs. Junction Temperature

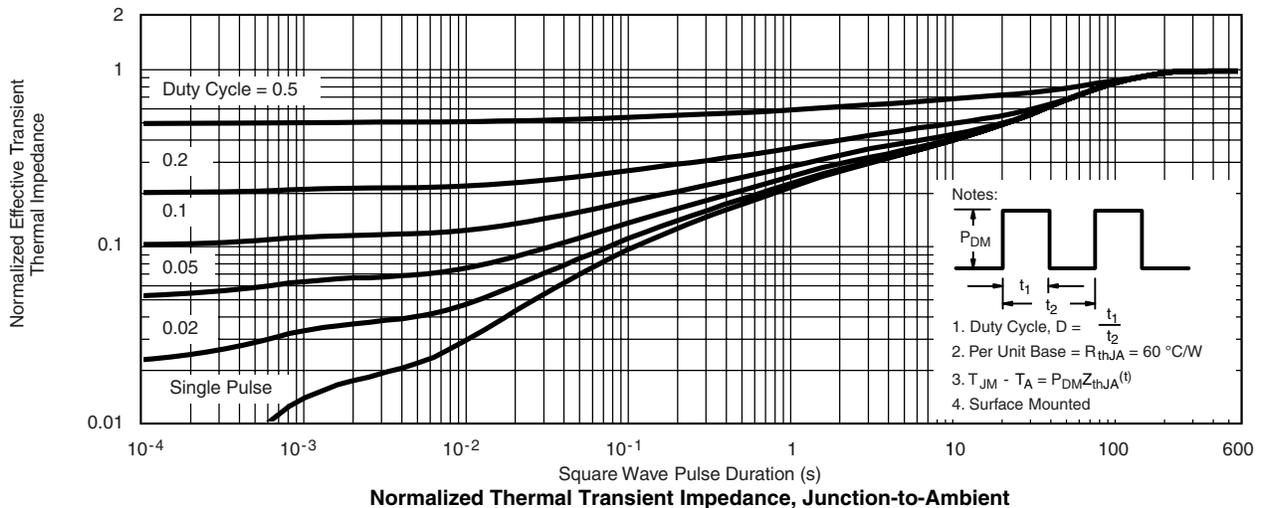
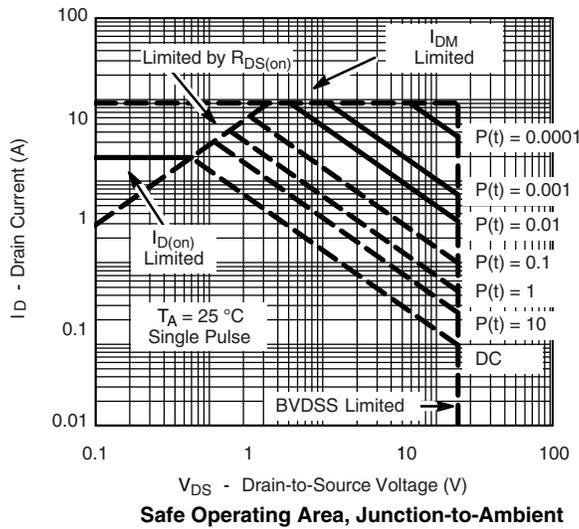
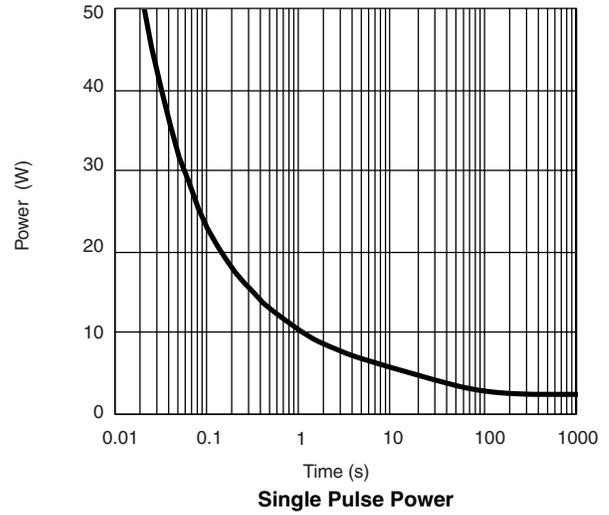
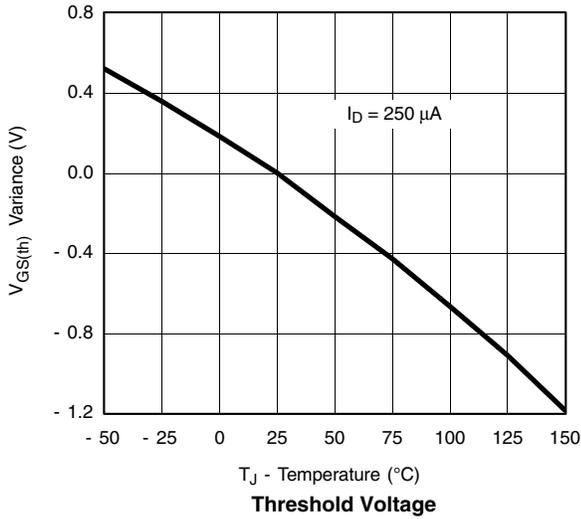


Source-Drain Diode Forward Voltage

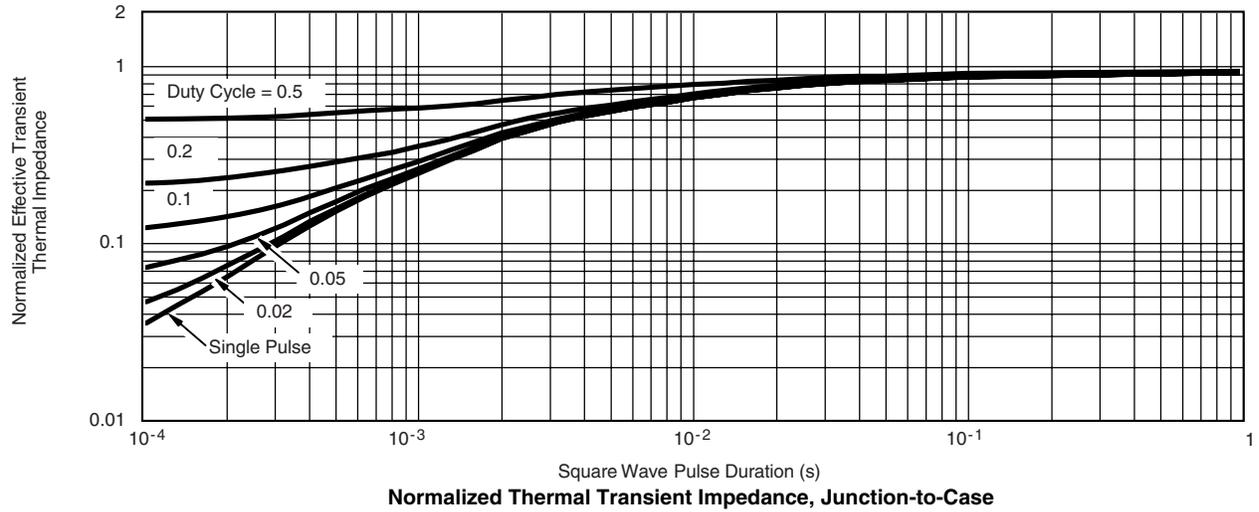


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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