

Dual N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY

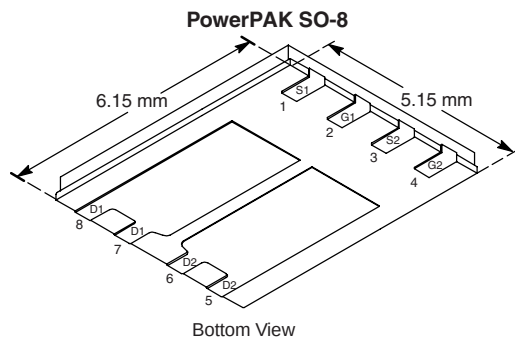
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
60	0.023 at $V_{GS} = 10$ V	9.6	43

FEATURES

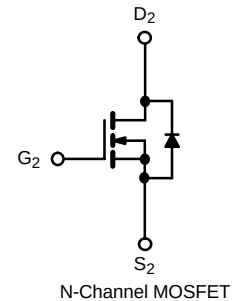
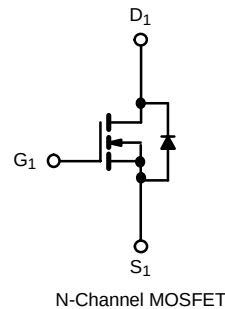
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings
- 100 % R_g Tested
- High Threshold Voltage at High Temperature



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si7964DP-T1-E3 (Lead (Pb)-free)
Si7964DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	60		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	9.6	6.1	A
		7.7	4.9	
Pulsed Drain Current	I_{DM}	40		
Continuous Source Current (Diode Conduction) ^a	I_S	2.9	1.2	
Single Avalanche Current	I_{AS}	25		
Single Avalanche Energy	E_{AS}	31		mJ
Maximum Power Dissipation ^a	P_D	3.5	1.4	W
		2.2	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{b, c}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	26	35	$^\circ\text{C/W}$
		60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg273257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3.4		4.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 60\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 9.6\ \text{A}$		0.019	0.023	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 9.6\ \text{A}$		30		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 9.6\ \text{A}$		43	65	nC
Gate-Source Charge	Q_{gs}			15		
Gate-Drain Charge	Q_{gd}			8.5		
Gate Resistance	R_g	$f = 1\ \text{MHz}$	1	2	3	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\ \text{V}$, $R_L = 20\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		20	30	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		35	60	

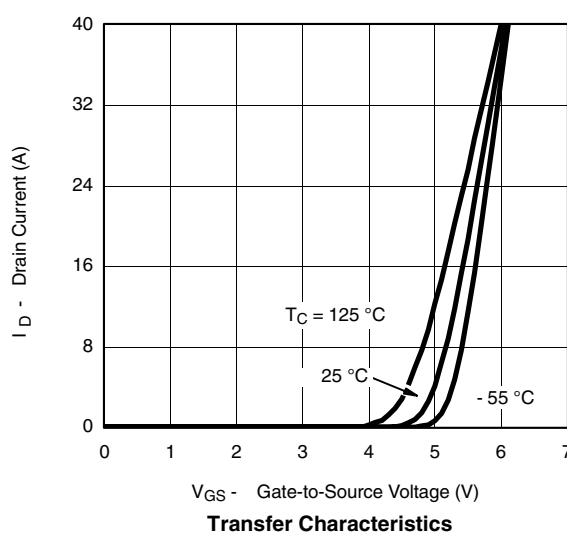
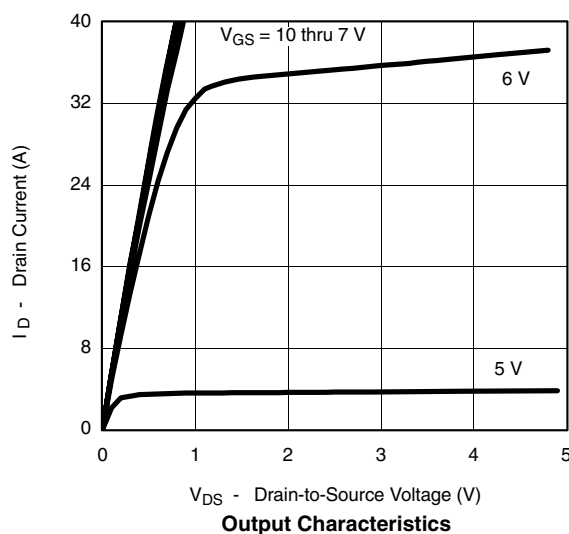
Notes:

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

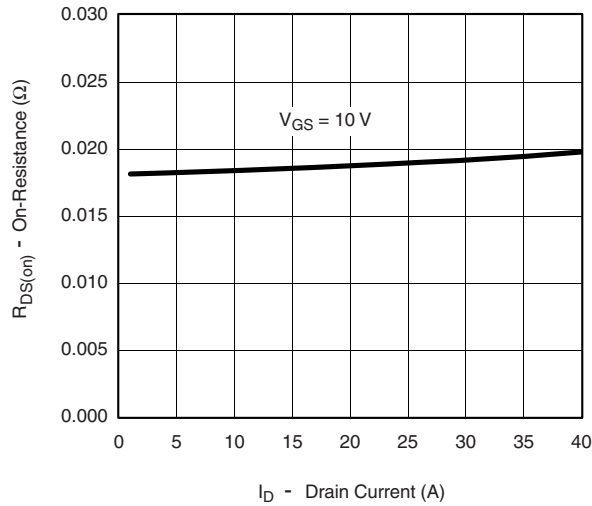
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

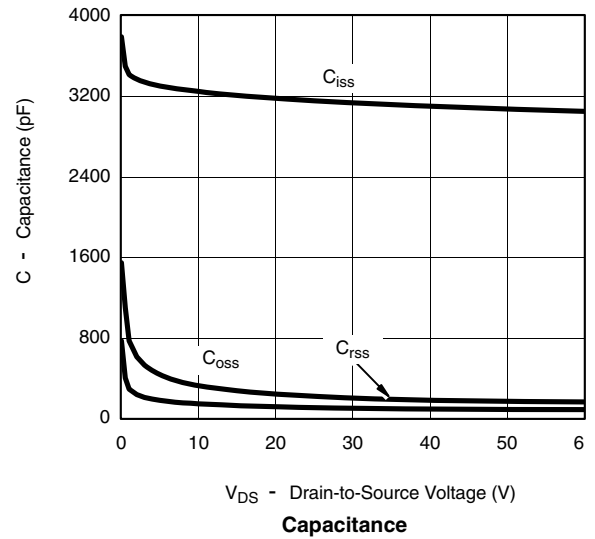
TYPICAL CHARACTERISTICS 25°C , unless otherwise noted



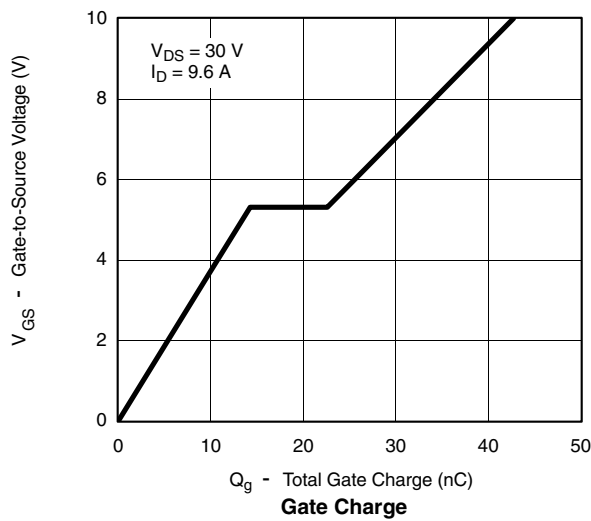
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



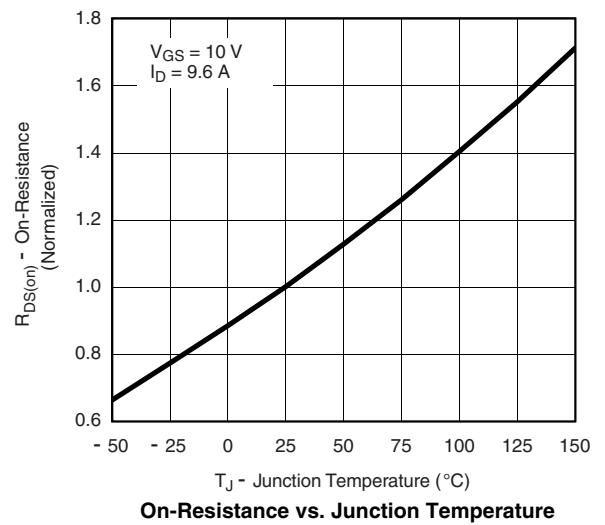
On-Resistance vs. Drain Current



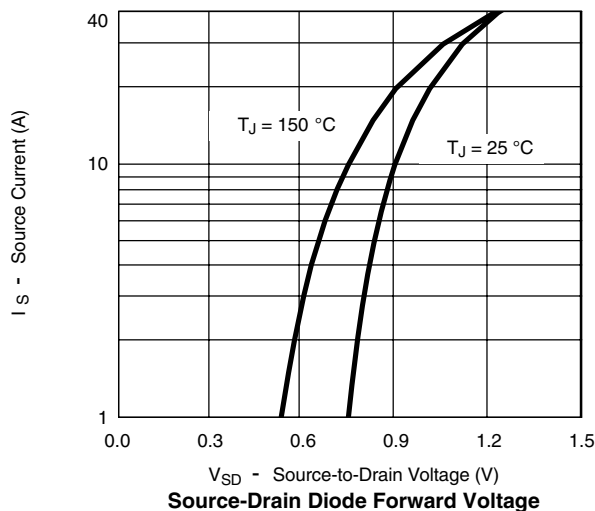
Capacitance



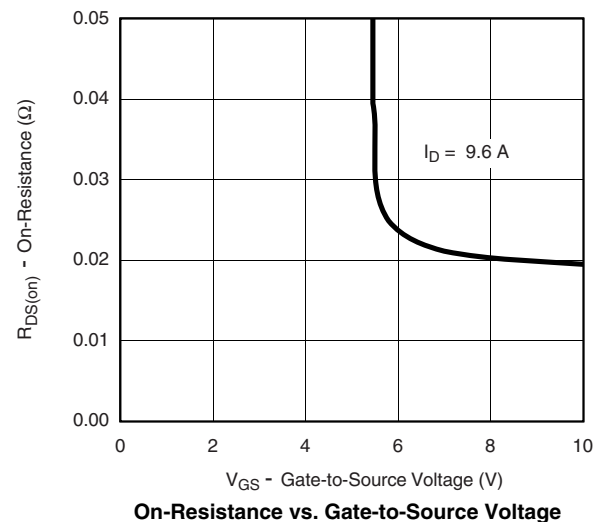
Gate Charge



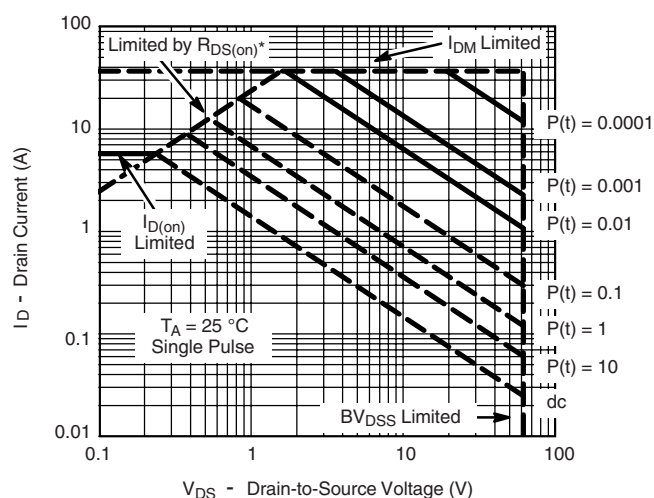
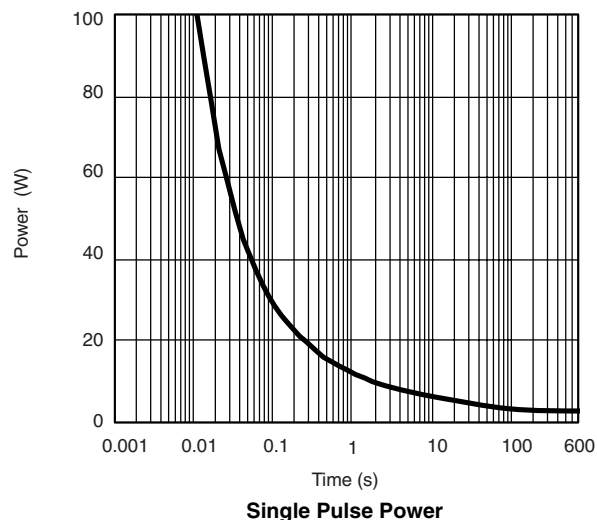
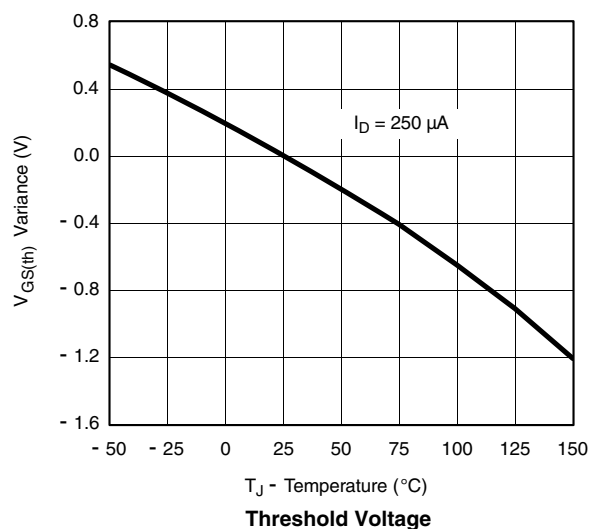
On-Resistance vs. Junction Temperature



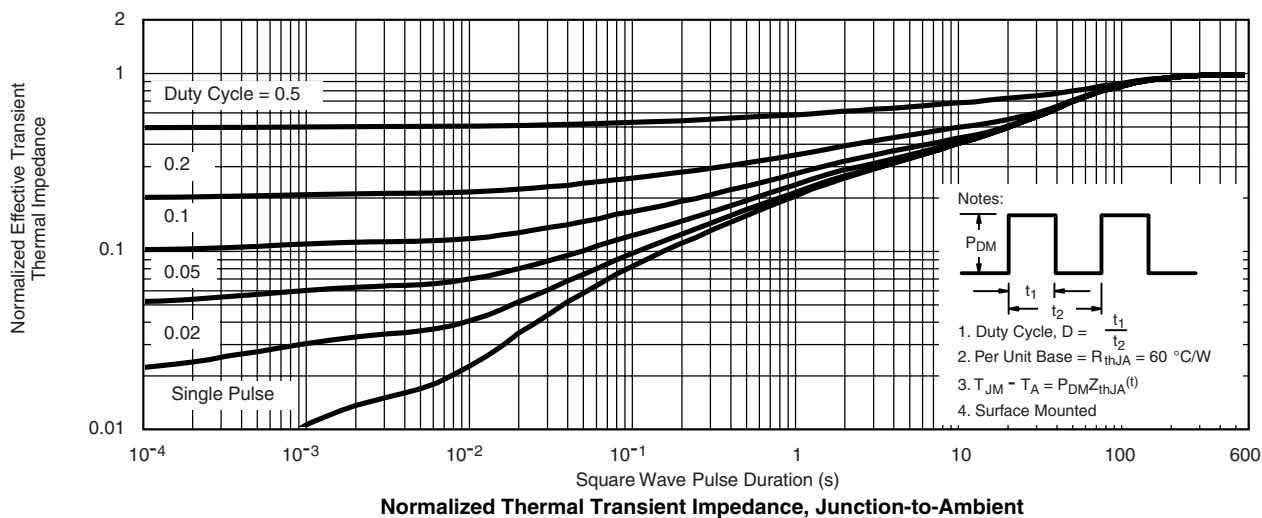
Source-Drain Diode Forward Voltage



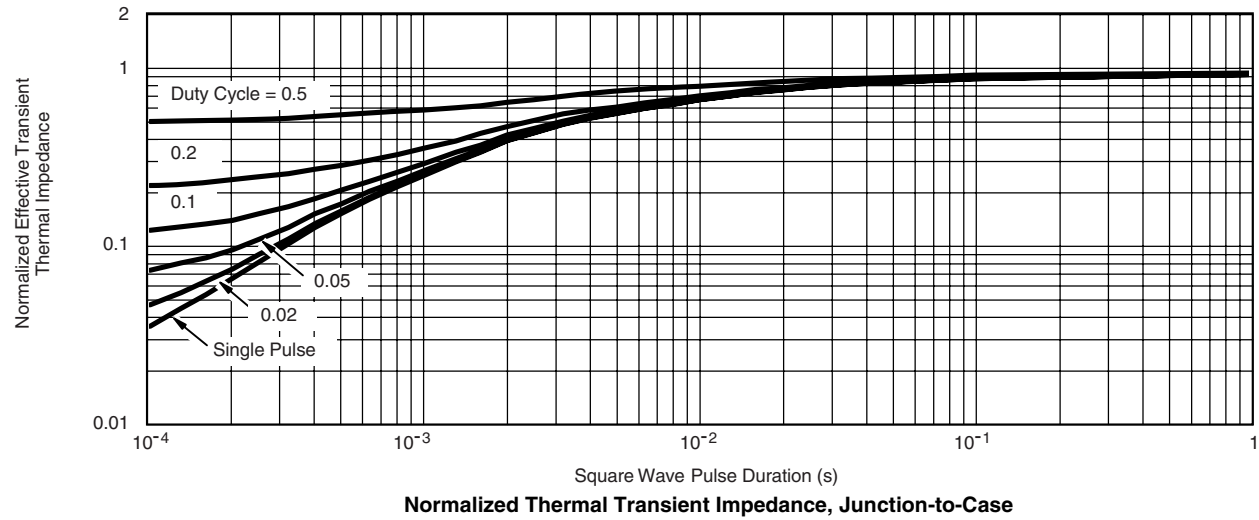
On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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