

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.017 at $V_{GS} = - 4.5$ V	- 12
	0.020 at $V_{GS} = - 2.5$ V	- 11
	0.024 at $V_{GS} = - 1.8$ V	- 10.1

FEATURES

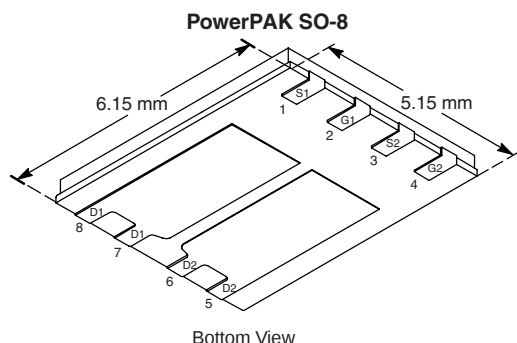
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile



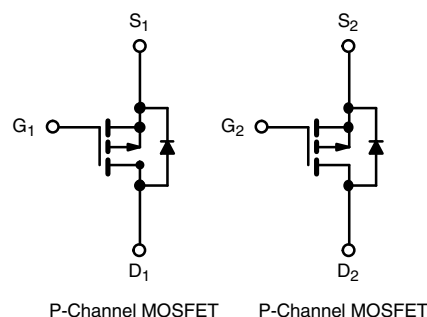
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch



Ordering Information: Si7983DP-T1-E3 (Lead (Pb)-free)
Si7983DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	- 12	- 7.7	A
	T _A = 70 °C		- 9.6	- 6.2	
Pulsed Drain Current		I _{DM}	- 30		
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.9	- 1.2	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.5	1.4	W
	T _A = 70 °C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	26	°C/W
		Steady State	60	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

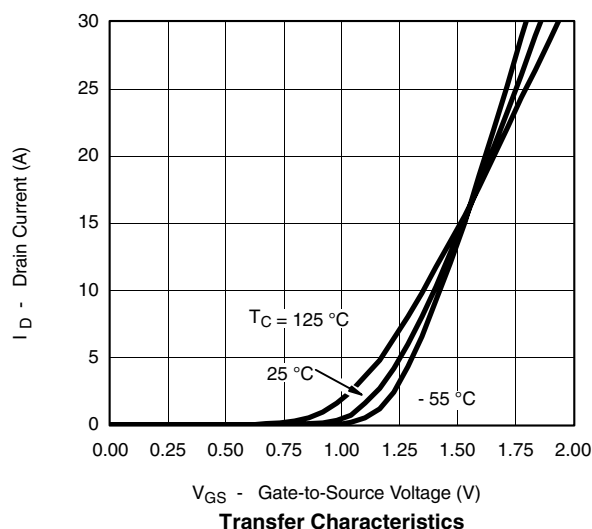
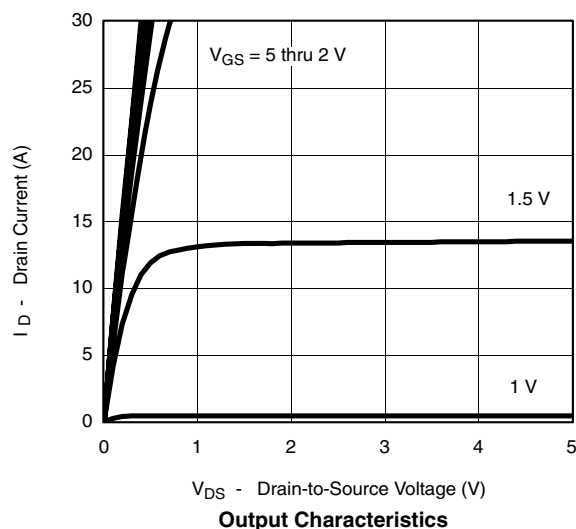
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -600\ \mu\text{A}$	-0.40		-1	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\ \text{V}$, $V_{GS} = -4.5\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\ \text{V}$, $I_D = -12\ \text{A}$		0.014	0.017	Ω
		$V_{GS} = -2.5\ \text{V}$, $I_D = -11\ \text{A}$		0.016	0.020	
		$V_{GS} = -1.8\ \text{V}$, $I_D = -4.1\ \text{A}$		0.020	0.024	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}$, $I_D = -12\ \text{A}$		41		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}$, $V_{GS} = -4.5\ \text{V}$, $I_D = -12\ \text{A}$		49	74	nC
Gate-Source Charge	Q_{gs}			7.2		
Gate-Drain Charge	Q_{gd}			12.1		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		8		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \cong -1\ \text{A}$, $V_{GEN} = -4.5\ \text{V}$, $R_g = 6\ \Omega$		35	55	ns
Rise Time	t_r			60	90	
Turn-Off Delay Time	$t_{d(off)}$			390	585	
Fall Time	t_f			190	285	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.9\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		106	160	

Notes:

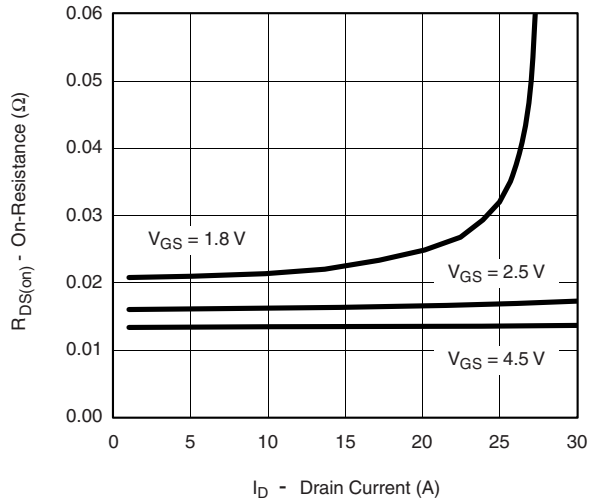
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

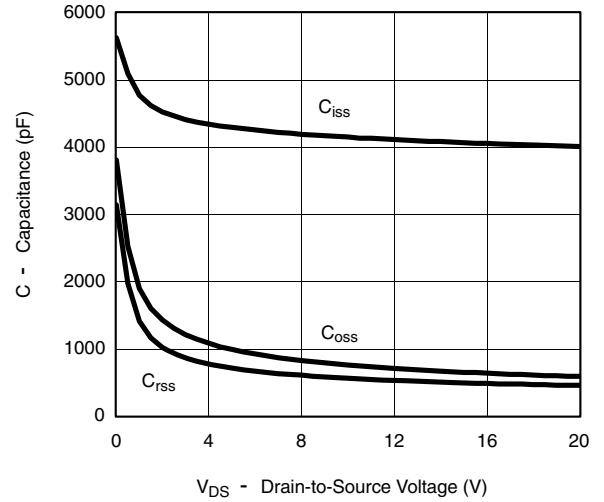
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

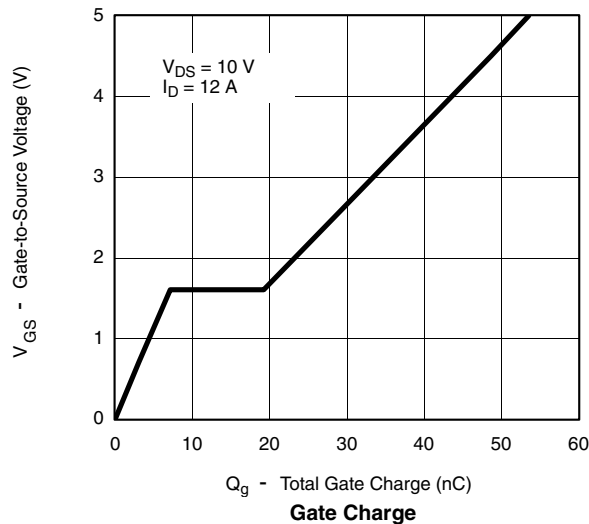
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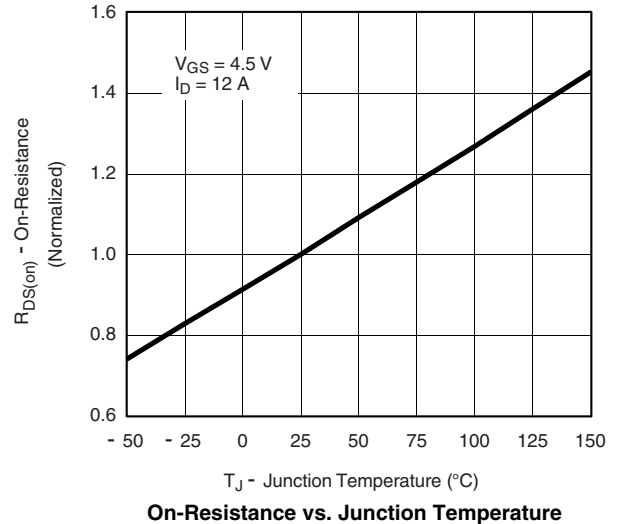
On-Resistance vs. Drain Current



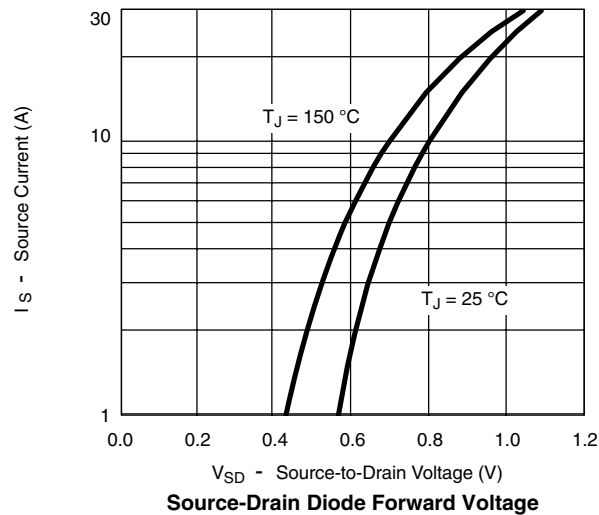
Capacitance



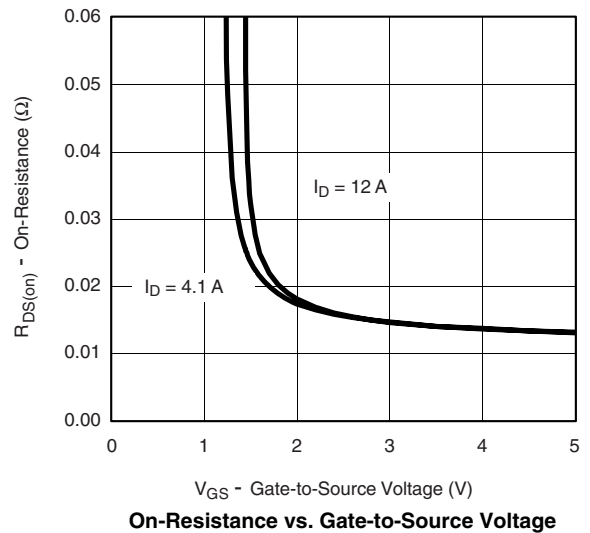
Gate Charge



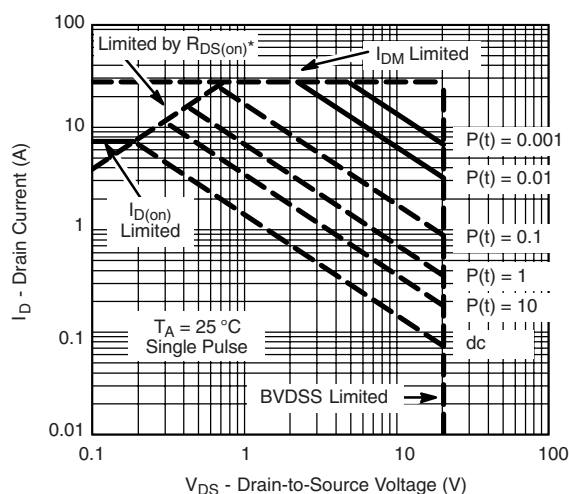
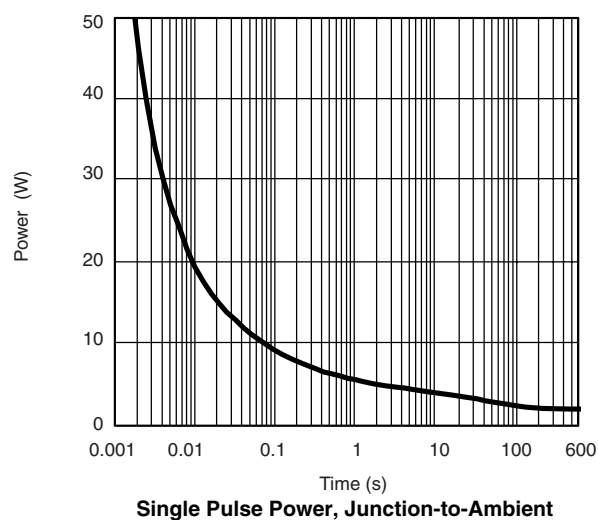
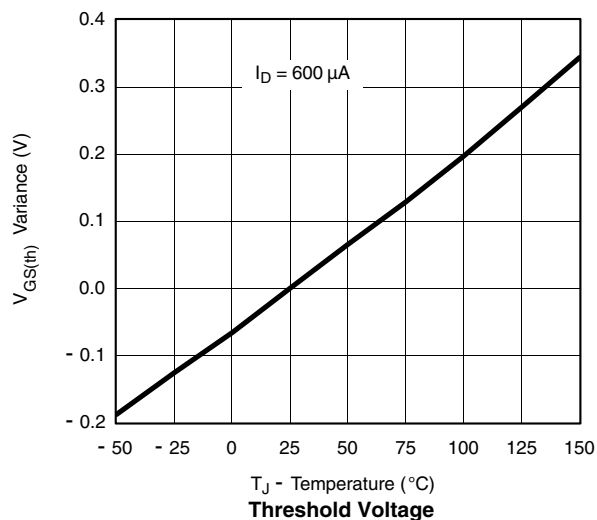
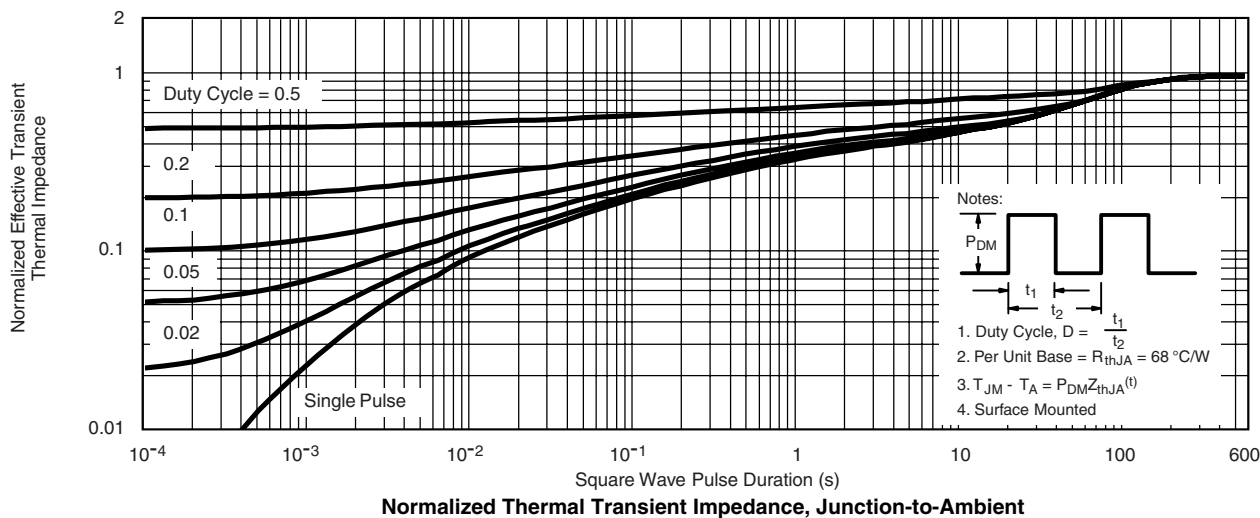
On-Resistance vs. Junction Temperature



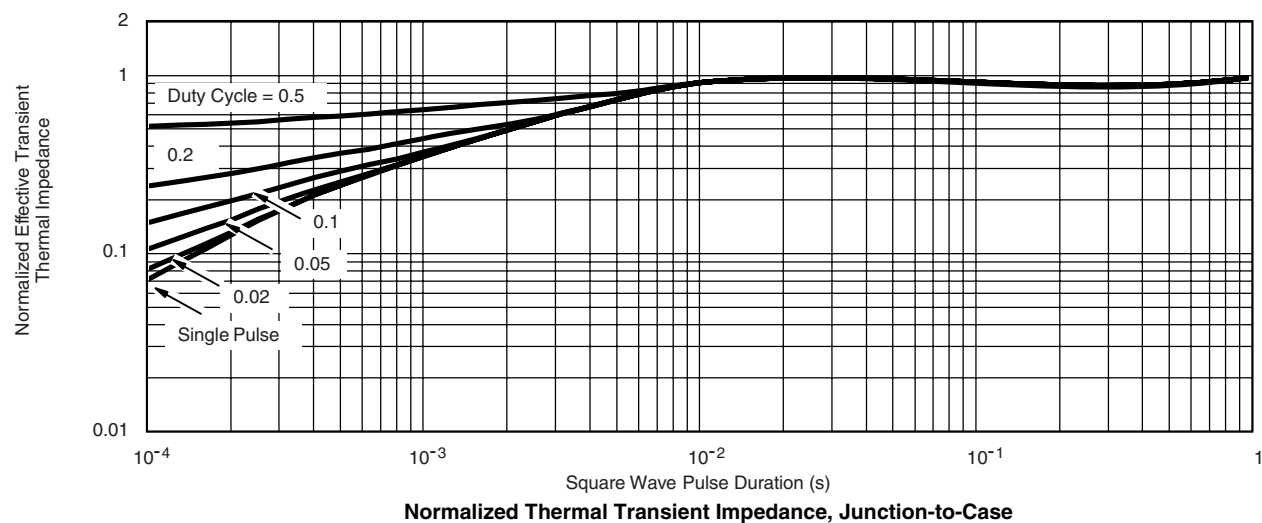
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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