

N-Channel 20-V (D-S) MOSFET

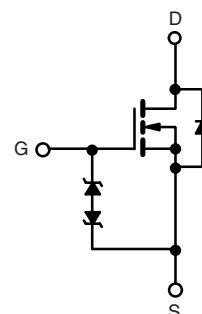
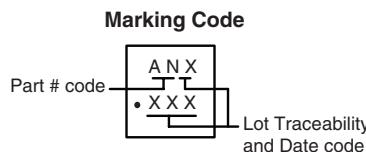
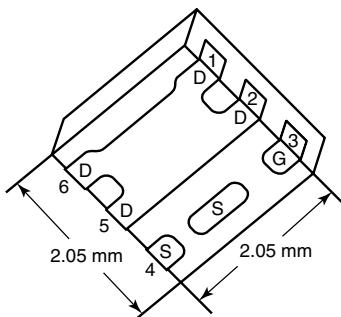
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)^a	Q_g (Typ.)
20	0.046 at $V_{GS} = 4.5$ V	6	3.5 nC
	0.063 at $V_{GS} = 2.5$ V	6	

FEATURES

- Halogen-free According to IEC 61249-2-21
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- Typical ESD Protection 1200 V



PowerPAK SC-70-6L-Single



Ordering Information: SiA438EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	20	V	
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150$ °C)	I_D	6^a	A	
		6^a		
		5.7 ^{b, c}		
		4.5 ^{b, c}		
Pulsed Drain Current	I_{DM}	15		
Continuous Source-Drain Diode Current	I_S	6^a	W	
		1.75 ^{b, c}		
Maximum Power Dissipation	P_D	11.4	W	
		7.3		
		2.4 ^{b, c}		
		1.5 ^{b, c}		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	41	52
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	9	11 °C/W

Notes:

- Package limited
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$ s.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 90 °C/W.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

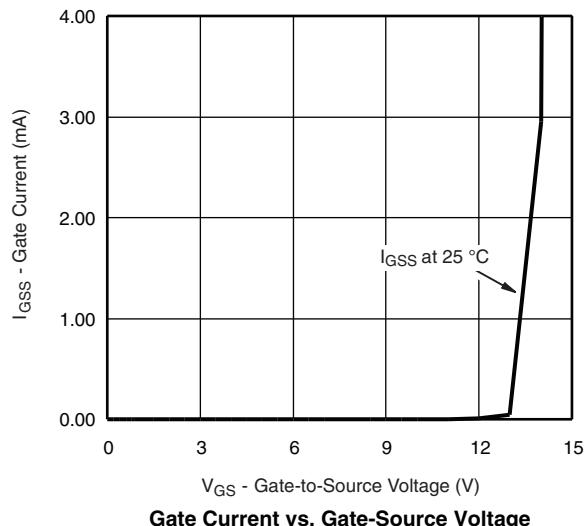
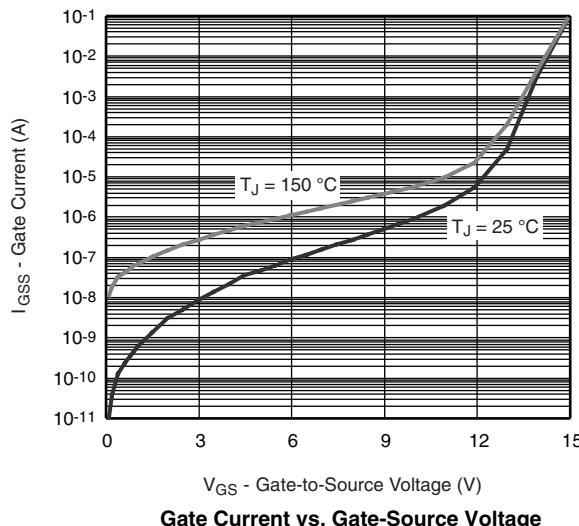
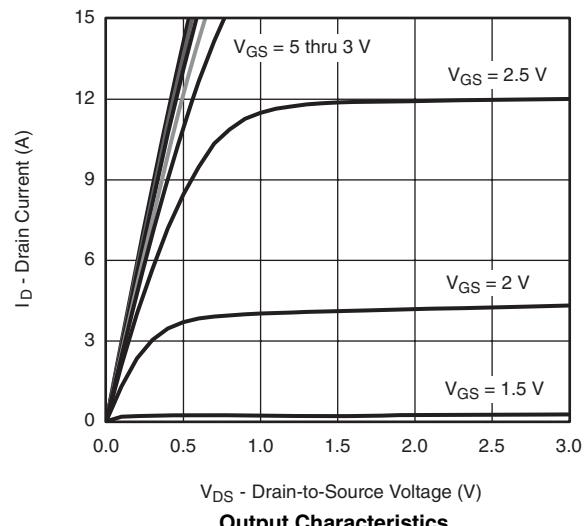
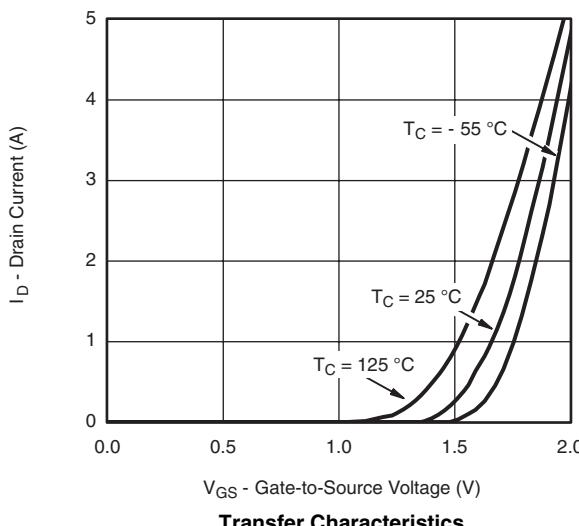
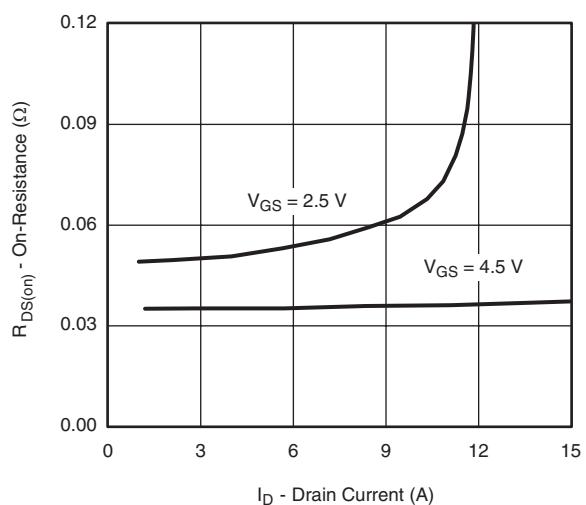
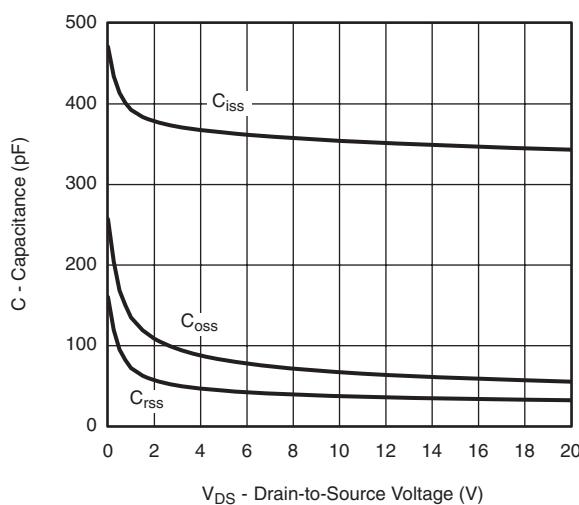
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		23		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 3.3		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.6		1.4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 70	μA
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$		0.037	0.046	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 3.3 \text{ A}$		0.051	0.063	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 3.9 \text{ A}$		14		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		350		pF
Output Capacitance	C_{oss}			63		
Reverse Transfer Capacitance	C_{rss}			37		
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5.1 \text{ A}$		7.5	12	nC
Gate-Source Charge	Q_{gs}			3.5	5.5	
Gate-Drain Charge	Q_{gd}			0.95		
Gate Resistance	R_g			0.75		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}, R_L = 2.4 \Omega$ $I_D \geq 4.1 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		3.5		Ω
Rise Time	t_r			10	15	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			12	20	
Fall Time	t_f			18	30	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}, R_L = 2.4 \Omega$ $I_D \geq 4.1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		12	20	ns
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(\text{off})}$			12	20	
Fall Time	t_f			15	25	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			6	A
Pulse Diode Forward Current	I_{SM}				15	
Body Diode Voltage	V_{SD}	$I_S = 4.1 \text{ A}, V_{GS} = 0 \text{ V}$ $I_F = 4.1 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}			15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			8	20	nC
Reverse Recovery Fall Time	t_a			8		ns
Reverse Recovery Rise Time	t_b			7		

Notes:

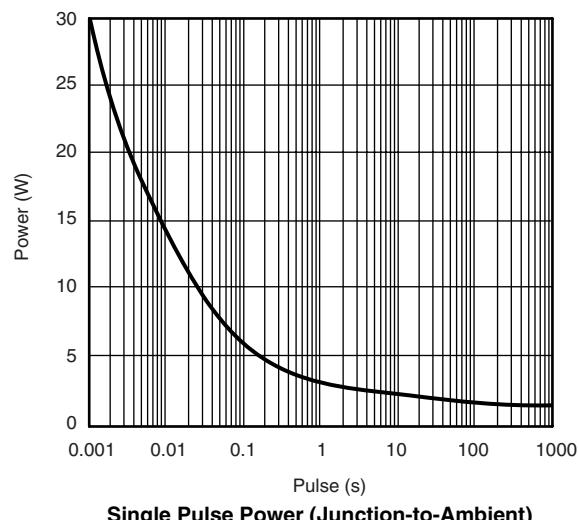
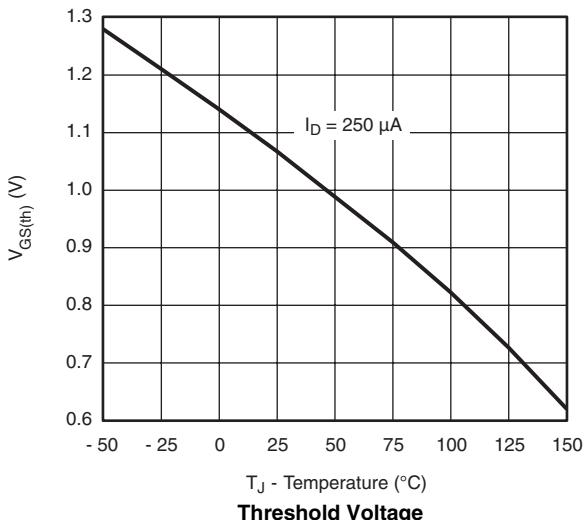
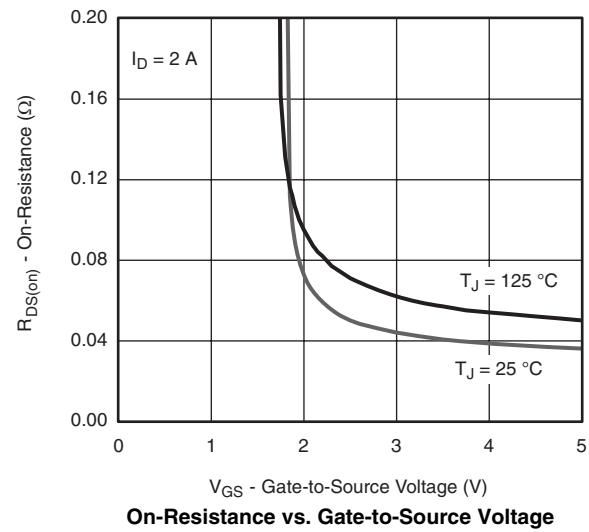
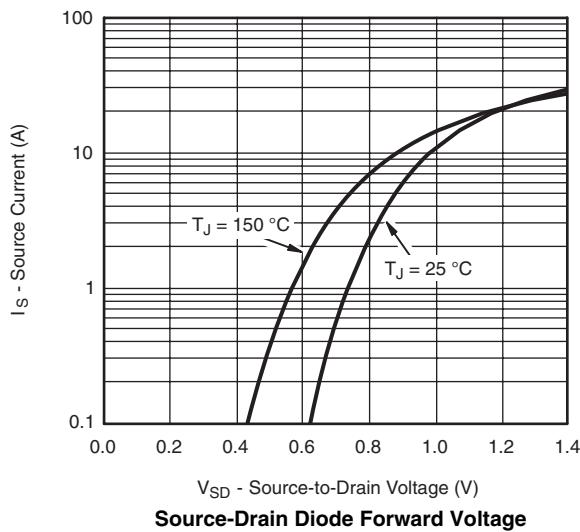
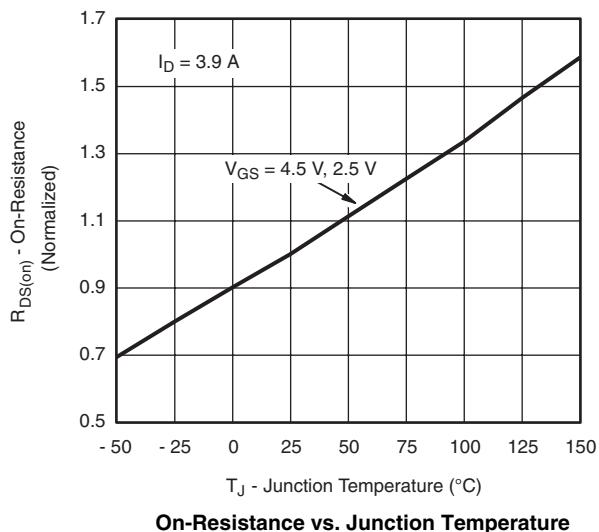
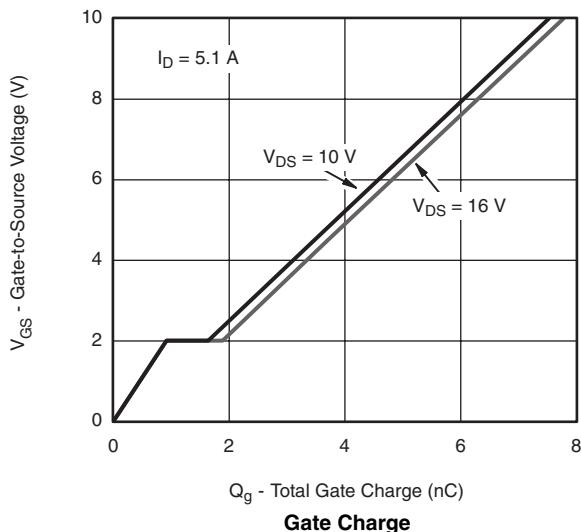
a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

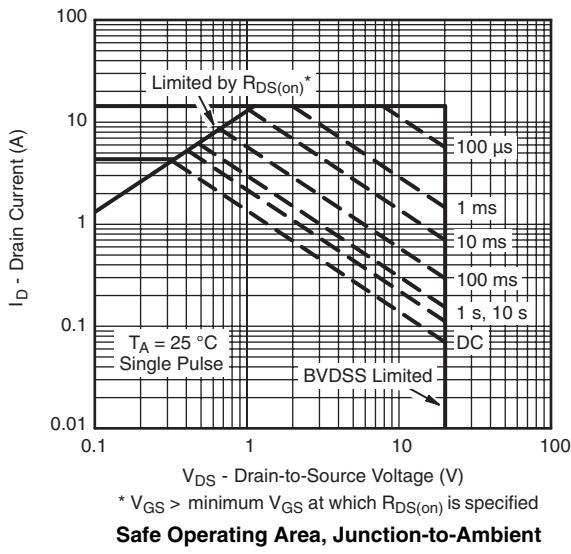
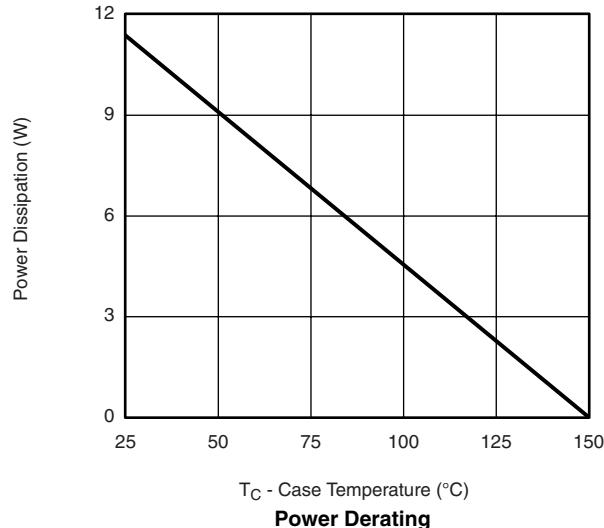
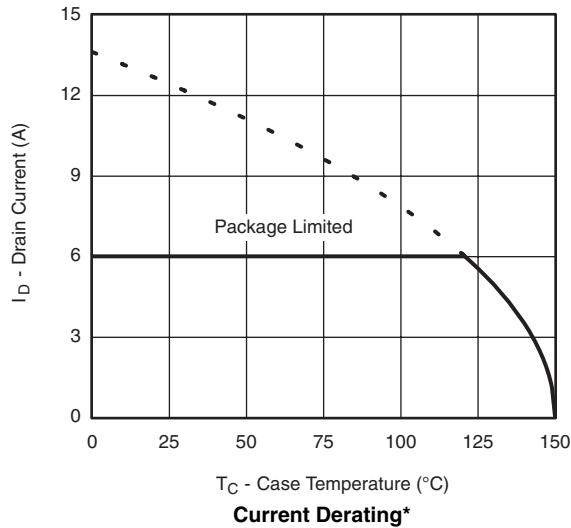
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

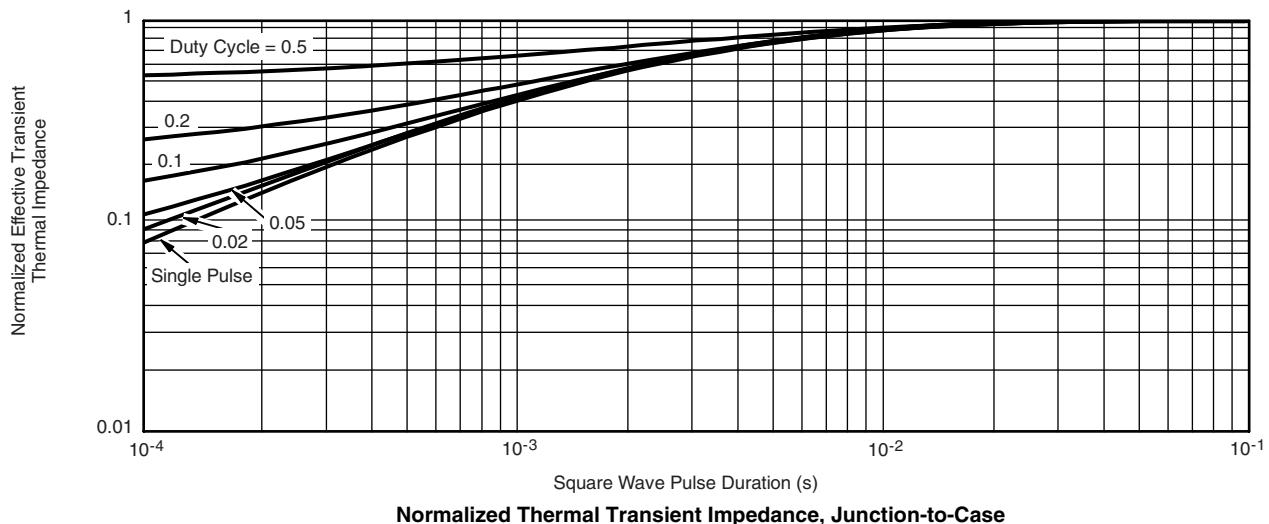
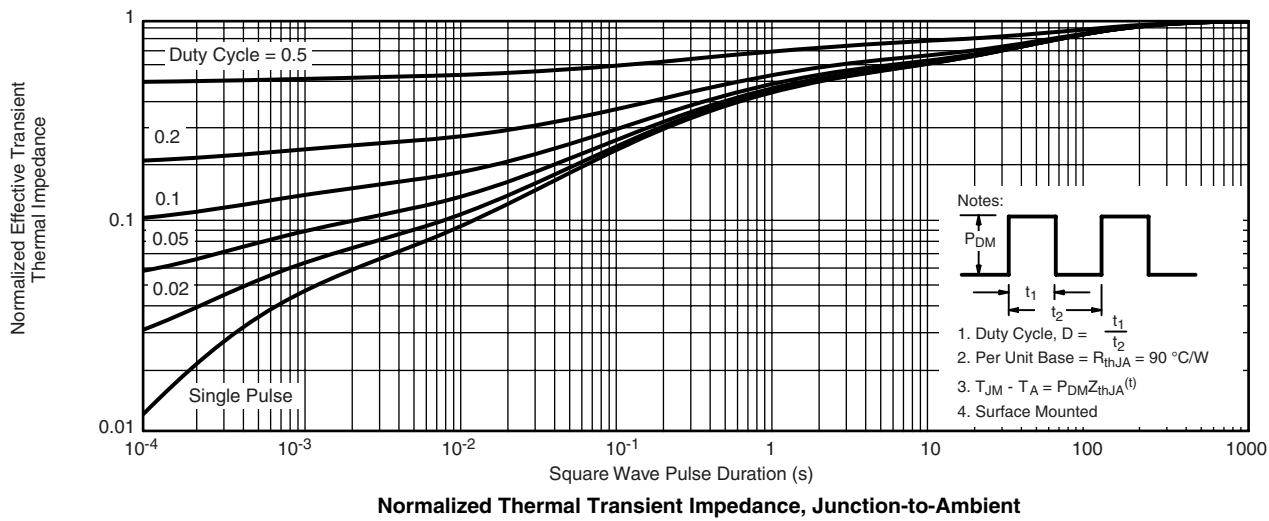
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Safe Operating Area, Junction-to-Ambient


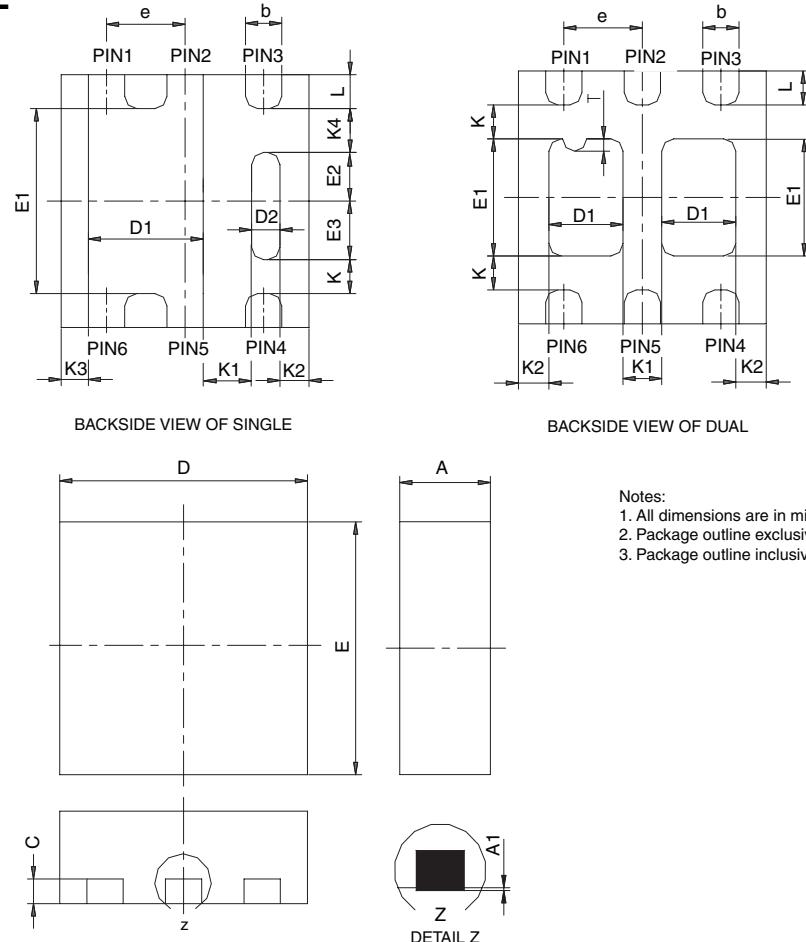
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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PowerPAK® SC70-6L



Notes:

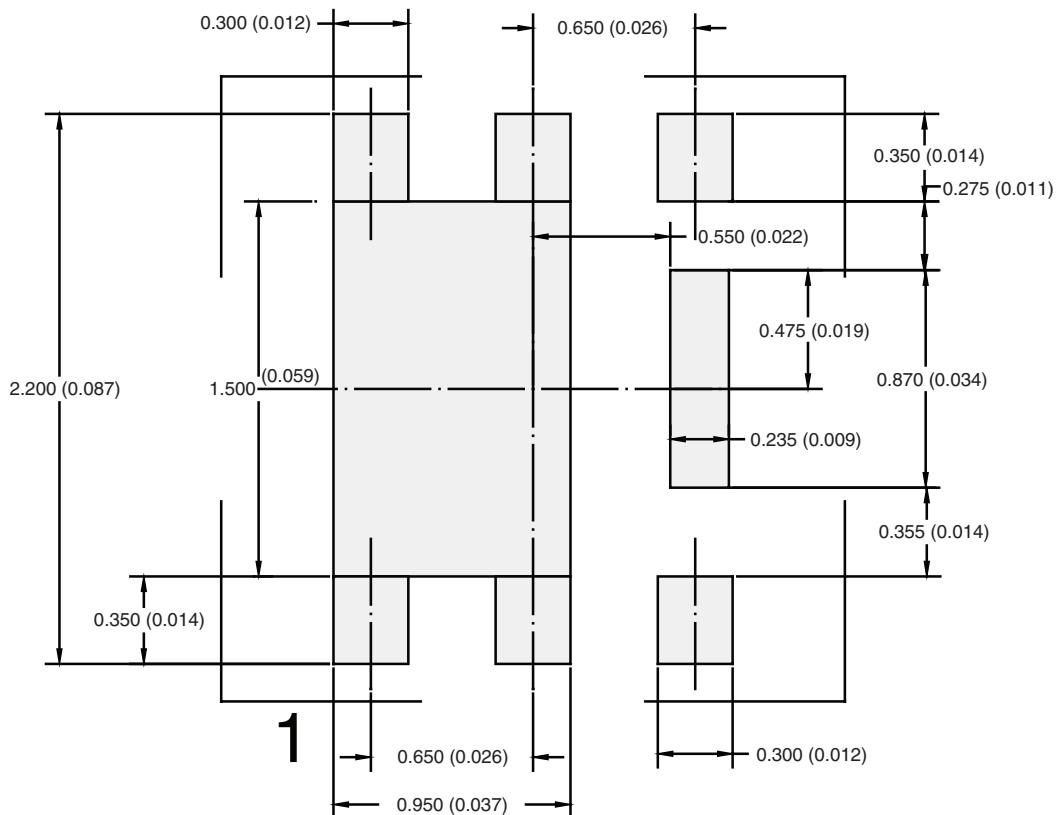
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07

DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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