

N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Channel	20	0.060 at V _{GS} = 4.5 V	4.5 ^a	3.5 nC
		0.092 at V _{GS} = 2.5 V	4.5 ^a	
P-Channel	- 20	0.110 at V _{GS} = - 4.5 V	- 4.5 ^a	3 nC
		0.185 at V _{GS} = - 2.5 V	- 4.5 ^a	

FEATURES

- Halogen-free
- TrenchFET® Power MOSFETs
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance

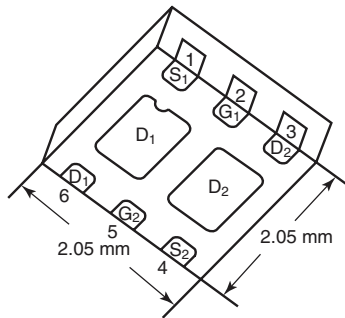


RoHS
COMPLIANT

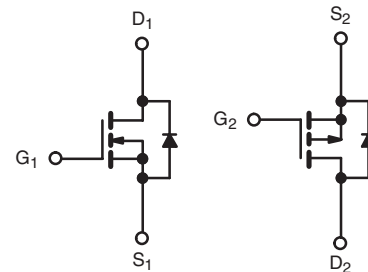
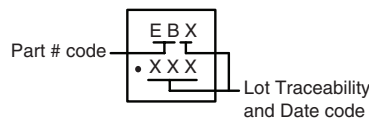
APPLICATIONS

- Portable Devices

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA513DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	- 20	V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	4.5 ^a	- 4.5 ^a	A
	T _C = 70 °C		4.5 ^a	- 4.5 ^a	
	T _A = 25 °C		4.5 ^{a, b, c}	- 3.3 ^{b, c}	
	T _A = 70 °C		3.2 ^{b, c}	- 2.4 ^{b, c}	
Pulsed Drain Current		I _{DM}	15	- 10	
Source Drain Current Diode Current	T _C = 25 °C	I _S	4.5 ^a	- 4.5 ^a	
	T _A = 25 °C		1.6 ^{b, c}	- 1.6 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	6.5	6.5	W
	T _C = 70 °C		5	5	
	T _A = 25 °C		1.9 ^{b, c}	1.9 ^{b, c}	
	T _A = 70 °C		1.2 ^{b, c}	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	12.5	16	12.5	16	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 110 °C/W.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted									
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit		
Static									
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	20			V		
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 20					
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		22		mV/°C		
		I _D = - 250 μA	P-Ch		- 16				
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 3.5				
		I _D = - 250 μA	P-Ch		2.5				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6		1.5	V		
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 0.6		- 1.5			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch P-Ch			± 100 ± 100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	μA		
		V _{DS} = - 20 V, V _{GS} = 0 V	P-Ch			- 1			
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10			
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10			
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	10			A		
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 5					
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 3.4 A	N-Ch		0.050	0.060	Ω		
		V _{GS} = - 4.5 V, I _D = - 2.5 A	P-Ch		0.091	0.110			
		V _{GS} = 2.5 V, I _D = 1.1 A	N-Ch		0.076	0.092			
		V _{GS} = - 2.5 V, I _D = - 0.54 A	P-Ch		0.152	0.185			
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 3.4 A	N-Ch		8		S		
		V _{DS} = - 10 V, I _D = - 2.5 A	P-Ch		3.5				
Dynamic ^a									
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch P-Ch		360 250		pF		
Output Capacitance	C _{oss}		N-Ch P-Ch		70 70				
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch P-Ch		40 45				
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 4.5 A	N-Ch		7.5	12	nC		
		V _{DS} = - 10 V, V _{GS} = - 10 V, I _D = - 3.3 A	P-Ch		6	9			
Gate-Source Charge	Q _{gs}	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.5 A	N-Ch P-Ch		3.5 3	5.3 4.5			
			P-Channel V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 3.3 A	N-Ch P-Ch		0.9 0.7			
		Gate-Drain Charge		Q _{gd}		N-Ch P-Ch			0.7 0.9
Gate Resistance	R _g	f = 1 MHz	N-Ch P-Ch		2.5 8			Ω	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



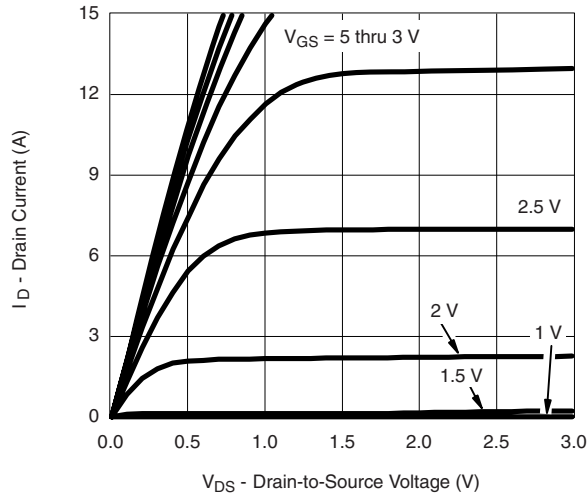
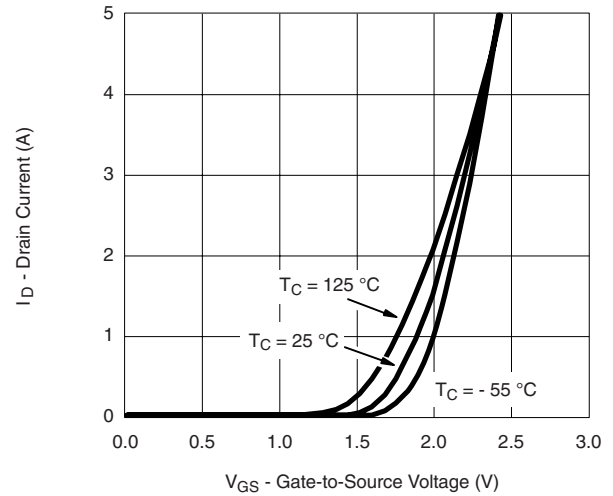
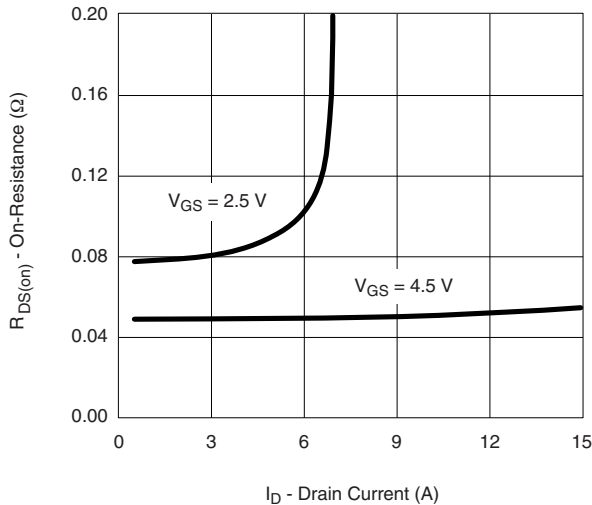
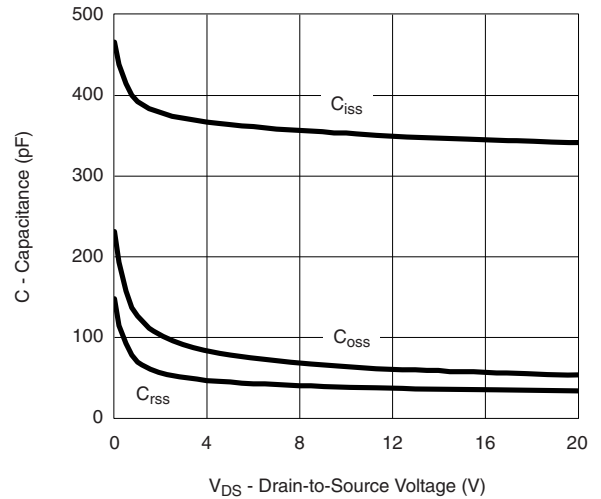
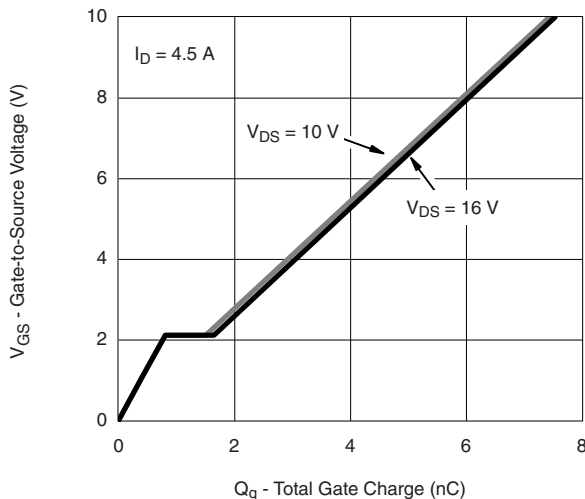
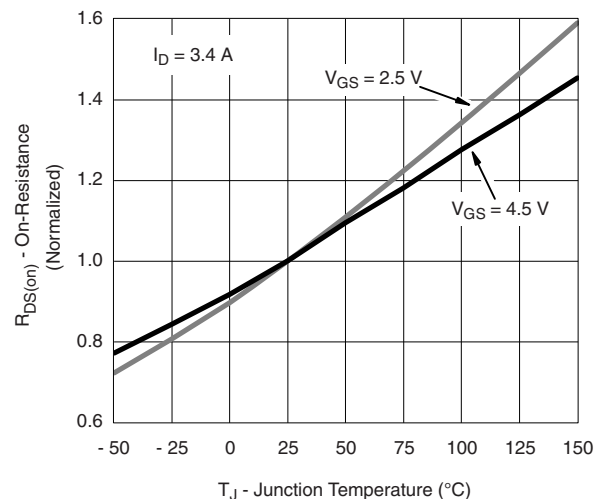
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.8\text{ }\Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$ P-Channel $V_{DD} = -10\text{ V}$, $R_L = 3.9\text{ }\Omega$ $I_D \cong -2.6\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		10	15	ns
			P-Ch		20	30	
Rise Time	t_r		N-Ch		40	60	
			P-Ch		45	70	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		20	30	
			P-Ch		15	25	
Fall Time	t_f		N-Ch		30	45	
			P-Ch		10	15	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$, $R_L = 2.8\text{ }\Omega$ $I_D \cong 3.6\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$ P-Channel $V_{DD} = -10\text{ V}$, $R_L = 3.9\text{ }\Omega$ $I_D \cong -2.6\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		5	10	
			P-Ch		4	8	
Rise Time	t_r		N-Ch		15	25	
			P-Ch		12	20	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		15	25	
			P-Ch		12	20	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		5	10	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	N-Ch			4.5	A
			P-Ch			- 4.5	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			15	
			P-Ch			- 10	
Body Diode Voltage	V_{SD}	$I_S = 3.6\text{ A}$, $V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -2.6\text{ A}$, $V_{GS} = 0\text{ V}$	P-Ch		- 0.8	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 3.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$ P-Channel $I_F = -2.6\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		15	30	ns
			P-Ch		20	40	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		10	20	nC
			P-Ch		10	20	
Reverse Recovery Fall Time	t_a		N-Ch		10		ns
			P-Ch		8		
Reverse Recovery Rise Time	t_b		N-Ch		5		
			P-Ch		12		

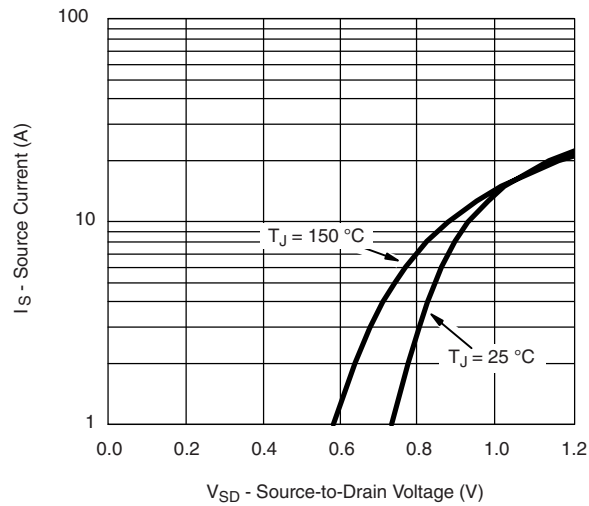
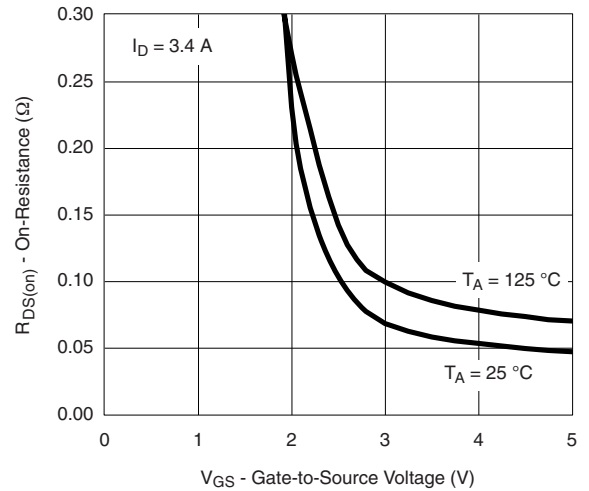
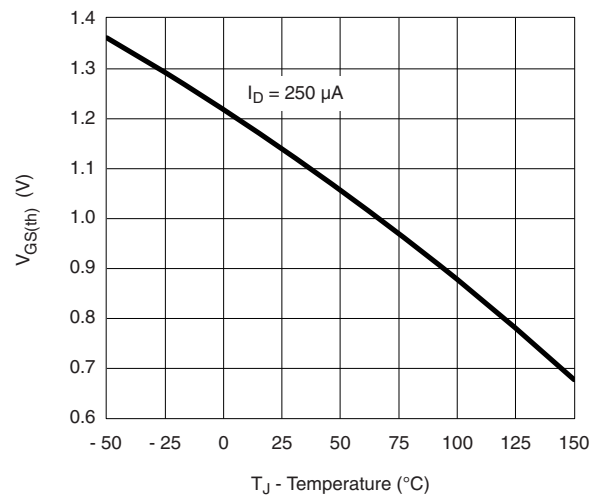
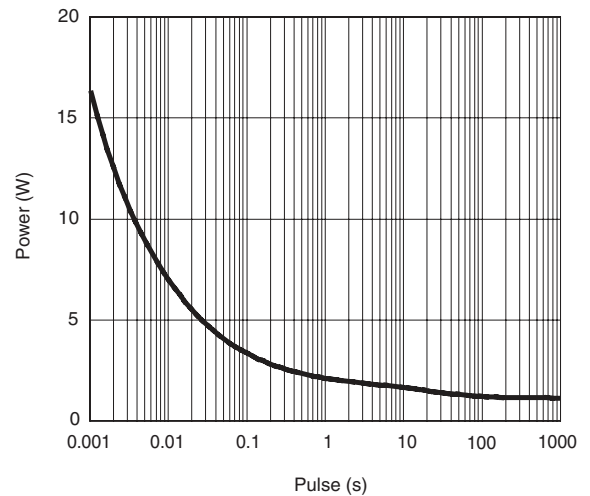
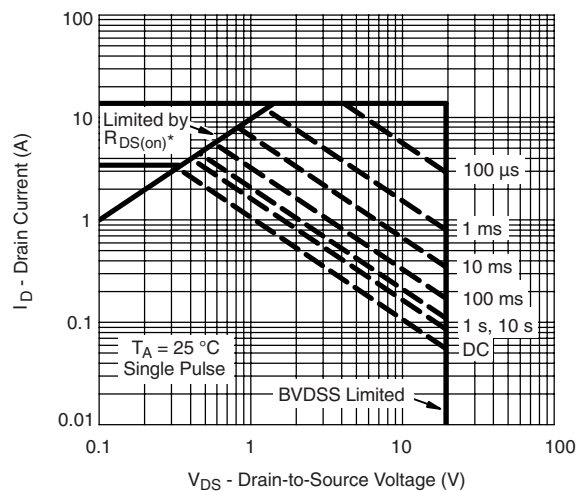
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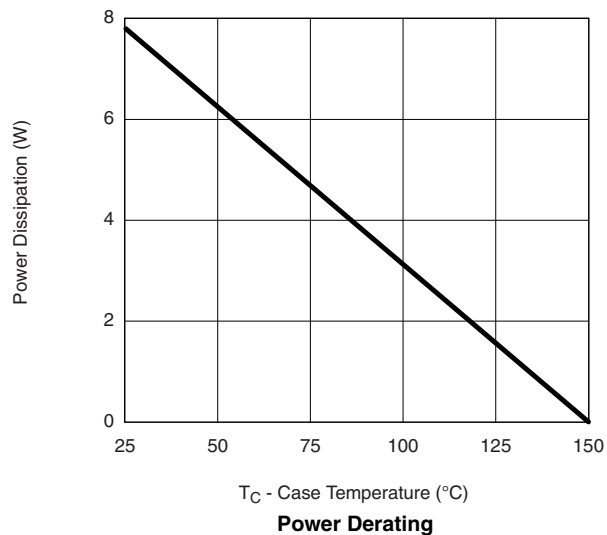
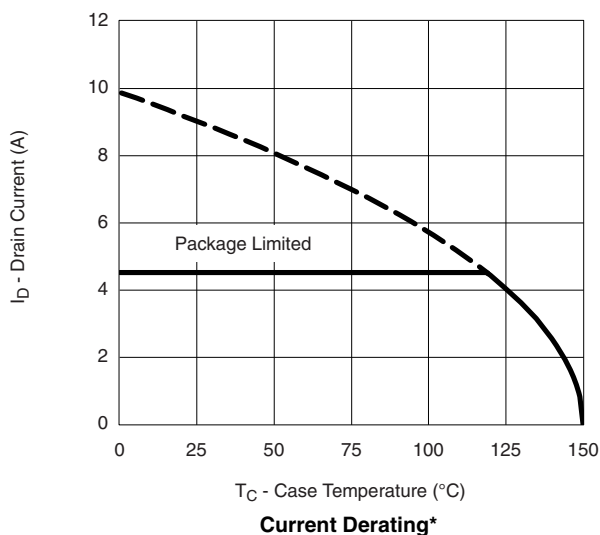
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

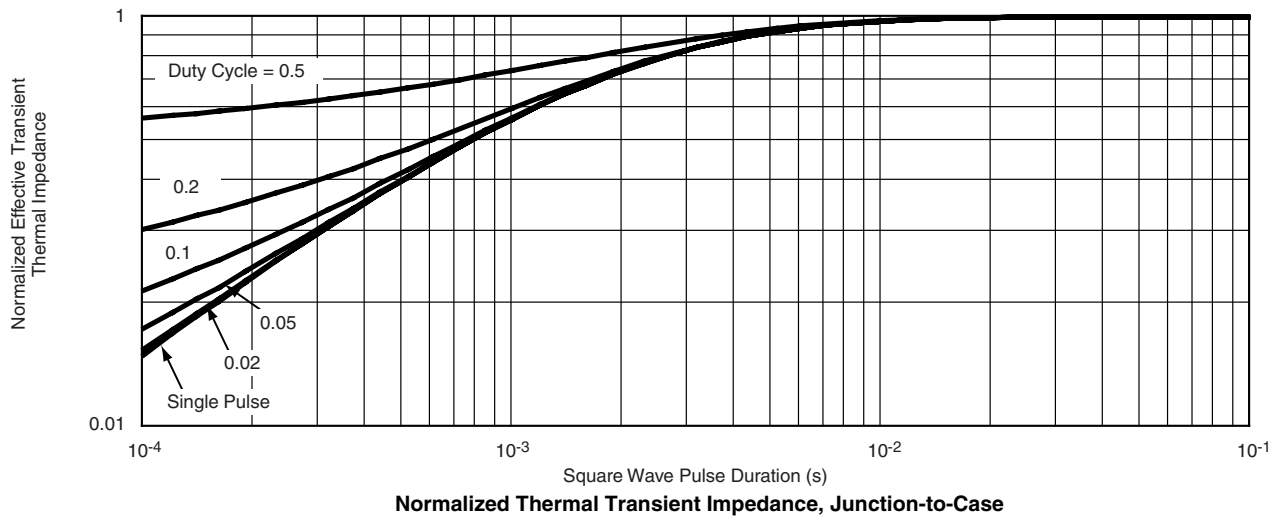
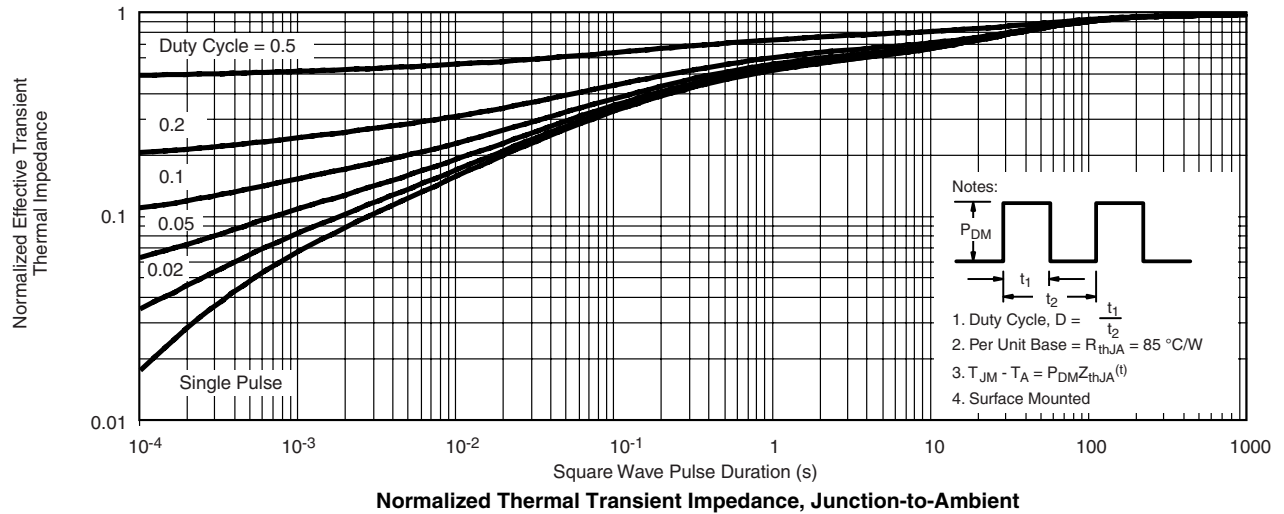
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

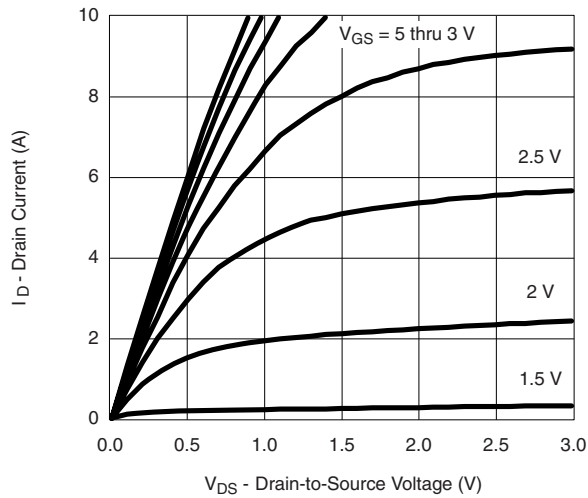
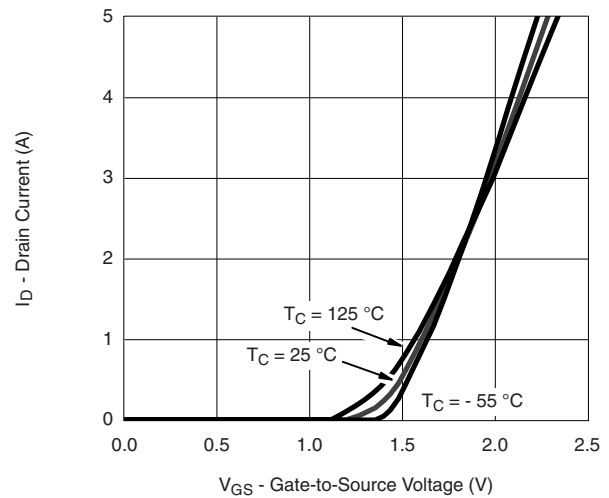
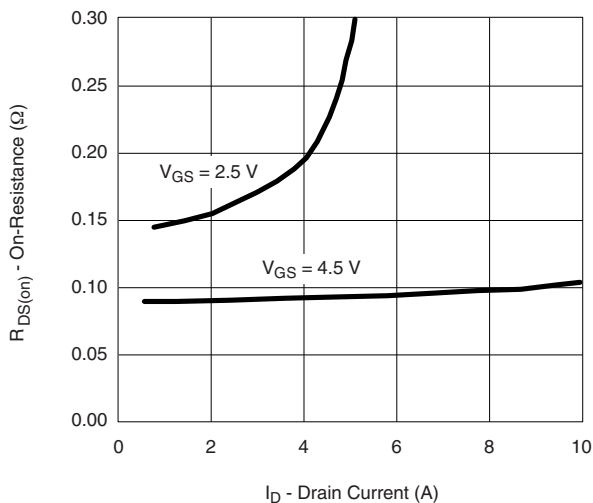
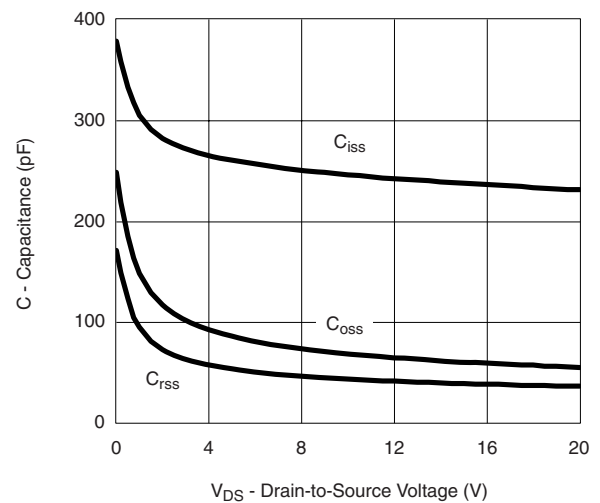
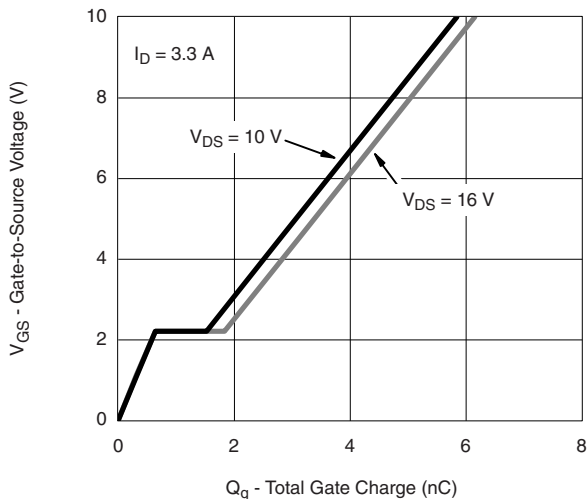
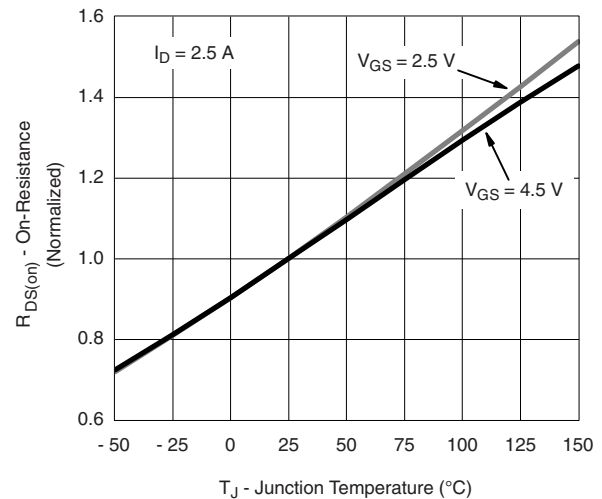
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

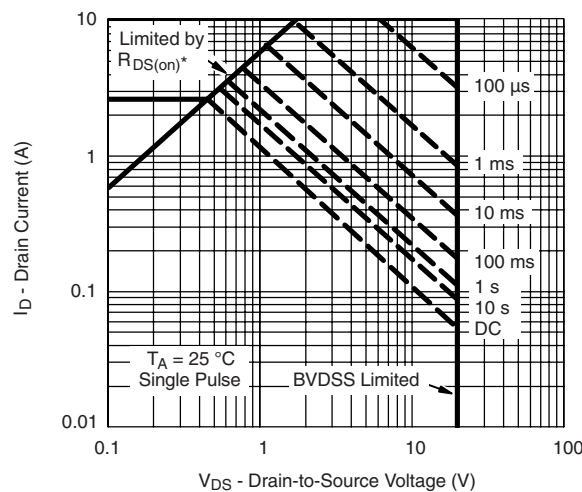
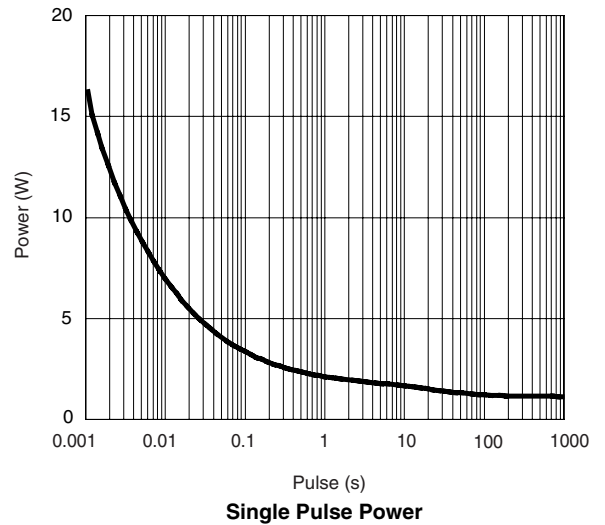
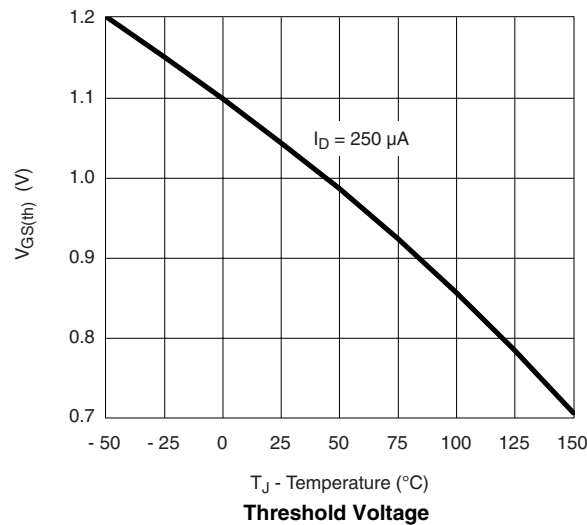
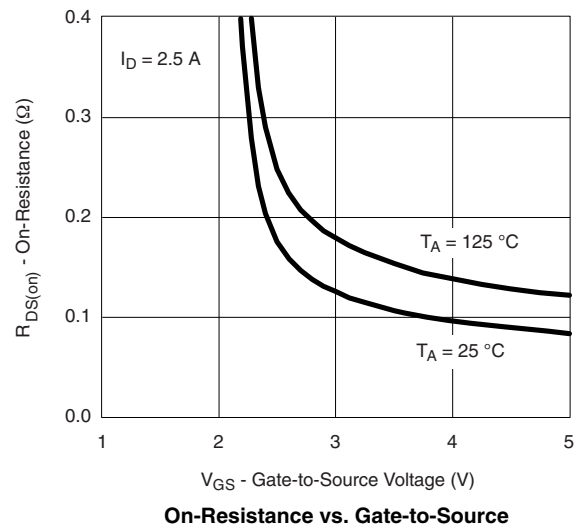
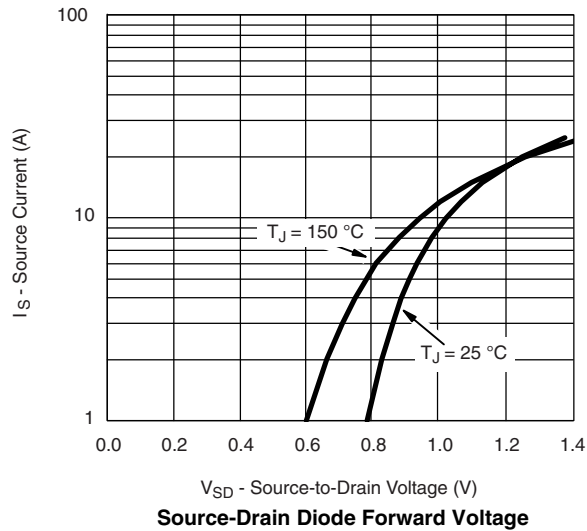
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

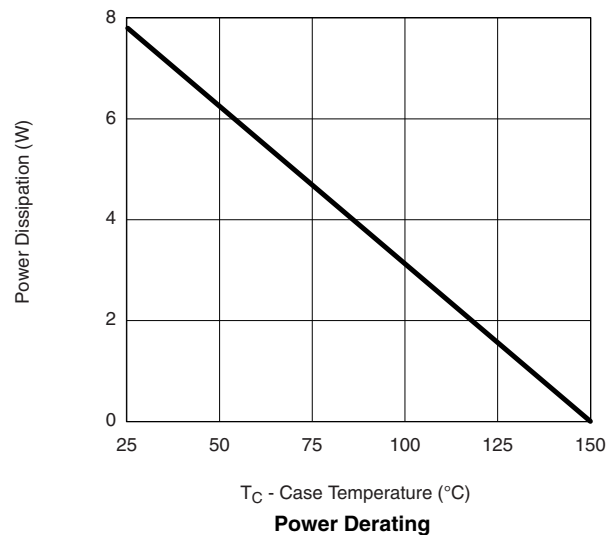
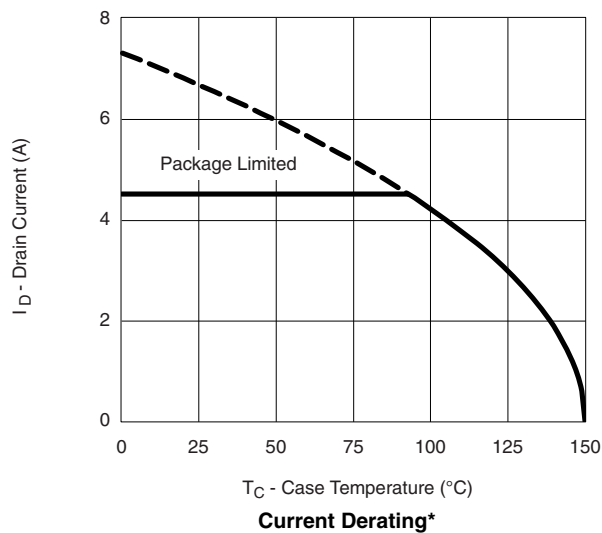


N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

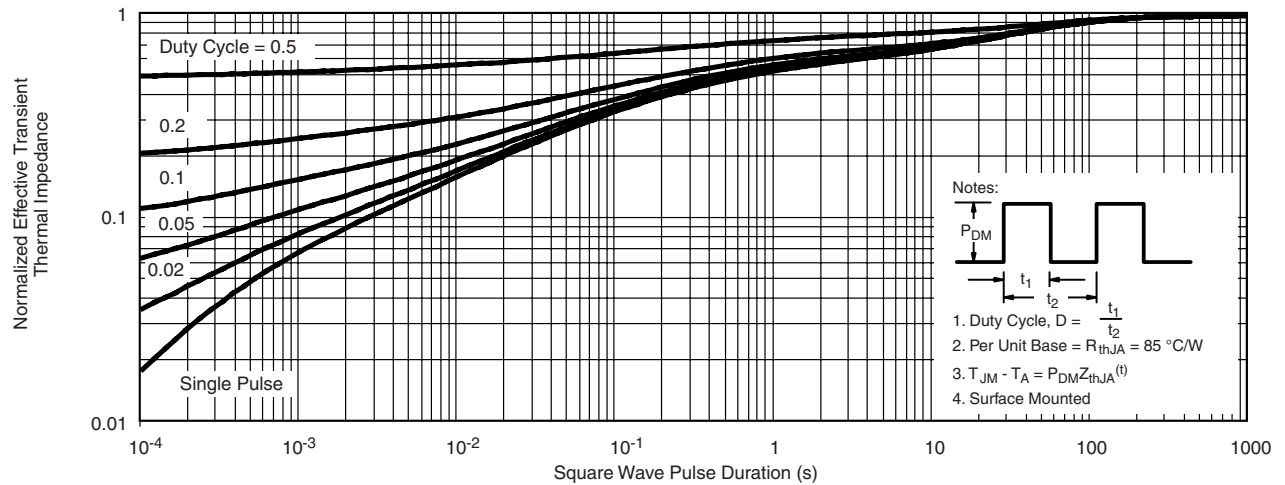
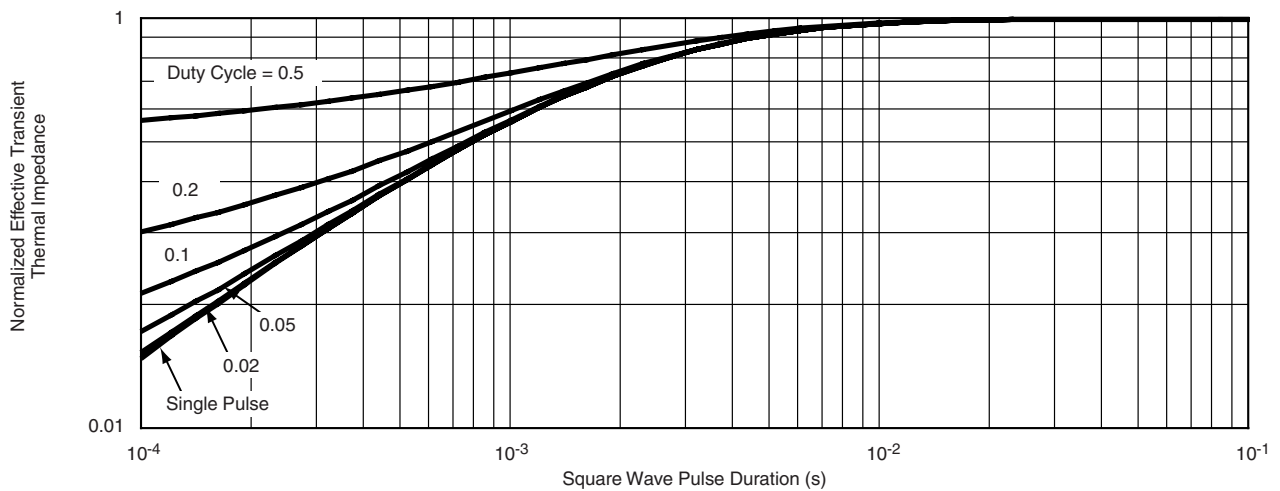


P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


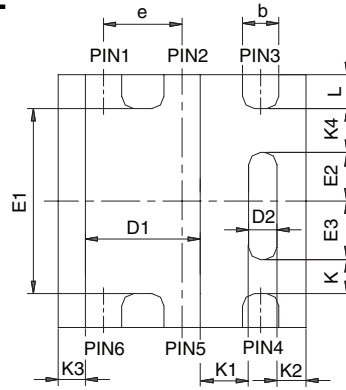
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

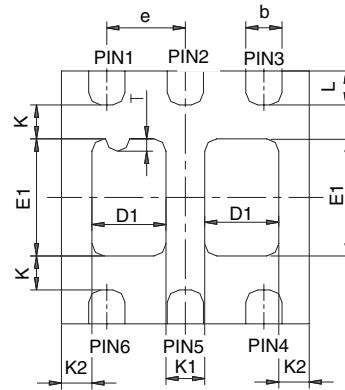
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70443>.



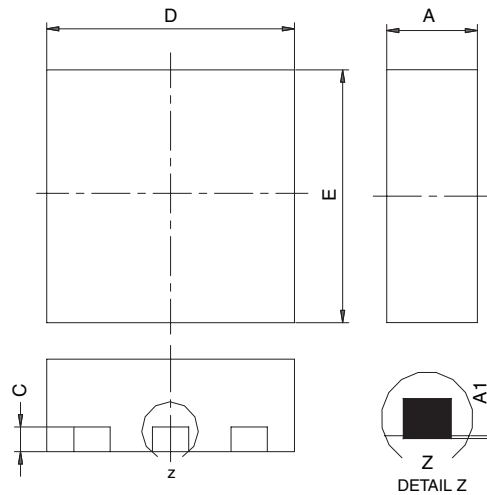
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL

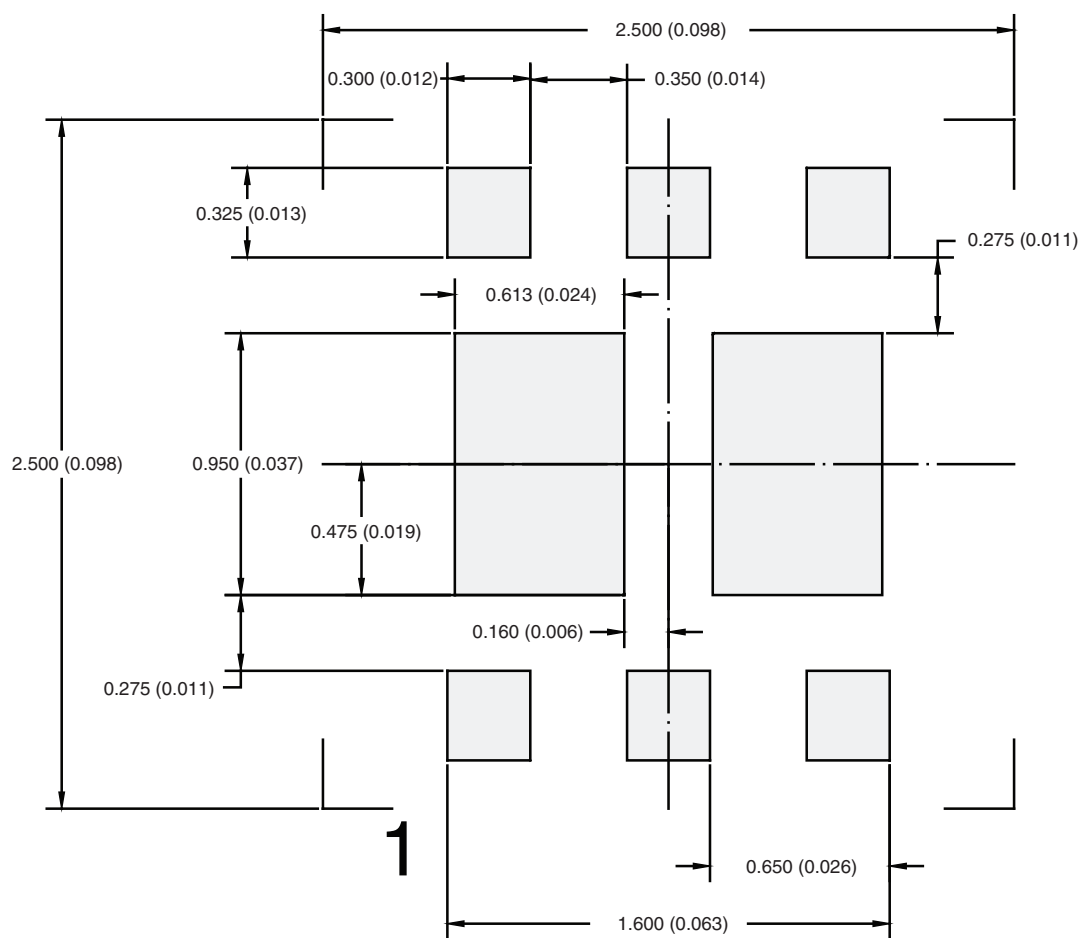


Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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