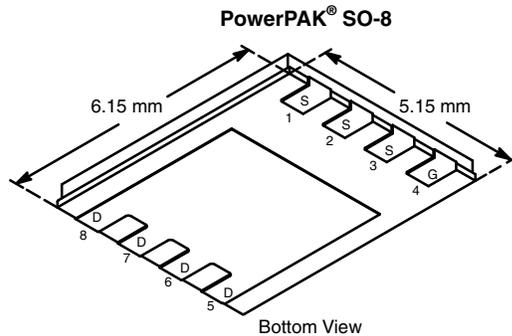


N-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
150	0.033 at V _{GS} = 10 V	35	33 nC



Ordering Information:
SiR838DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

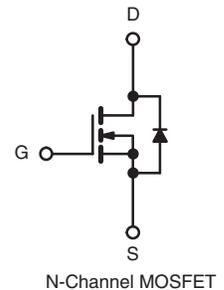
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Primary Side Switch
- Isolated DC/DC Converters



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	150	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	35	A
		T _C = 70 °C	28	
		T _A = 25 °C	8.3 ^{b, c}	
		T _A = 70 °C	6.6 ^{b, c}	
Pulsed Drain Current	I _{DM}	60		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	60 ^a	
		T _A = 25 °C	4.5 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	30		
Single Pulse Avalanche Energy	E _{AS}	45	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	96	W
		T _C = 70 °C	62	
		T _A = 25 °C	5.4 ^{b, c}	
		T _A = 70 °C	3.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	18	23	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	1	1.3		

Notes:

- Package limited
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 65 °C/W.

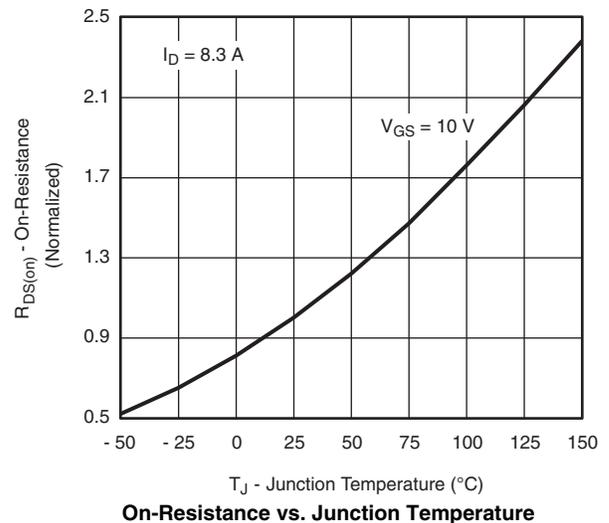
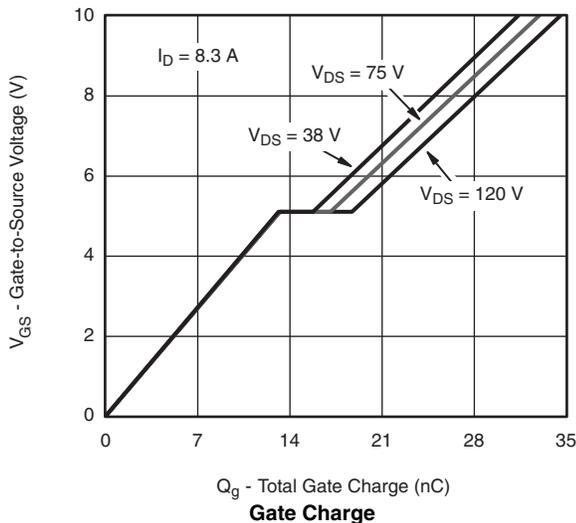
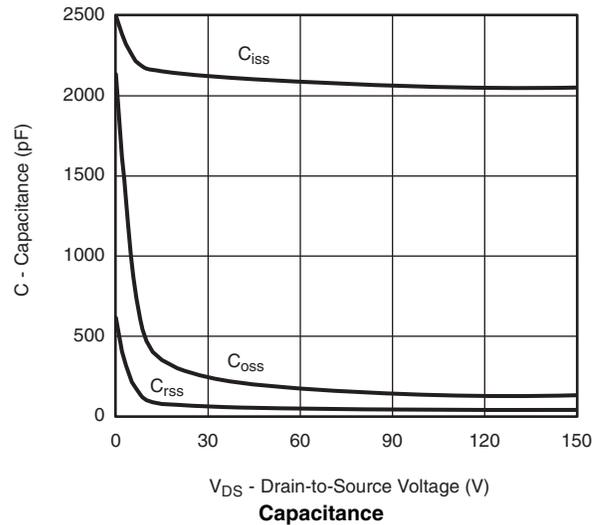
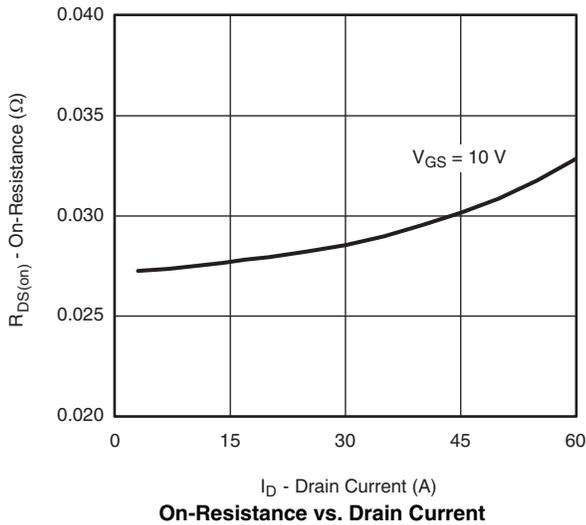
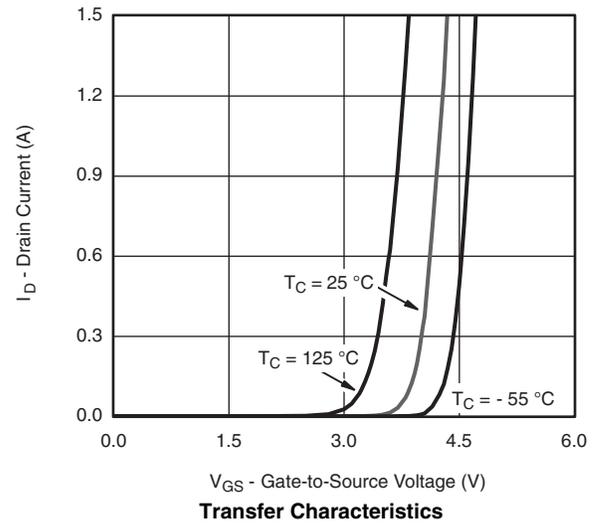
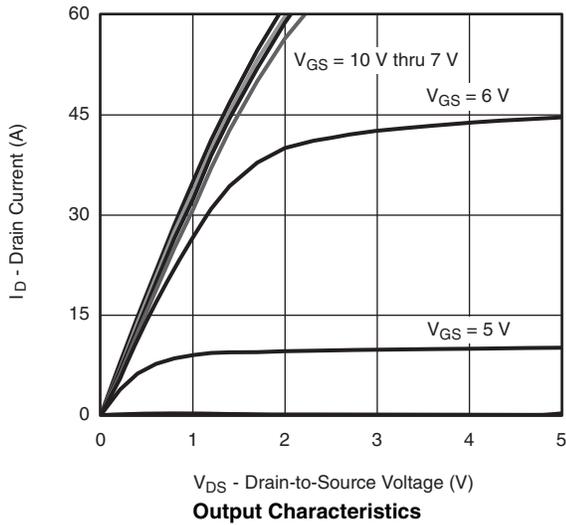
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		175		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8.3\text{ A}$		0.0275	0.0330	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 8.3\text{ A}$		28		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2075		pF
Output Capacitance	C_{oss}			155		
Reverse Transfer Capacitance	C_{rss}			45		
Total Gate Charge	Q_g	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 8.3\text{ A}$		33	50	nC
Gate-Source Charge	Q_{gs}			14		
Gate-Drain Charge	Q_{gd}			4		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.3	1.4	2.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 11.5\text{ }\Omega$ $I_D \cong 6.6\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		16	25	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			23	35	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			60	A
Pulse Diode Forward Current	I_{SM}				60	
Body Diode Voltage	V_{SD}	$I_S = 6.6\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6.6\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		77	116	ns
Body Diode Reverse Recovery Charge	Q_{rr}			260	390	nC
Reverse Recovery Fall Time	t_a			60		ns
Reverse Recovery Rise Time	t_b			17		

Notes:

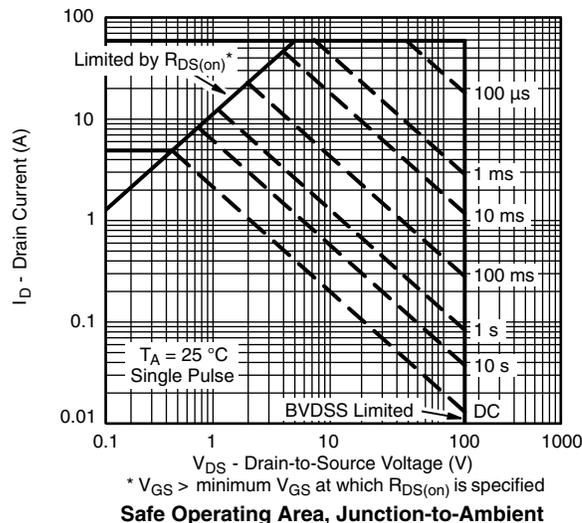
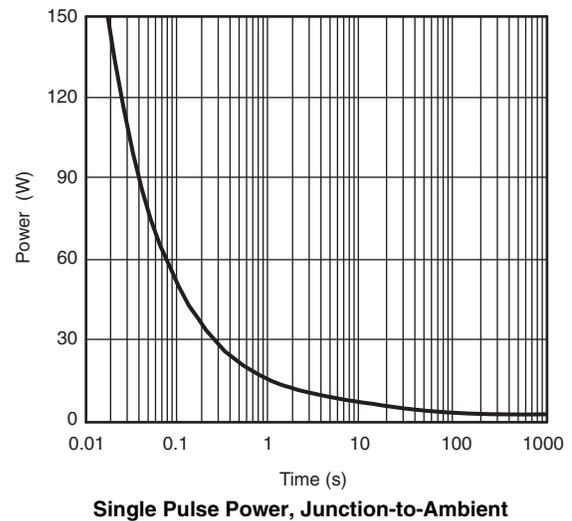
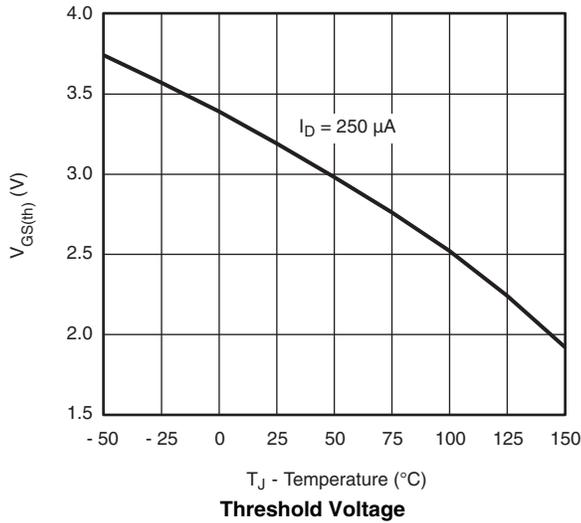
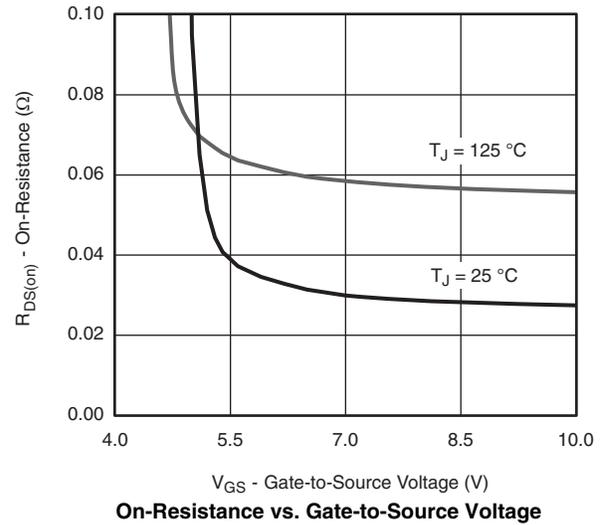
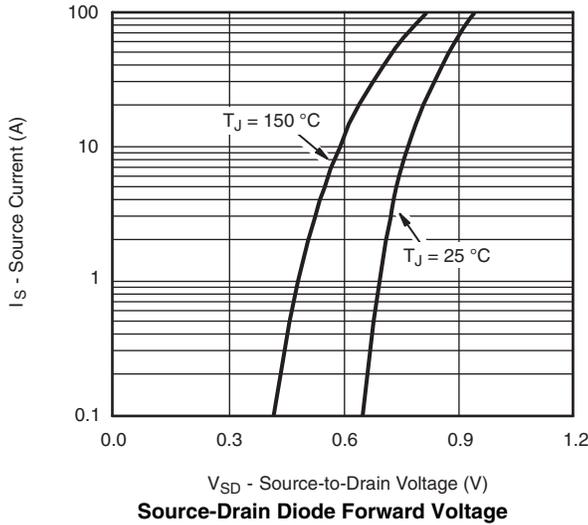
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

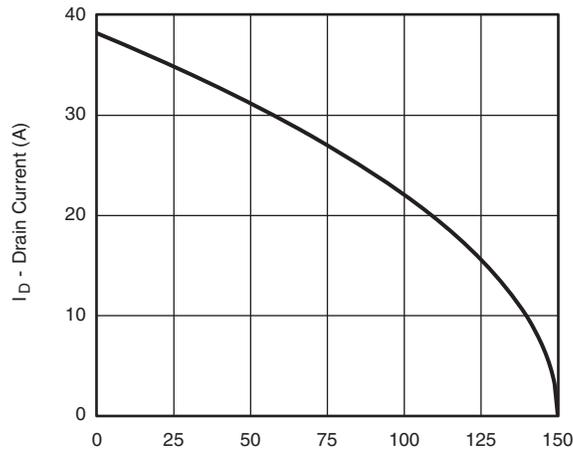
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



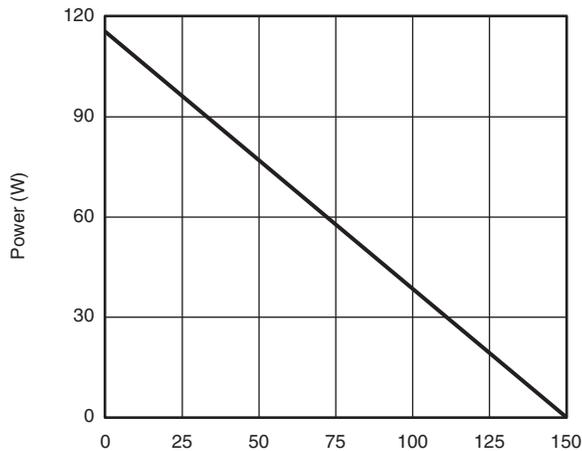
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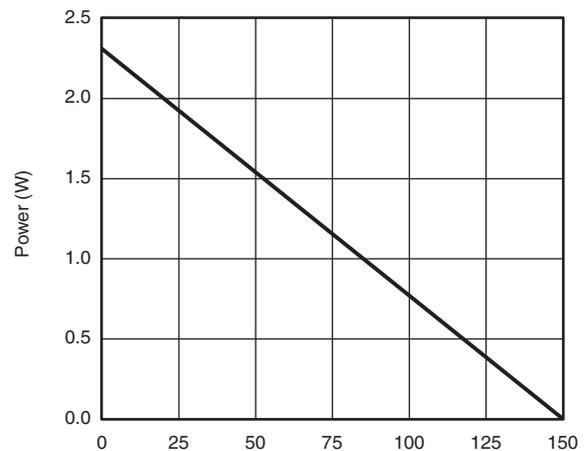
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



T_C - Case Temperature (°C)
Current Derating*



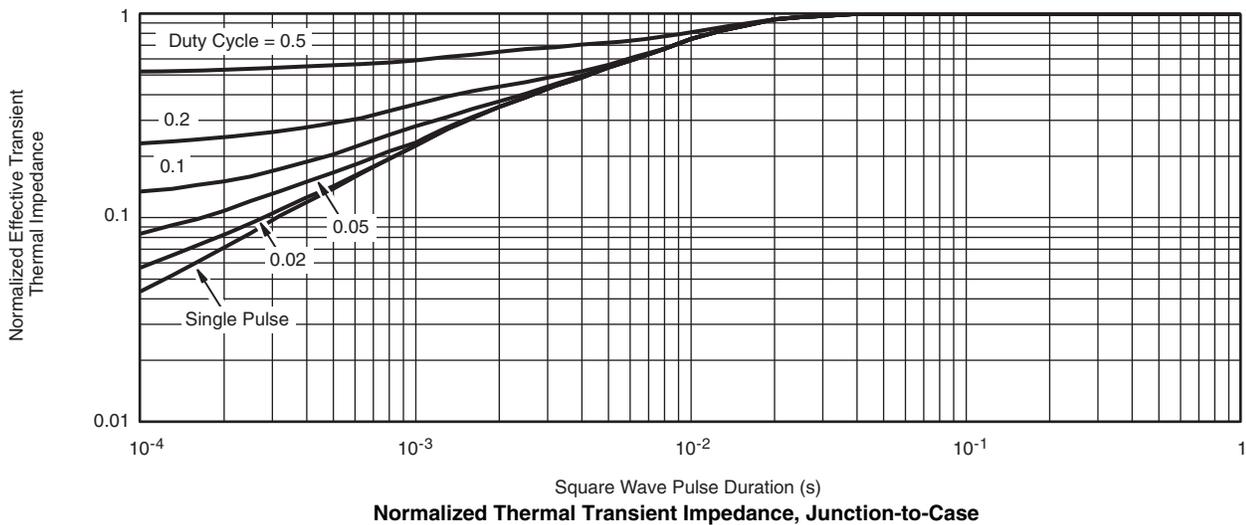
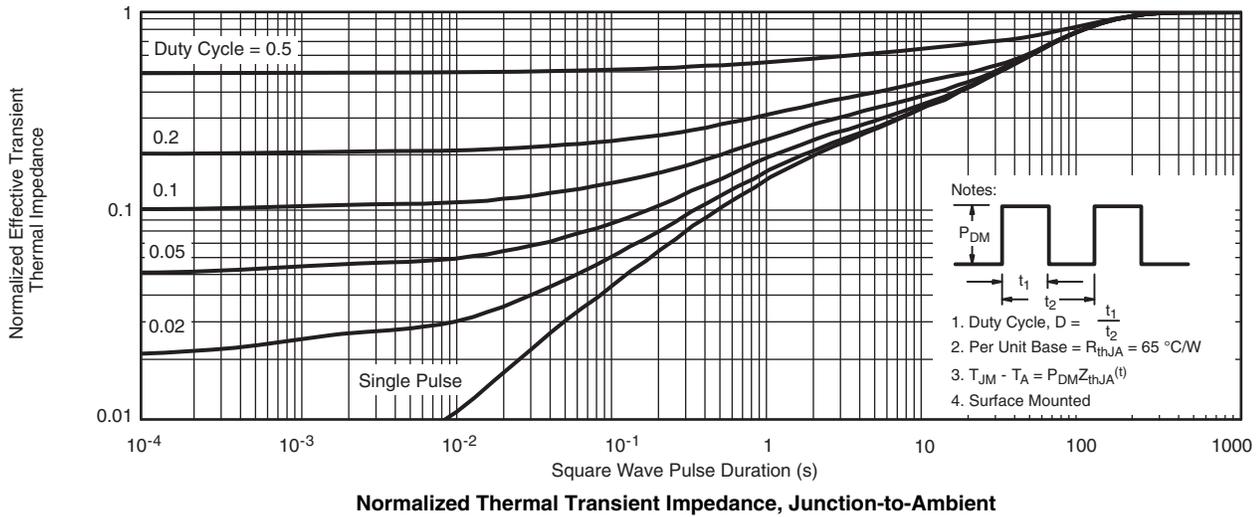
T_C - Case Temperature (°C)
Power, Junction-to-Case



T_A - Ambient Temperature (°C)
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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