

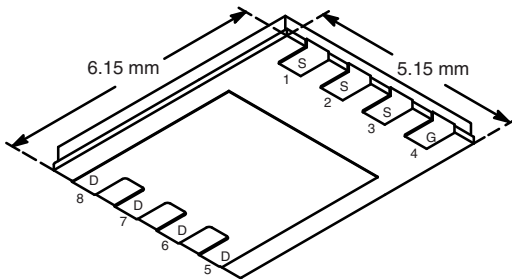


N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
100	0.0108 at $V_{GS} = 10$ V	40	16.9 nC
	0.0114 at $V_{GS} = 7.5$ V	40	
	0.0145 at $V_{GS} = 4.5$ V	40	

PowerPAK® SO-8



Bottom View

Ordering Information: SiR876DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

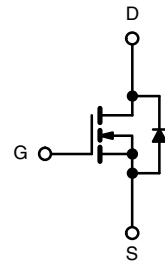
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server 48 V, Full/Half-Bridge dc-to-dc
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	40 ^a	A
		40 ^a	
		15.2 ^{b, c}	
		12.1 ^{b, c}	
Pulsed Drain Current	I_{DM}	80	mJ
Continuous Source-Drain Diode Current	I_S	40 ^a	
		4.5 ^{b, c}	
Single Pulse Avalanche Current	I_{AS}	25	
Single Pulse Avalanche Energy	E_{AS}	31.2	mJ
Maximum Power Dissipation	P_D	62.5	
		40	
		5.0 ^{b, c}	
		3.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	1.6	2.0	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 10$ s.d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 65 °C/W.

SiR876DP

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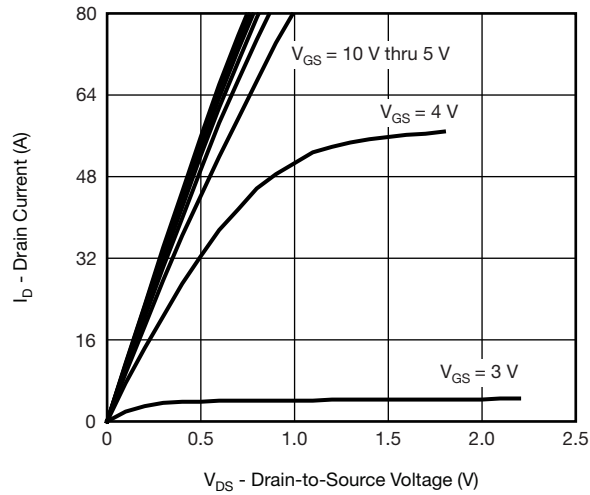
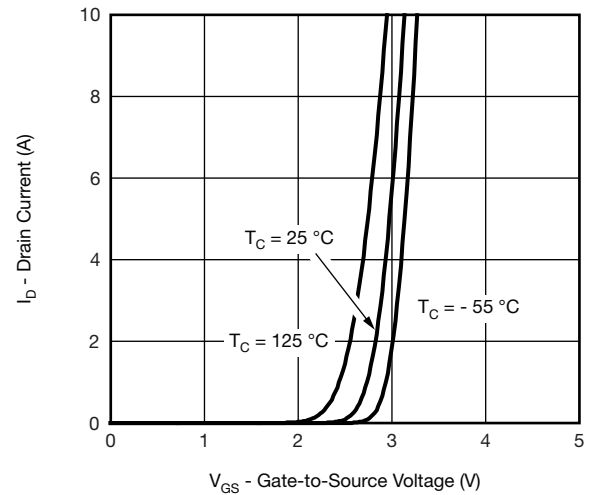
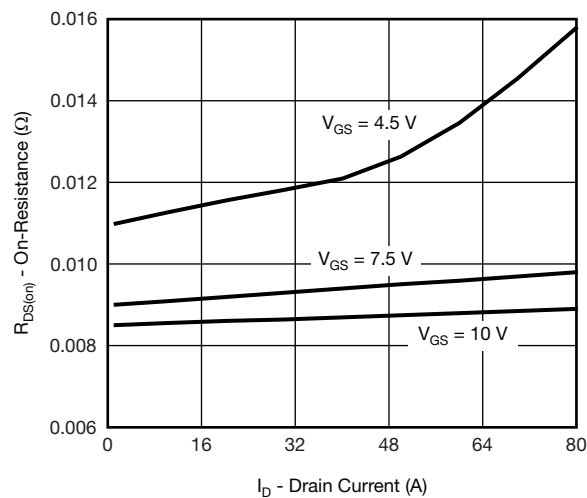
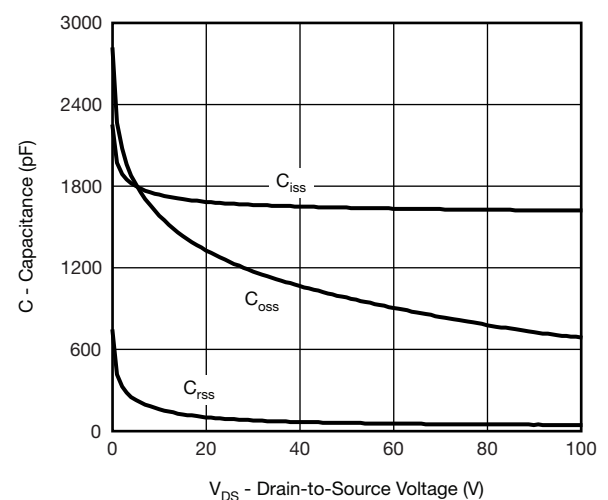
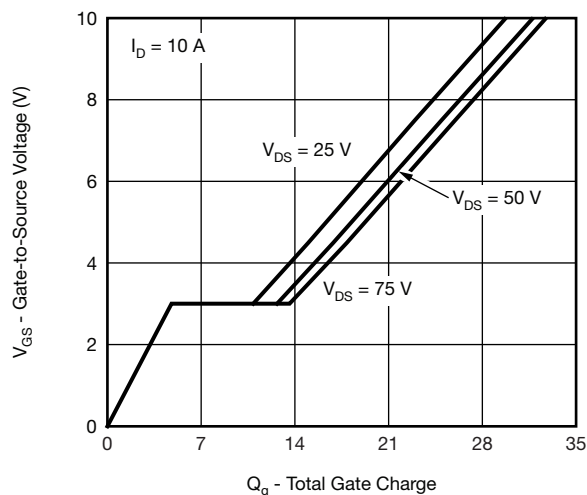
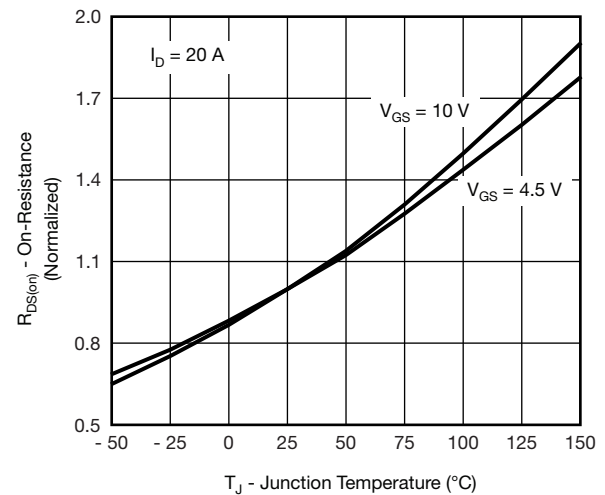
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		47		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.8	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0087	0.0108	Ω
		V _{GS} = 7.5 V, I _D = 15 A		0.0092	0.0114	
		V _{GS} = 4.5 V, I _D = 10 A		0.0115	0.0145	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A		57		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		1640		pF
Output Capacitance	C _{oss}			960		
Reverse Transfer Capacitance	C _{rss}			60		
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A		31.8	48	nC
		V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 10 A		25	37.5	
		V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 10 A		16.9	25.5	
Gate-Source Charge	Q _{gs}			4.8		
Gate-Drain Charge	Q _{gd}			7.9		
Gate Resistance	R _g	f = 1 MHz	0.8	3.6	7.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		11	22	ns
Rise Time	t _r			9	18	
Turn-Off Delay Time	t _{d(off)}			36	70	
Fall Time	t _f			11	22	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω		12	24	
Rise Time	t _r			14	28	
Turn-Off Delay Time	t _{d(off)}			35	70	
Fall Time	t _f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			40	A
Pulse Diode Forward Current ^a	I _{SM}				80	
Body Diode Voltage	V _{SD}	I _S = 4 A		0.76	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		52	100	ns
Body Diode Reverse Recovery Charge	Q _{rr}			65	120	nC
Reverse Recovery Fall Time	t _a			22		ns
Reverse Recovery Rise Time	t _b			30		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

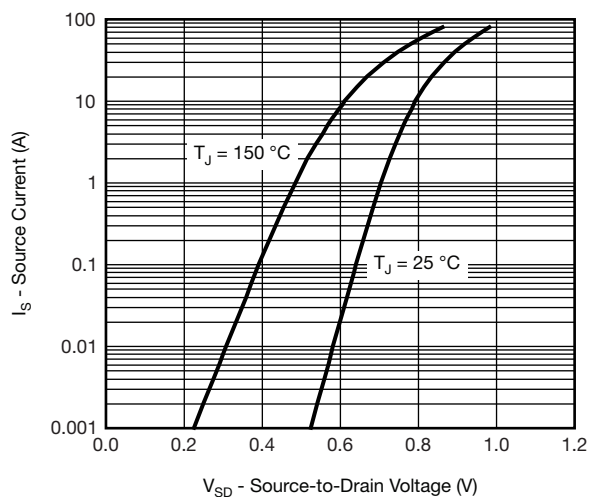
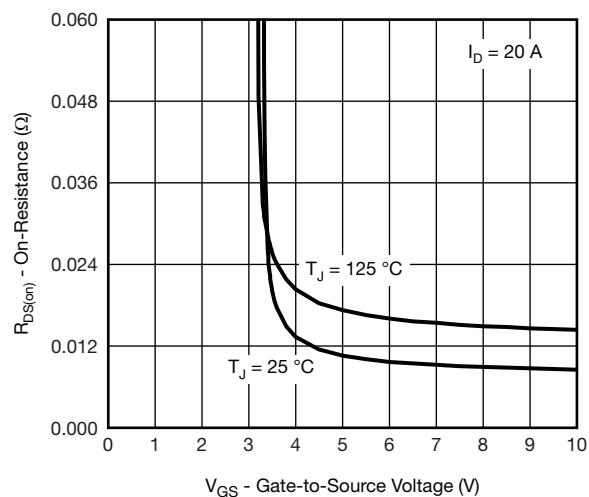
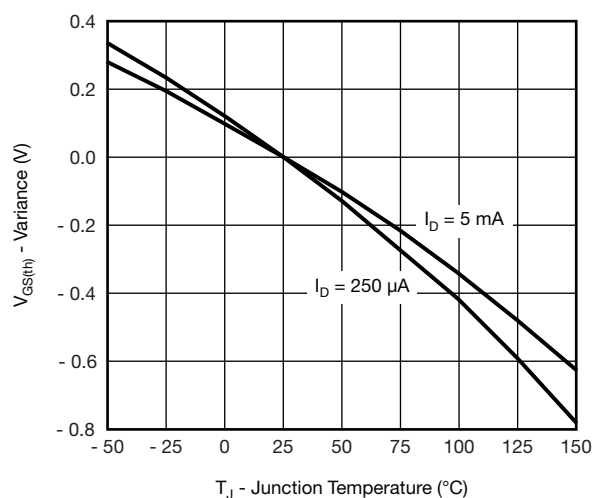
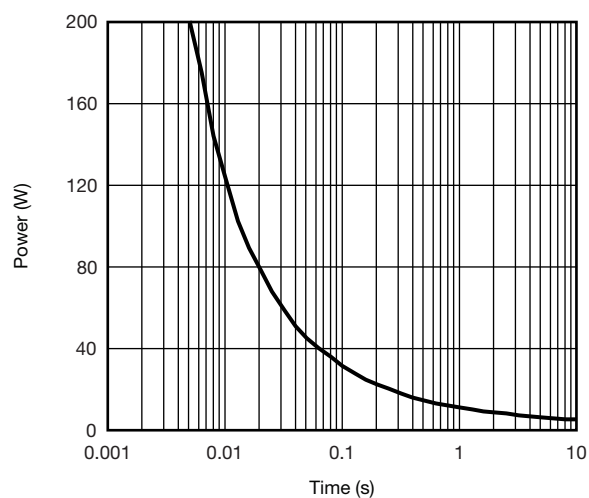
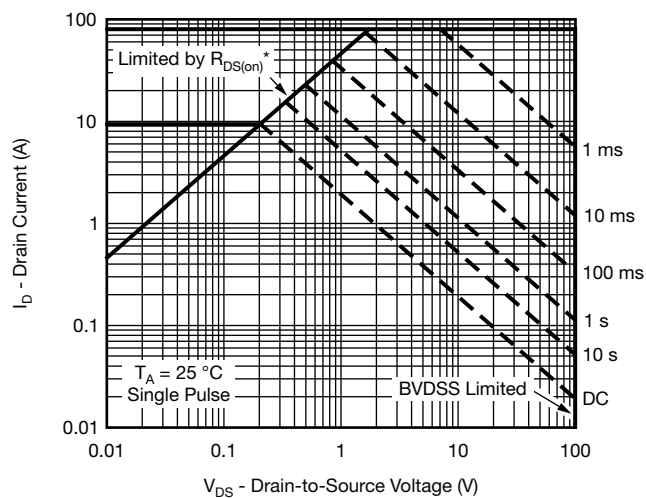
b. Guaranteed by design, not subject to production testing.

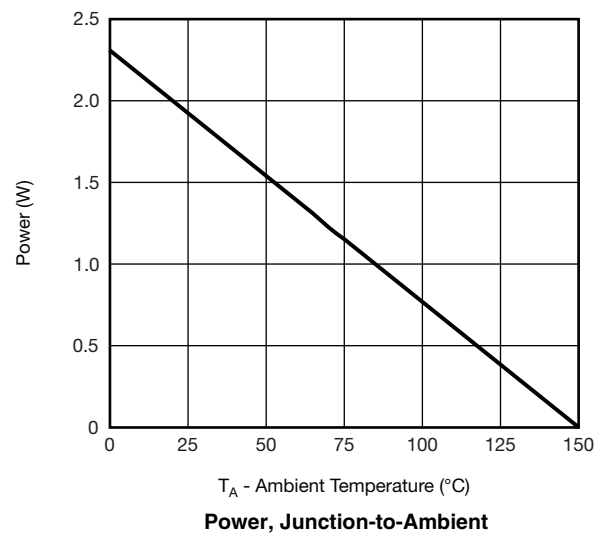
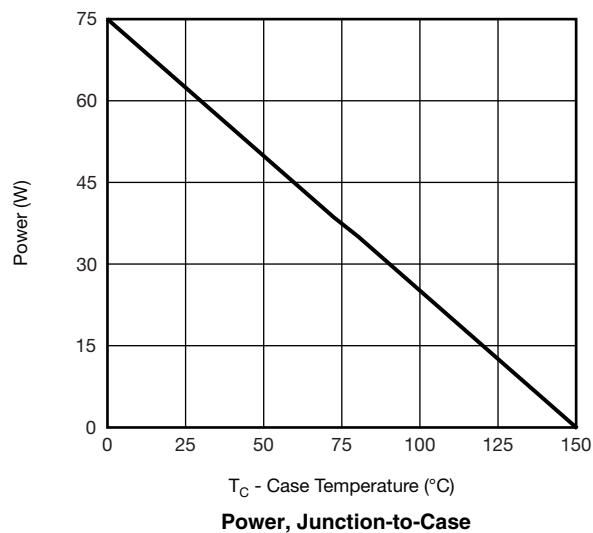
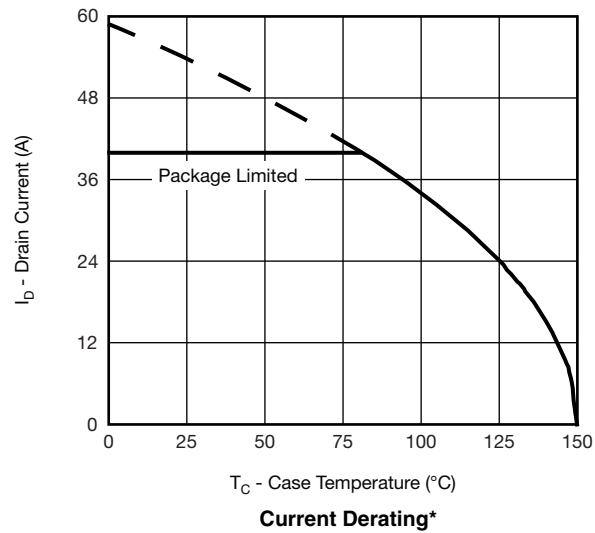
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

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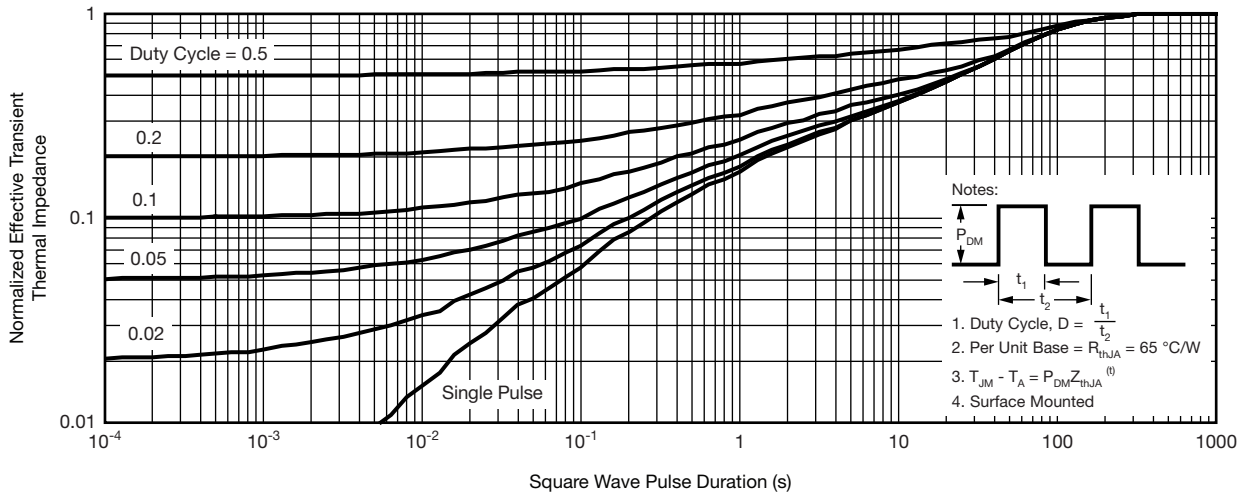
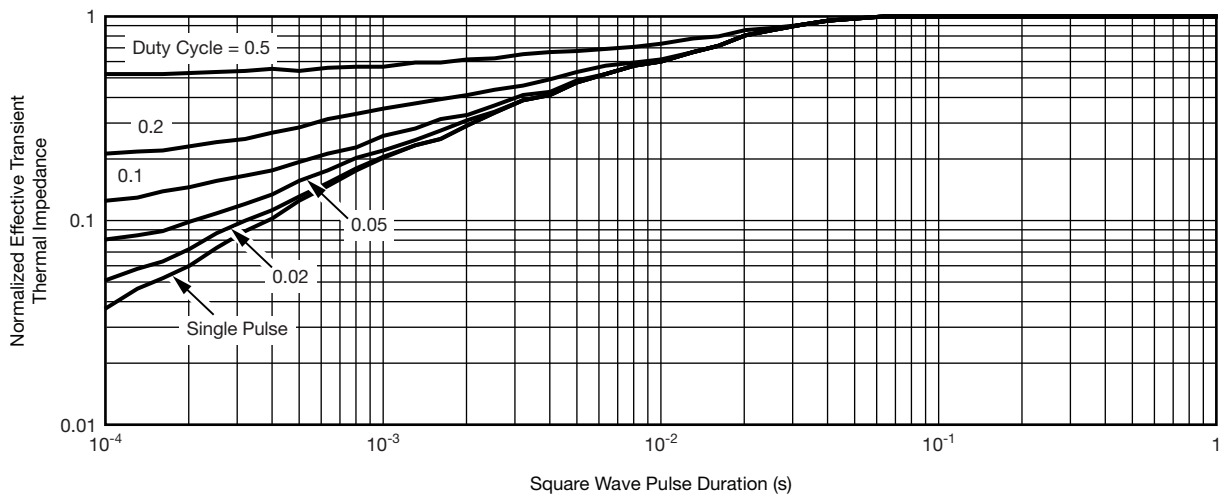
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} > \text{minimum } V_{GS} \text{ at which } R_{DS(on)} \text{ is specified}$ **Safe Operating Area, Junction-to-Ambient**


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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