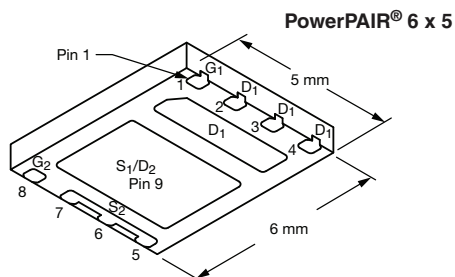




Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω) (Max.)	I _D (A)	Q _g (Typ.)
Channel-1	30	0.0071 at V _{GS} = 10 V	40 ^a	10.5 nC
		0.0089 at V _{GS} = 4.5 V	40 ^a	
Channel-2	30	0.0030 at V _{GS} = 10 V	40 ^a	29 nC
		0.0035 at V _{GS} = 4.5 V	40 ^a	



Ordering Information:

SiZ920DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

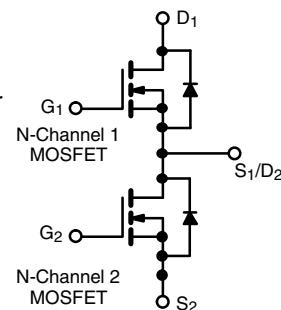
FEATURES

- TrenchFET® Power MOSFETs
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- CPU Core Power
- Computer Peripherals
- POL
- Synchronous Buck Converter



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage		V _{DS}	30		V	
Gate-Source Voltage		V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	40 ^a	40 ^a	A	
	T _C = 70 °C		40 ^a	40 ^a		
	T _A = 25 °C		22 ^{b, c}	32 ^{b, c}		
	T _A = 70 °C		17 ^{b, c}	26 ^{b, c}		
Pulsed Drain Current (t = 300 μs)		I _{DM}	70	120		
Continuous Source Drain Diode Current	T _C = 25 °C	I _S	28 ^a	28 ^a		
	T _A = 25 °C		3.6 ^{b, c}	4.3 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	25	40		
Single Pulse Avalanche Energy		E _{AS}	31	80	mJ	
Maximum Power Dissipation	T _C = 25 °C	P _D	39	100	W	
	T _C = 70 °C		25	64		
	T _A = 25 °C		4.3 ^{b, c}	5.2 ^{b, c}		
	T _A = 70 °C		2.8 ^{b, c}	3.3 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260			

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	23	29	19	24	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	2.5	3.2	1	1.25	

Notes:

 a. Package limited - T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

 d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 65 °C/W for channel-1 and 55 °C/W for channel-2.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	Ch-1	30			V	
		V _{GS} = 0 V, I _D = 250 μA	Ch-2	30				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	Ch-1		34		mV/°C	
		I _D = 250 μA	Ch-2		31			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	Ch-1		- 5.2			
		I _D = 250 μA	Ch-2		- 6.1			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.2		2.5	V	
		V _{DS} = V _{GS} , I _D = 250 μA	Ch-2	1		2.2		
Gate Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	Ch-1 Ch-2			± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	Ch-1			1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V	Ch-2			1		
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	Ch-1			5		
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	Ch-2			5		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1	20			A	
		V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-2	25				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 18.9 A	Ch-1		0.0059	0.0071	Ω	
		V _{GS} = 10 V, I _D = 20 A	Ch-2		0.0025	0.0030		
		V _{GS} = 4.5 V, I _D = 16.9 A	Ch-1		0.0074	0.0089		
		V _{GS} = 4.5 V, I _D = 20 A	Ch-2		0.0029	0.0035		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 18.9 A	Ch-1		66		S	
		V _{DS} = 10 V, I _D = 20 A	Ch-2		140			
Dynamic ^a								
Input Capacitance	C _{iss}	Channel-1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		1260		pF	
			Ch-2		3600			
Output Capacitance	C _{oss}	Channel-2 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		260			
			Ch-2		660			
Reverse Transfer Capacitance	C _{rss}	Channel-1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		115			
			Ch-2		305			
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 18.9 A	Ch-1		22.3	35	nC	
		V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	Ch-2		60	110		
Gate-Source Charge	Q _{gs}	Channel-1 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 18.9 A	Ch-1		10.5	16		
			Ch-2		29	51		
			Ch-1		5.1			
			Ch-2		10			
Gate-Drain Charge	Q _{gd}	Channel-2 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	Ch-1		2.8			
			Ch-2		9.5			
Gate Resistance	R _g	f = 1 MHz	Ch-1	0.3	1.6	3.2	Ω	
			Ch-2	0.1	0.6	1.2		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1		15	23	ns
			Ch-2		30	60	
Rise Time	t _r		Ch-1		18	30	
			Ch-2		35	70	
Turn-Off Delay Time	t _{d(off)}	Ch-1		15	23		
		Ch-2		35	70		
Fall Time	t _f	Ch-1		10	20		
		Ch-2		12	25		
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1		4	8	
			Ch-2		12	25	
Rise Time	t _r		Ch-1		11	25	
			Ch-2		12	25	
Turn-Off Delay Time	t _{d(off)}	Ch-1		18	30		
		Ch-2		35	70		
Fall Time	t _f	Ch-1		8	16		
		Ch-2		10	20		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1			40	A
			Ch-2			40	
Pulse Diode Forward Current ^a	I _{SM}		Ch-1			70	
			Ch-2			120	
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	Ch-1		0.8	1.2	V
		I _S = 10 A, V _{GS} = 0 V	Ch-2		0.8	1.2	
Body Diode Reverse Recovery Time	t _{rr}	Channel-1 I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		17	30	ns
			Ch-2		36	70	
Body Diode Reverse Recovery Charge	Q _{rr}		Ch-1		10	20	nC
			Ch-2		36	70	
Reverse Recovery Fall Time	t _a	Channel-2 I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		10		ns
			Ch-2		20		
Reverse Recovery Rise Time	t _b		Ch-1		7		
			Ch-2		16		

Notes:

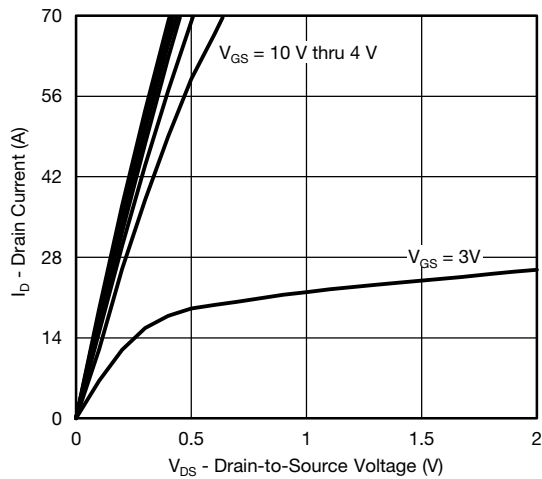
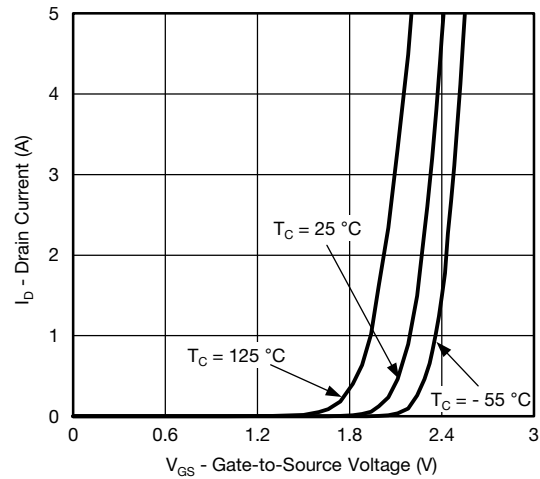
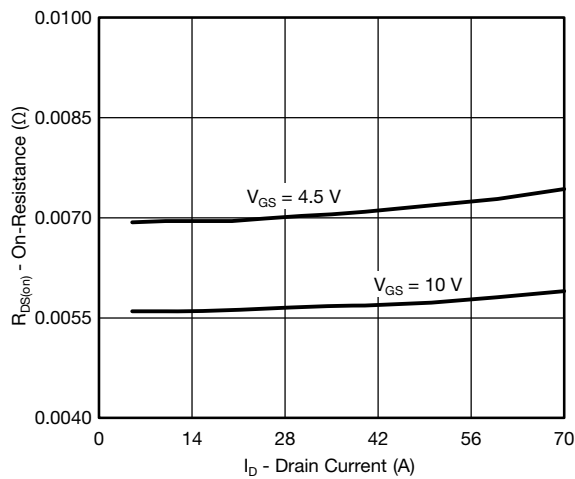
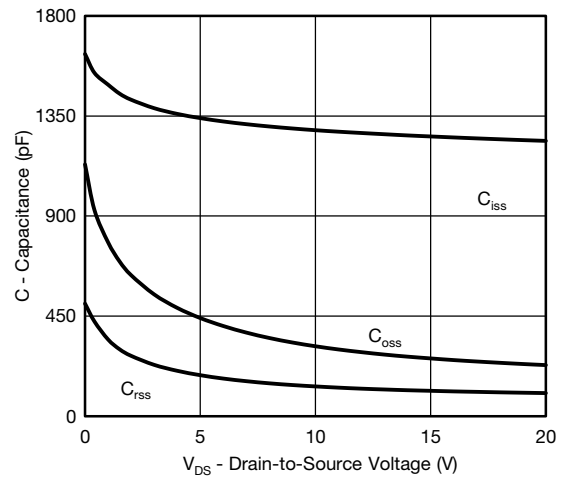
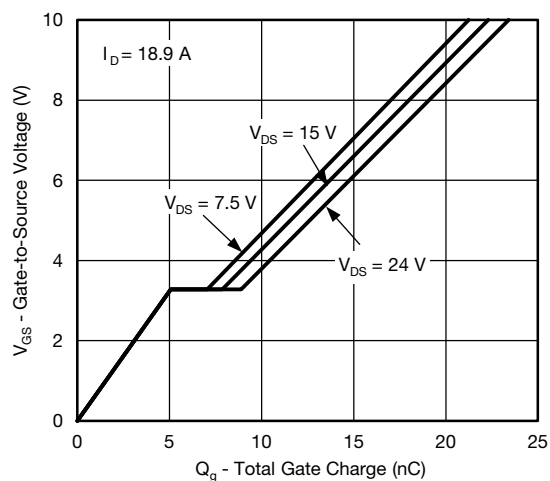
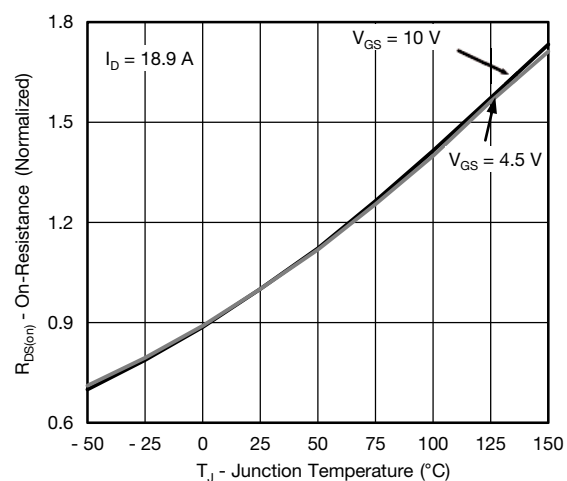
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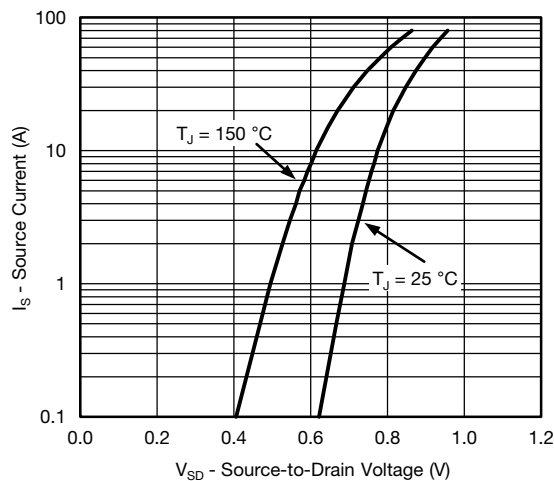
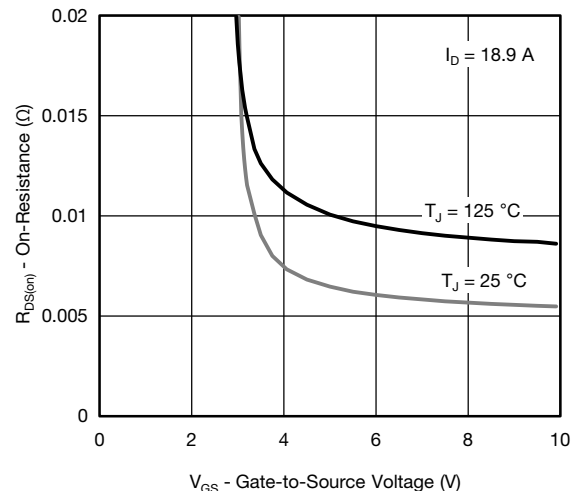
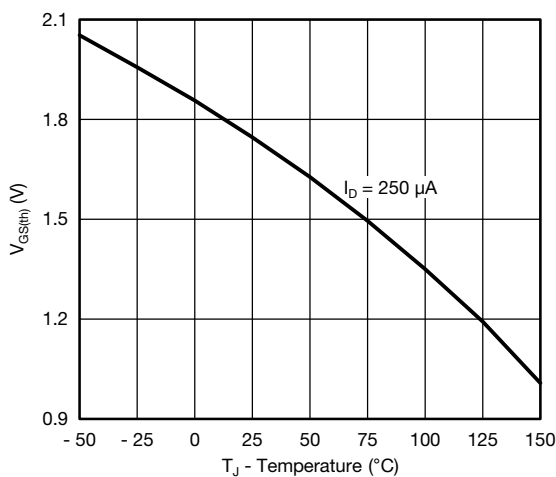
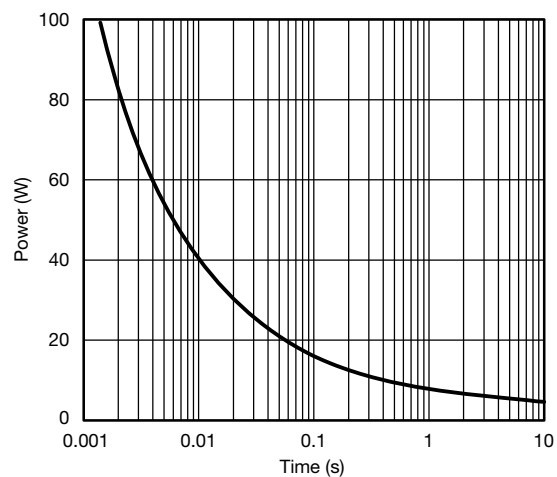
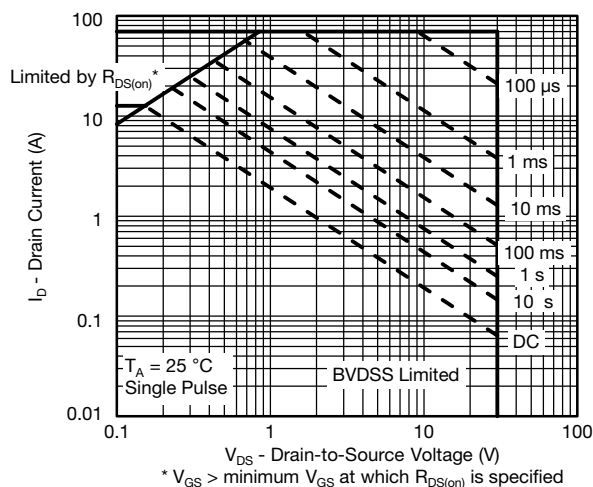
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SiZ920DT

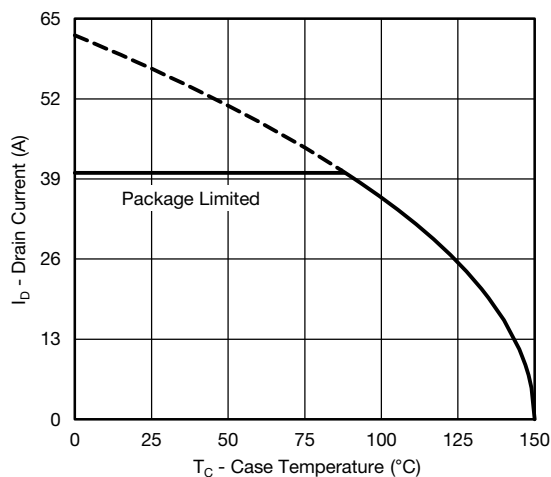
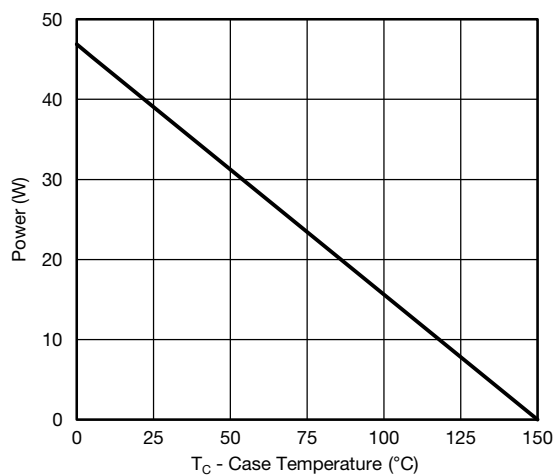
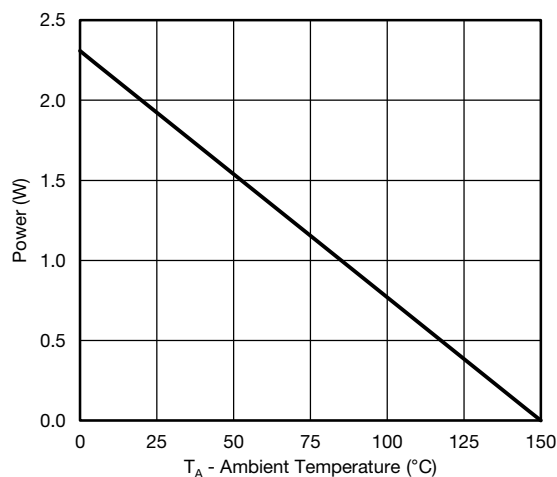
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**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

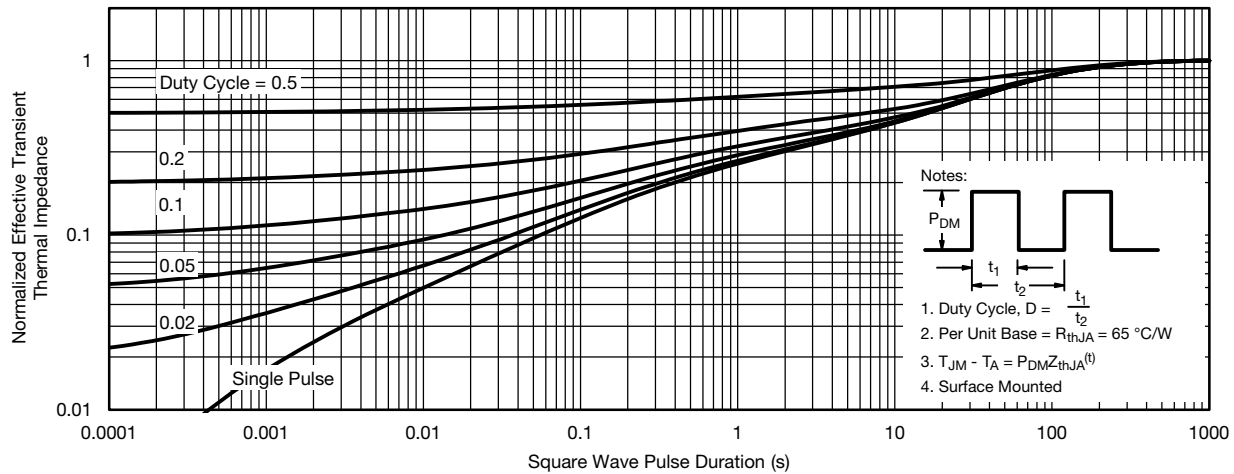
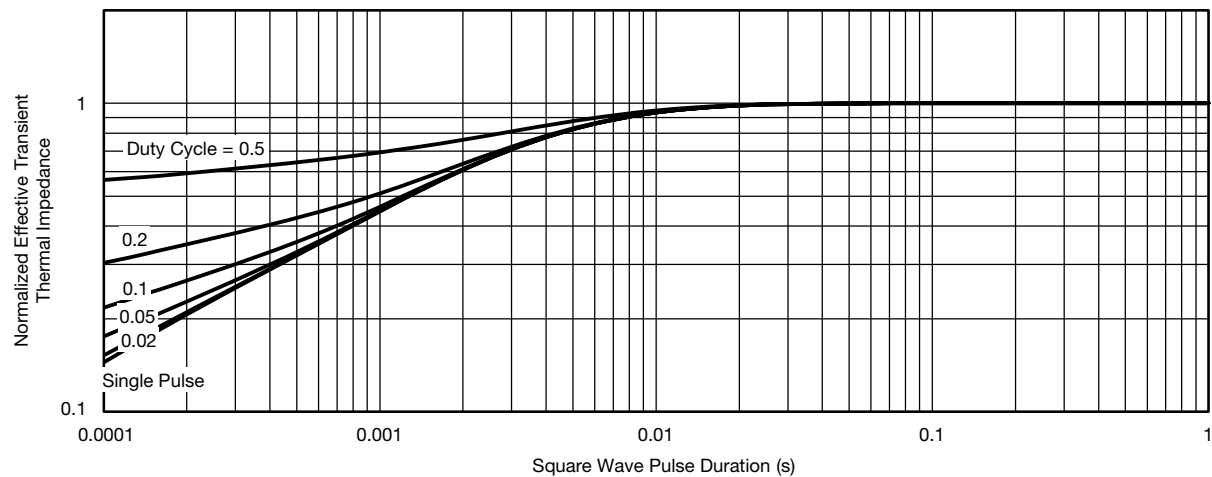

CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

SiZ920DT

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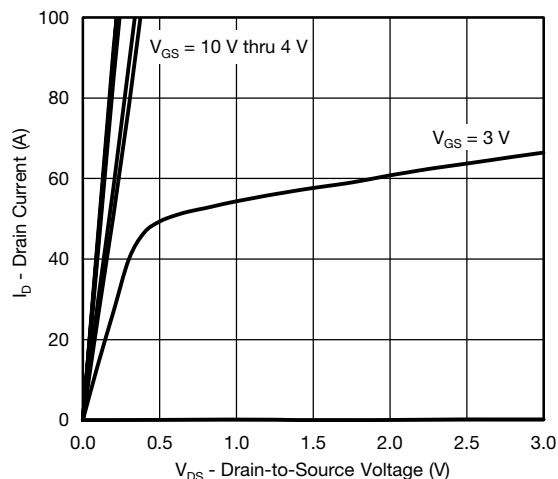
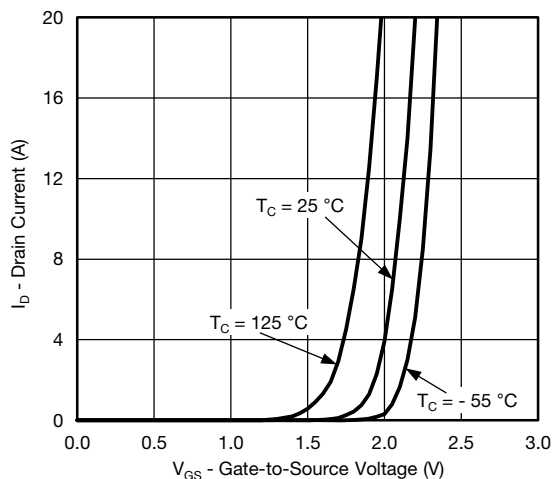
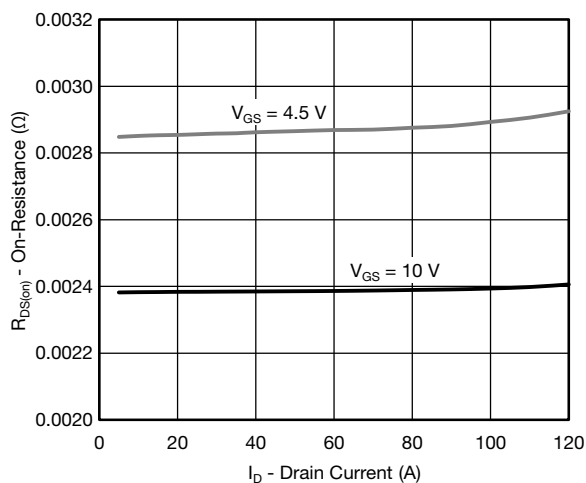
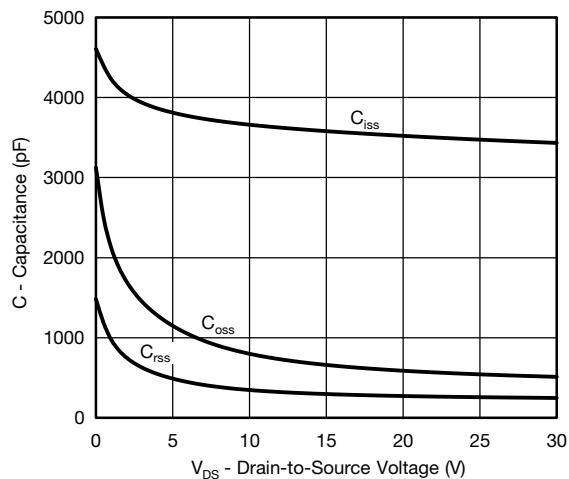
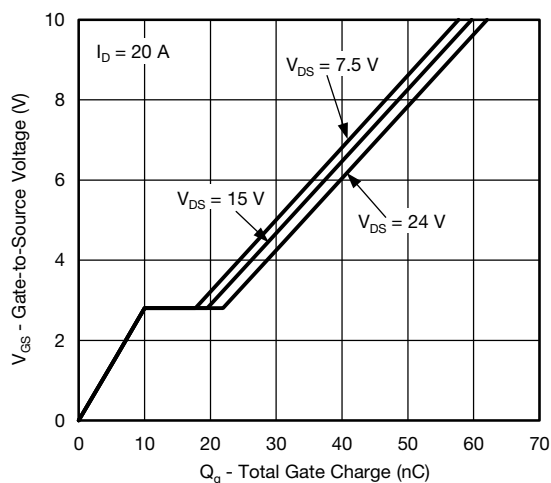
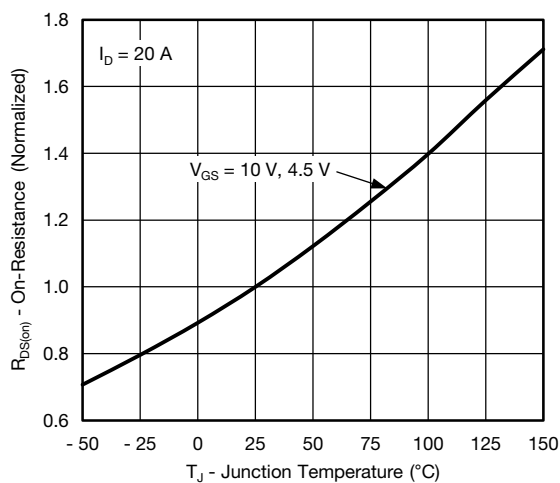
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Current Derating*****Power, Junction-to-Case****Power, Junction-to-Ambient**

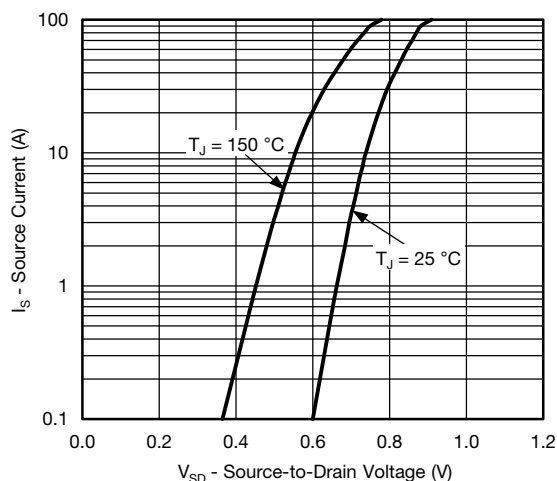
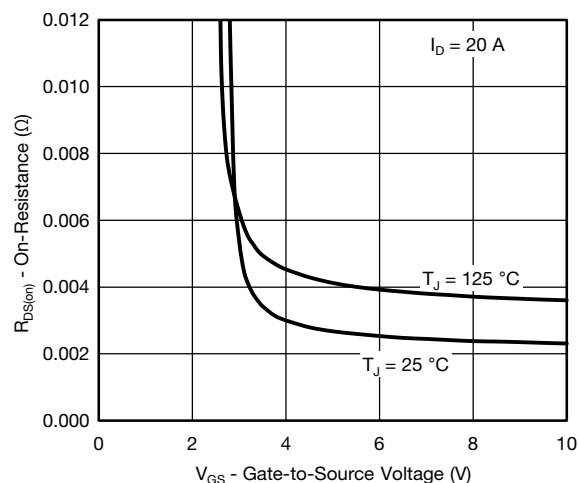
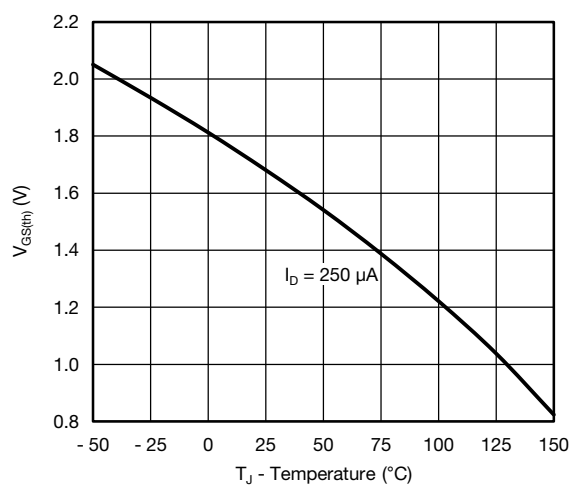
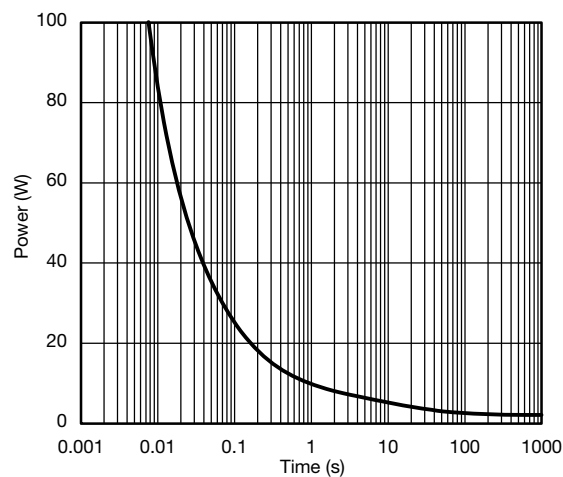
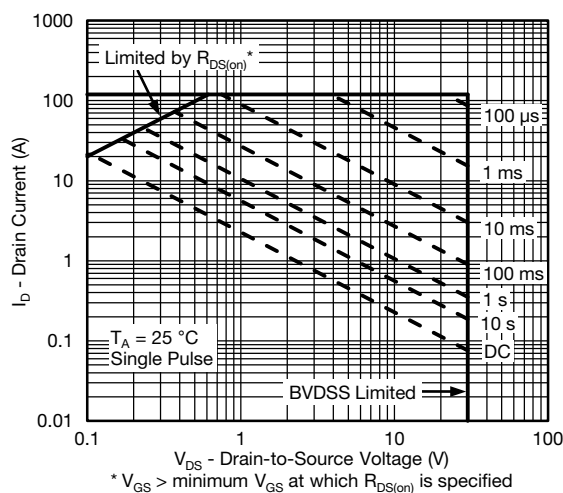
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

SiZ920DT

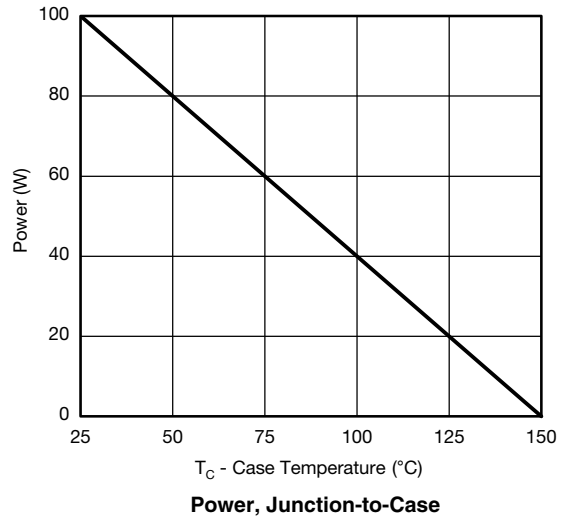
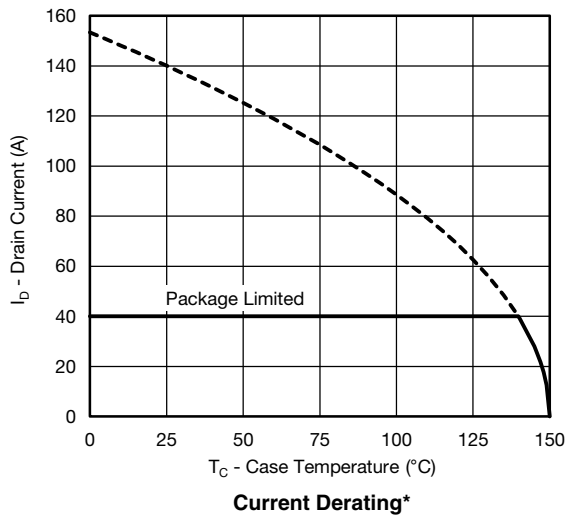
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**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

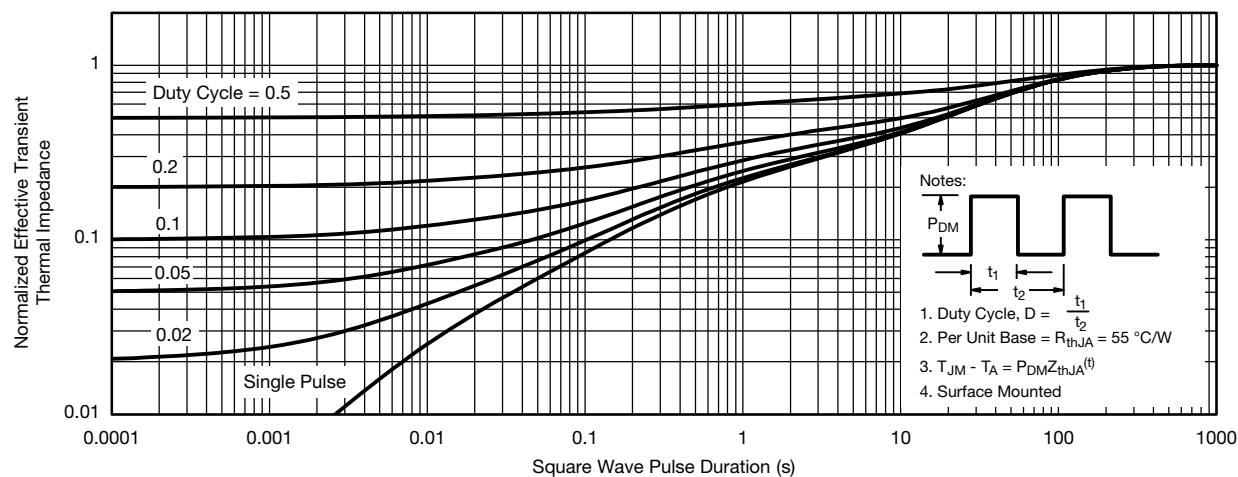
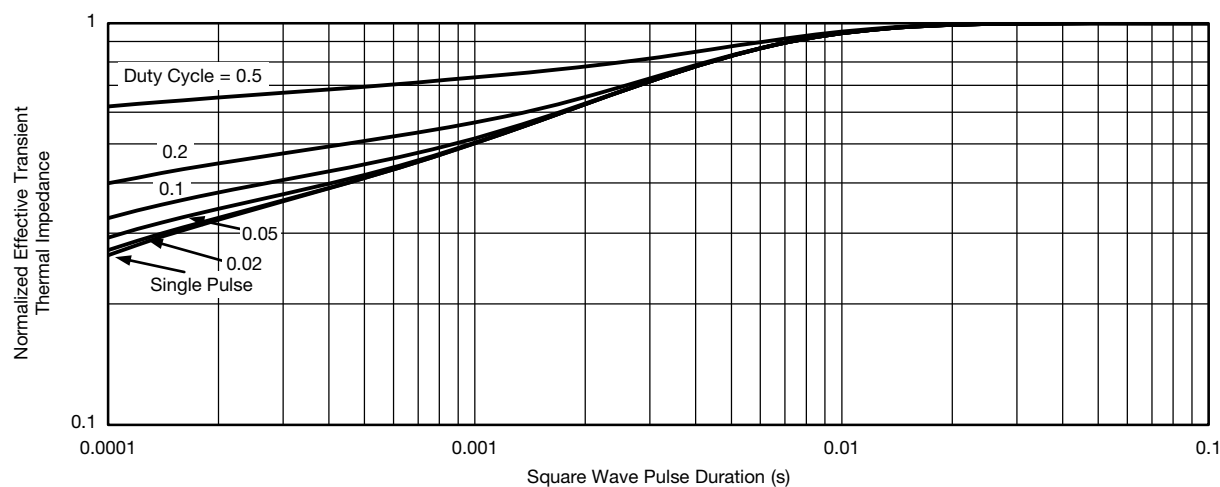

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power

Safe Operating Area, Junction-to-Ambient

SiZ920DT

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**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

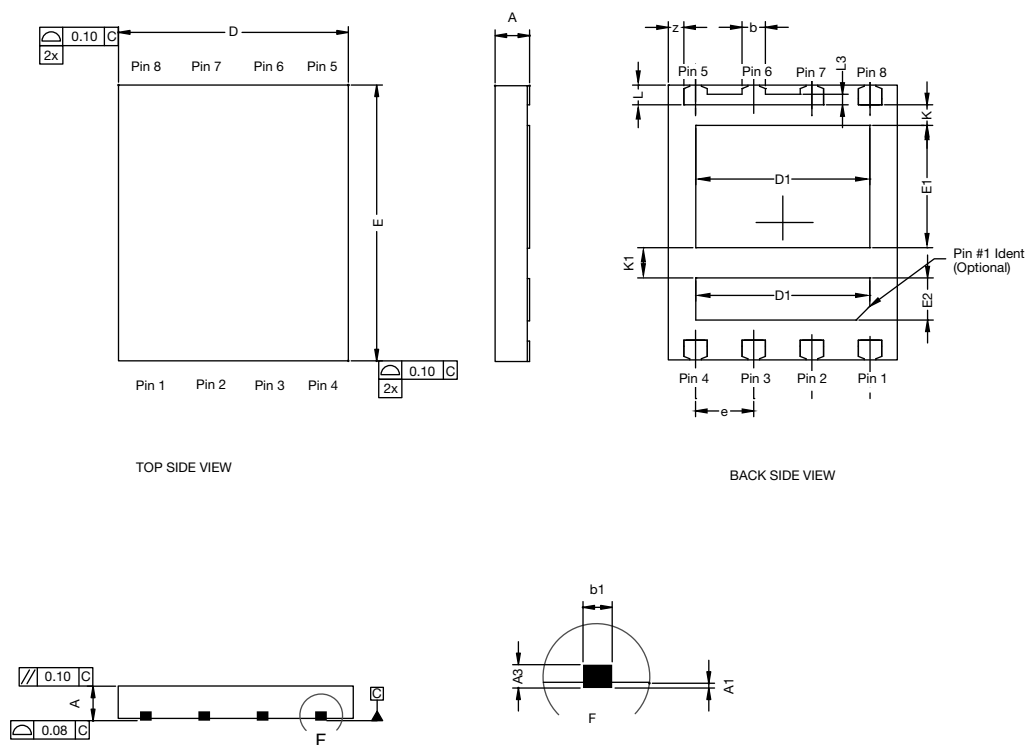
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63916.

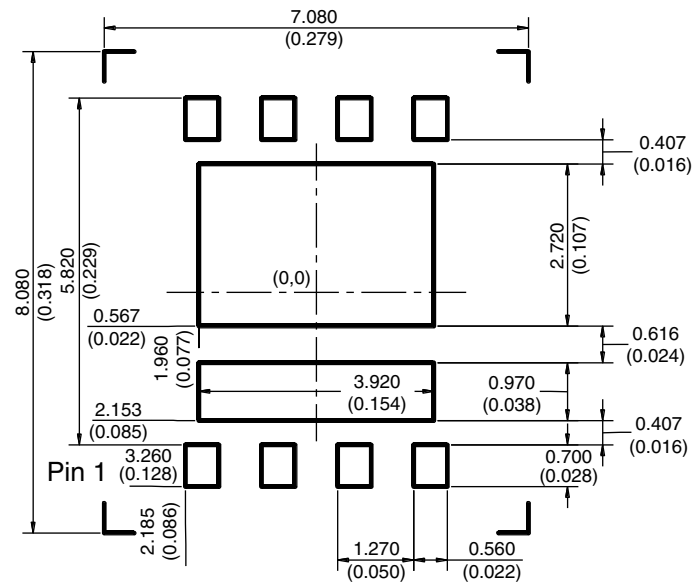


PowerPAIR® 6 x 5 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.20 REF			0.008 REF		
b	0.51 BSC			0.020 BSC		
b1	0.25 BSC			0.010 BSC		
D	5.00 BSC			0.197 BSC		
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	6.00 BSC			0.236 BSC		
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.005 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
L	0.43 BSC			0.017 BSC		
L3	0.23 BSC			0.009 BSC		
z	0.34 BSC			0.013 BSC		
ECN: C11-1242-Rev. A, 07-Nov-11 DWG: 6005						

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 6 x 5



Recommended Minimum Pad
Dimensions in mm (inches)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.