

TEST AND MEASUREMENT PRODUCTS

Description

The SK1904 is an extremely fast, stable, and accurate low skew 1:9 clock / signal distributor featuring a synchronous enable, which allows the outputs to be turned off and on without the risk of an unpredictable output pulse. The D - flip-flop is triggered on the falling edge of the clock.

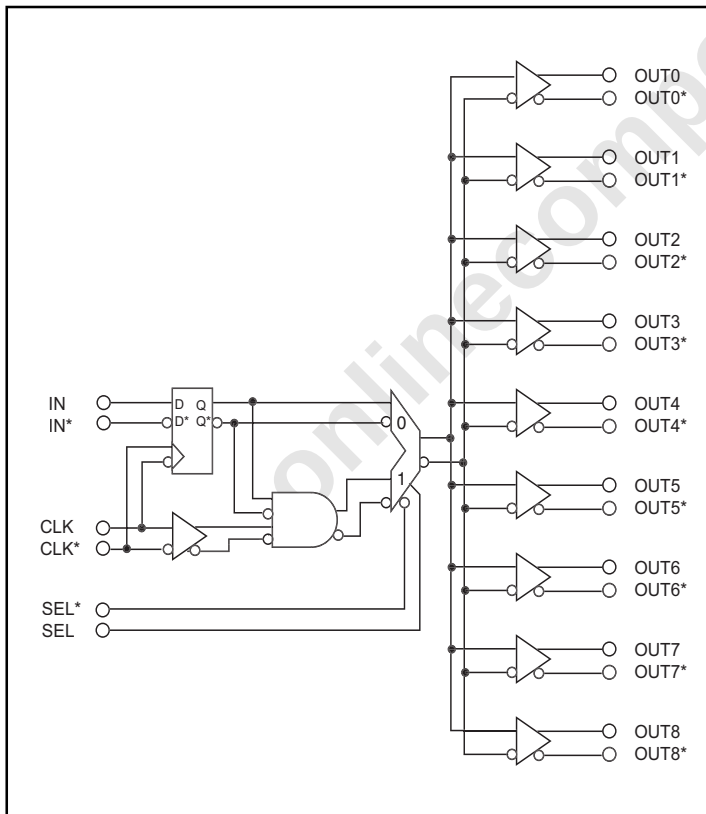
The SK1904 outputs are 50Ω with source and sink capability, optimized for:

- Point to point, series terminated, timing critical lines

Features

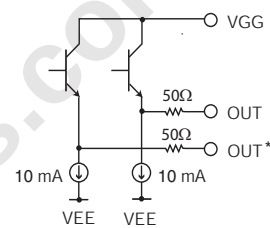
- 1:9 Clock/Data Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible
- Available in 32 pin, 5mm X5mm, TQFP Package

Functional Block Diagram



Output Option

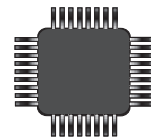
50Ω Source / Sink



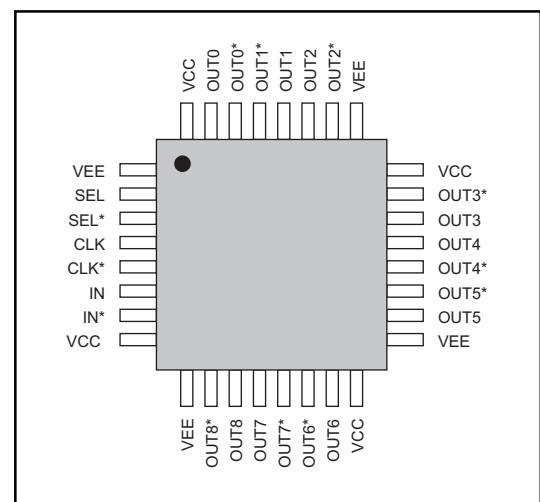
Package Information

32 pin, 5 mm X 5 mm

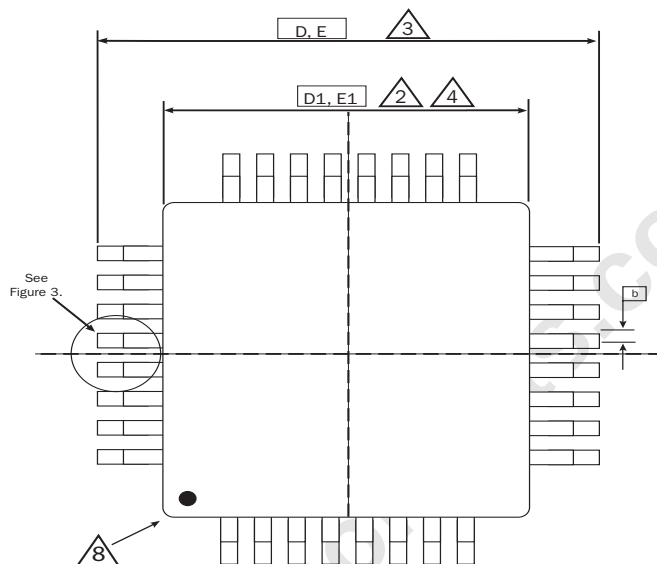
TQFP Package



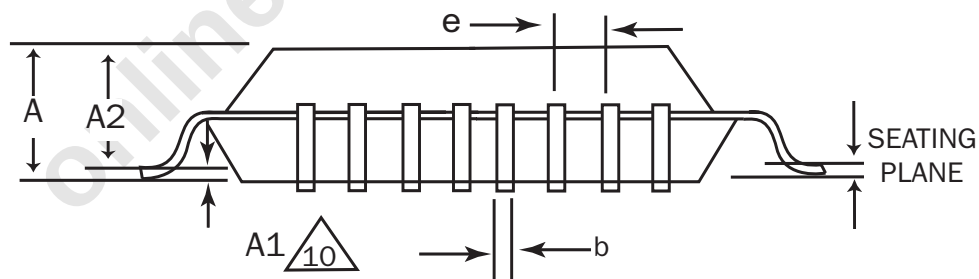
Pin Description



32 Pin, 5mm x 5mm TQFP Package



Top View



Side View

32 Pin, 5mm x 5mm TQFP Package

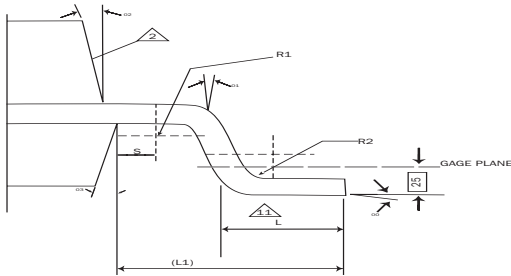


Figure 1.

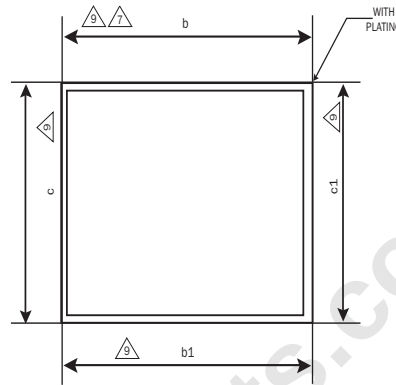


Figure 2.

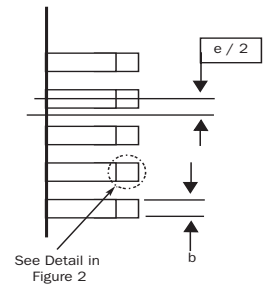


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation					
All Dimensions in Millimeters					
Symbol	MIN	NOM	MAX	Note	Comments
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D	7.00 BSC			3	
D1	5.00 BSC			4, 2	Package Body Length
E	7.00 BSC			3	
E1	5.00 BSC			4, 2	Package Body Width
N	32				Lead Count
e	0.50 BSC				Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	-	-		
R2	0.08	-	0.20		
00	0°	3.5°	7°		
01	0°	-	-		
02	11°	12°	13°		
03	11°	12°	13°		
S	0.20	-	-		
c	0.09	-	0.20		
c1	0.09	-	0.16		
L	0.45	0.60	0.75		
L1	1.00 REF				
aaa	0.20				
bbb	0.20				
ccc	0.08				
ddd	0.08				

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Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	- 8.0 to 0	V
V_{CC}	Power Supply ($V_{EE} = 0V$)	+8.0 to 0	V
V_I	Input Voltage	$V_{CC} \geq V_I \geq V_{EE}$	V
I_{OUT}	Output Current Continuous Surge	50 100	mA mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_{sol}	Solder Temperature (<2 to 3 seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

Note 1: Device is ESD sensitive and requires protective handling.

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DC Characteristics

($V_{CC} - V_{EE} = 3.0V$ to $5.5V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	V_{IH} V_{IL}	$V_{EE} + 2.0$ V_{EE}		V_{CC} $V_{CC} - 0.2$	V V
($IN - IN^*$, $CLK - CLK^*$, $SEL - SEL^*$) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK^*) Input High Current Input Low Current	I_{IH} I_{IL}	-5 -6		+30 +6	μA μA
Functional Inputs (IN / IN^* , SEL / SEL^*) Input Current	I_{IH} , I_{IL}	-500		+500	μA
Outputs					
Digital Output Voltage Output Common Mode Range Internal Current Source Output Impedance	$ OUT - OUT^* $ ($OUT + OUT^*$) / 2 I_{SINK} R_{OUT}	600 $V_{CC} - 1.4$ 7.5 40	700 $V_{CC} - 1.2$ 10 50	$V_{CC} - 1.0$ 13 60	mV V mA Ω
Power Supply					
Power Supply Current	I_{EE}			355	mA

Test Conditions: Outputs unterminated.

AC Characteristics

($V_{CC} - V_{EE} = 3.0V$ to $5.5V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay CLK to OUT ($SEL = 0$) CLK to OUT ($SEL = 1$) SEL to OUT	T_{pd} T_{pd} T_{pd}	485 300 300	630 450 450	785 600 600	ps ps ps
Channel to Channel Skew	t_{SKEW}			20	ps
Maximum Operating Frequency (Note 1)	F_{max}	3.0			GHz
Minimum Pulse Width (Note 1)	PW_{min}	250			ps
IN to CLK Set Up Time Hold Time	T_s T_h	100 100			ps ps
Output Rise and Fall Times (20% / 80%) (Note 1)	T_r / T_f		125	175	ps
Temperature Coefficient (Note 1)	$\Delta T_{pd} / \Delta T$		<1		$ps / ^{\circ}C$

AC TEST CONDITIONS: Outputs terminated with 50Ω to $V_{CC} - 2.0V$.

Note 1: Guaranteed by characterization. Not production tested.



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Ordering Information

Ordering Code	Package ID
SK1904ATF	32-TQFP 5 x 5 mm
SK1904ATF-T	Tape and Reel

Notes:

1. For Tape and Reel information, see TMD Part Ordering Information Data

Application Notes

AN1001- EPIC Family Product Line

AN1003- Termination Techniques for ECL / LVECL
PECL / LVPECL Devices

AN1004- Interfacing Between LVDS and
ECL / LVECL / PECL / LVPECL

Contact Information

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