

DATA SHEET

SKY13362-389LF: 0.4-2.7 GHz GaAs SP10T Switch

Applications

- 2G/3G multimode cellular handsets (UMTS, CDMA2000, EDGE, GSM)
- Embedded data cards

Features

- Broadband frequency range: 0.4 to 2.7 GHz
- Four CMOS/TTL control voltages (0/1.35 to 3.1 V)
- Single, positive DC power supply (2.7 to 3.3 V)
- Excellent triple beat ratio performance
- Integrated, low-pass harmonic filter for GSM transmit paths
- Integrated CMOS decoder
- Small QFN (26-pin, 3.0 x 3.8 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



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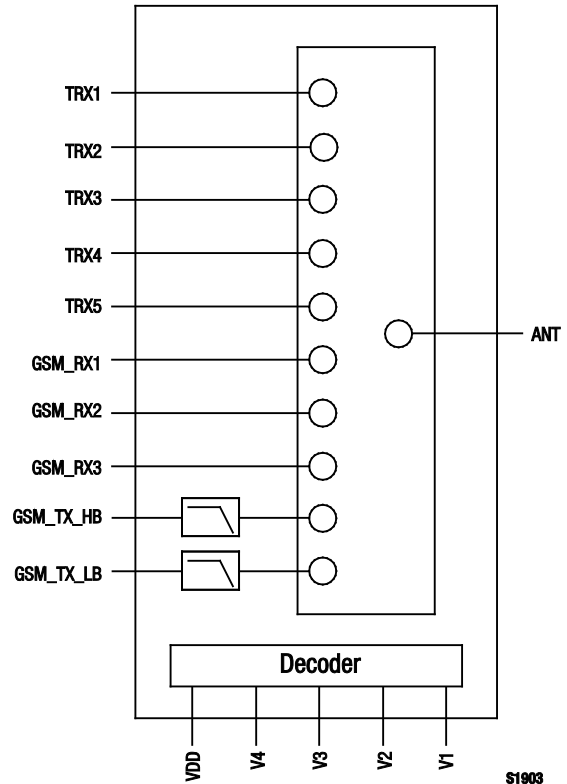


Figure 1. SKY13362-389LF Block Diagram

Description

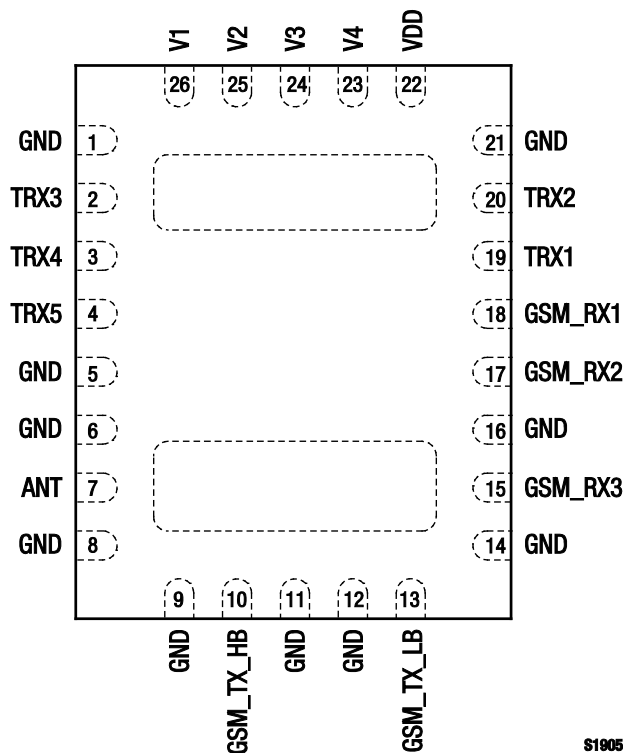
The SKY13362-389LF is a GaAs pHEMT single-pole, ten-throw (SP10T) antenna switch with an integrated CMOS decoder and dual low-pass harmonic filters. The switch has five transmit/receive ports that make it ideal for any combination of 2G/3G multimode cellular applications.

Using advance switching technologies, the SKY13362-389LF maintains low insertion loss and high isolation for both transmit and receive switching paths. The switch also exhibits an excellent triple beat ratio and 2nd/3rd order modulation distortion performance.

Switching is controlled by four CMOS/TTL-compatible control voltage inputs (V1, V2, V3, and V4). Depending on the logic voltage level applied to the control pins, the antenna pin is connected to one of ten switched RF ports using a low insertion loss path, while the paths between the antenna pin and the other RF pins are in a high isolation state. No external DC blocking capacitors are required on the RF paths.

The SKY13362-389LF is manufactured in a compact, 3.0 x 3.8 mm, 26-pin Quad Flat No-Lead (QFN) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



**Figure 2. SKY13362-389LF Pinout – 26-Pin QFN
(Top View)**

Table 1. SKY13362-389LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground	14	GND	Ground
2	TRX3	RF input/output port 3	15	GSM_RX3	GSM RF output port 3
3	TRX4	RF input/output port 4	16	GND	Ground
4	TRX5	RF input/output port 5	17	GSM_RX2	GSM RF output port 2
5	GND	Ground	18	GSM_RX1	GSM RF output port 1
6	GND	Ground	19	TRX1	RF input/output port 1
7	ANT	Antenna RF port	20	TRX2	RF input/output port 2
8	GND	Ground	21	GND	Ground
9	GND	Ground	22	VDD	DC power supply
10	GSM_TX_HB	GSM high band transmit RF input port with integrated harmonic filter	23	V4	DC input control voltage 4
11	GND	Ground	24	V3	DC input control voltage 3
12	GND	Ground	25	V2	DC input control voltage 2
13	GSM_TX_LB	GSM low band transmit RF input port with integrated harmonic filter	26	V1	DC input control voltage 1

Note: Bottom ground paddles must be connected to ground.

Table 2. SKY13362-389LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
RF input power	P _{IN}			+36	dBm
Power supply				5	V
Control voltage	V _{CTL}			3.3	V
Storage temperature	T _{STG}	–40		+125	°C
Operating temperature	T _{OP}	–30		+90	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Functional Description

To achieve optimum harmonic performance of GSM signal transmission, it is recommended to set the switch in “sleep” mode first, then apply control voltages, before RF power is applied. Refer to the Skyworks Application Note, *SKY13362-389LF SP10T Recommended Timing Sequence for Optimal GSM Transmit Harmonic Performance* (document number 201511) for detailed timing sequence recommendations.

The time from when V_{DD} is applied to when the switch is active is the startup time. Once the startup time has passed, the control voltages can be applied. RF power should not be applied during the startup time or damage to the device could result.

The recommended startup sequence is:

Step 1: Apply V_{DD}.

Step 2: Apply V1 to V4 voltages.

Step 3: Apply the RF input.

Recommended startup time is 25 μ s.

The device must be turned off in the reverse order.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13362-389LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY13362-389LF are illustrated in Figures 3 to 19.

The state of the SKY13362-389LF is determined by the logic provided in Table 4.

Figure 20 illustrates the test setup used to measure data for Figure 17. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX5 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

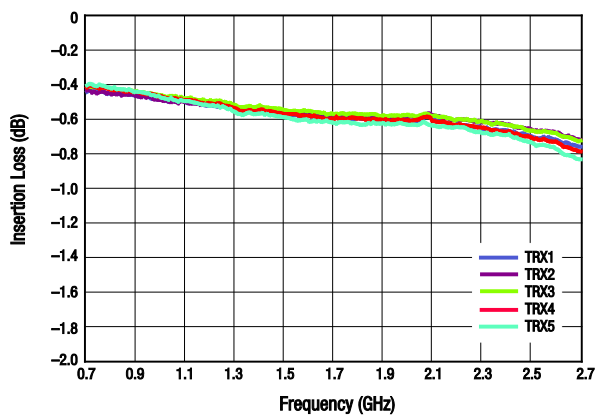
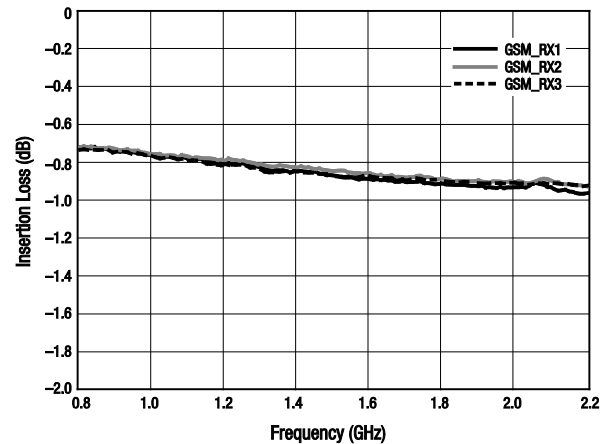
The resulting 3rd Order Intermodulation Distortion (IMD3), f_{rx}, is measured over all phases of f_{FUND}. The SKY13362-389LF exhibits exceptional performance for all TRX ports.

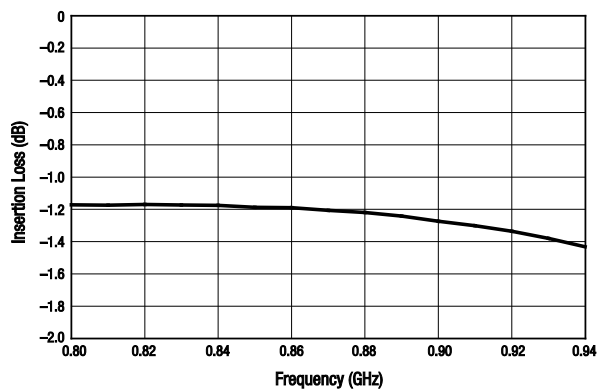
Table 3. SKY13362-389LF Electrical Specifications (Note 1) (1 of 2)**(V_{DD} = 2.85 V, V₁ = V₂ = V₃ = V₄ = 0/1.8 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss: ANT to TRX1/2 ports	IL	824 to 960 MHz		0.5	0.7	dB
		1710 to 2170 MHz		0.6	0.8	dB
		2300 to 2690 MHz		0.8	1.0	dB
Insertion loss: ANT to TRX3/4/5 ports	IL	824 to 960 MHz		0.50	0.70	dB
		1710 to 2170 MHz		0.65	0.85	dB
		2300 to 2690 MHz		0.85	1.05	dB
Insertion loss: ANT to GSM_TX_LB port	IL	824 to 915 MHz		1.35	1.55	dB
Insertion loss: ANT to GSM_TX_HB port	IL	1710 to 1910 MHz		1.2	1.4	dB
Insertion loss: ANT to GSM_RX1/2/3 ports	IL	869 to 960 MHz		0.8	1.0	dB
		1805 to 1990 MHz		1.0	1.2	dB
Isolation (TRX1/2 to TRX3/4/5 ports)	ISO	824 to 1910 MHz	32	35		dB
Isolation (GSM_TX_LB to TRX1/23/4/5 and GSM_RX1/2/3 ports)	ISO	824 to 915 MHz	35	38		dB
Isolation (GSM_TX_HB to TRX1/23/4/5 and GSM_RX1/2/3 ports)	ISO	1710 to 1910 MHz	32	35		dB
Isolation (TRX3 to TRX5 port)	ISO	824 to 1910 MHz	25	28		dB
Isolation (TRX1 to TRX2, TRX3 to TRX4, TRX4 to TRX5 ports)	ISO	824 to 1910 MHz	18	21		dB
Isolation (ANT to GSM_RX2/3 ports)	ISO	1805 to 1990 MHz	30	33		dB
Harmonics		UMTS, P _{IN} = +27 dBm		-48	-36	dBm
		GSM_TX_LB port, P _{IN} = +35 dBm		-45	-36	dBm
		GSM_TX_HB port, P _{IN} = +33 dBm		-44	-36	dBm
Attenuation (GSM_TX_LB port)		GSM850				
		2f	18	22		dB
		3f	25	28		dB
		>4f		20		dB
		EGSM900				
		2f	22	25		dB
Attenuation (GSM_TX_HB port)		DCS1800				
		2f	20	25		dB
		3f	25	28		dB
		>4f		20		dB
		PCS1900				
		2f	22	25		dB
Return loss	IS111	0.4 to 2.2 GHz	14	18		dB

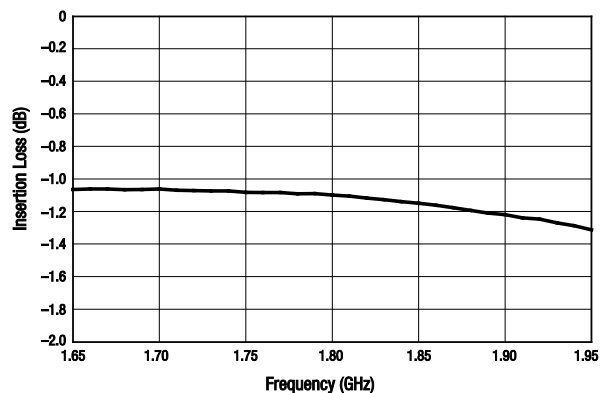
Table 3. SKY13362-389LF Electrical Specifications (Note 1) (2 of 2)**($V_{DD} = 2.85\text{ V}$, $V_1 = V_2 = V_3 = V_4 = 0/1.8\text{ V}$, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\text{ }\Omega$, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications (continued)						
2 nd Order Input Intercept Point	IIP2	AWS, PCS, IMT to CDMA2000 modes	+95.5			dBm
2 nd Order Intermodulation Distortion	IMD2	UMTS mode		-105	-97	dBm
3 rd Order Intermodulation Distortion	IMD3	UMTS mode		-105	-97	dBm
Triple Beat Ratio	TBR	650 to 900 MHz		81		dBc
		1710 to 2155 MHz		81		dBc
1 dB Input Compression Point	IP1dB	GSM_TX_LB port, 824 to 915 MHz	+40			dBm
		GSM_TX_HB port, 1710 to 1910 MHz	+39			dBm
Switching speed		10/90% RF		3	5	μs
DC Specifications						
Supply voltage	V_{DD}		2.70	2.85	3.30	V
Supply current	I_{DD}			0.5	0.6	mA
Supply current (sleep mode)	I_{DD}			1		μA
Control voltage: High Low	V_1, V_2, V_3, V_4		1.35	1.80	3.10	V
			0		0.3	V
Control current: High Low					10	μA
				5		μA

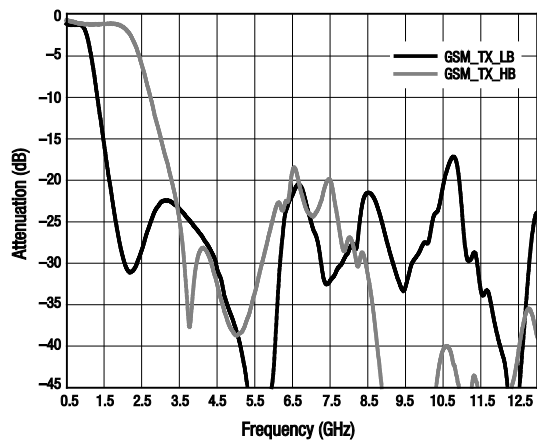
Note 1: Performance is guaranteed only under the conditions listed in this Table.**Typical Performance Characteristics****($V_{DD} = 2.85\text{ V}$, $V_1 = V_2 = V_3 = V_4 = 0/1.8\text{ V}$, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\text{ }\Omega$, Unless Otherwise Noted)****Figure 3. Insertion Loss vs Frequency
(ANT to TRX Ports)****Figure 4. Insertion Loss vs Frequency
(ANT to GSM_RX Ports)**



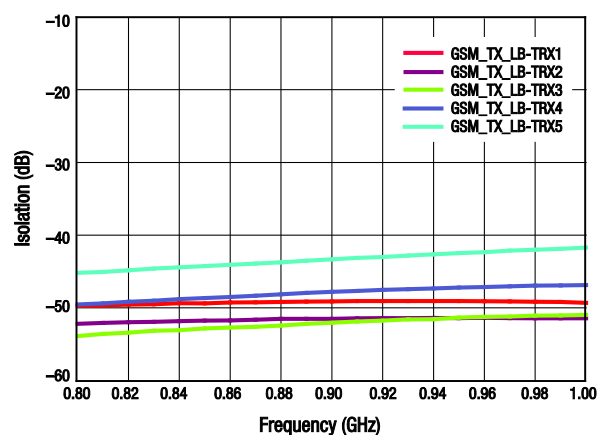
**Figure 5. Insertion Loss vs Frequency
(ANT to GSM_TX_LB Port)**



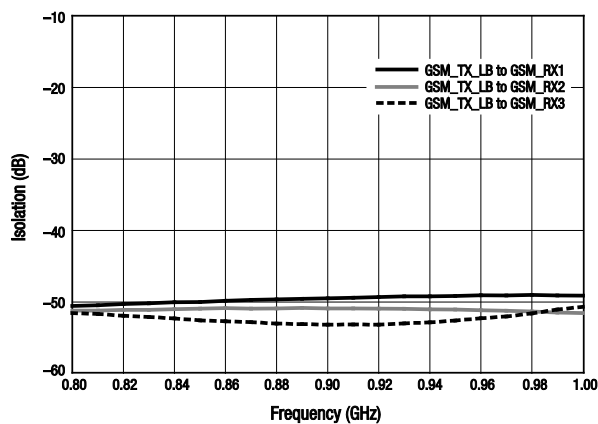
**Figure 6. Insertion Loss vs Frequency
(ANT to GSM_TX_HB Port)**



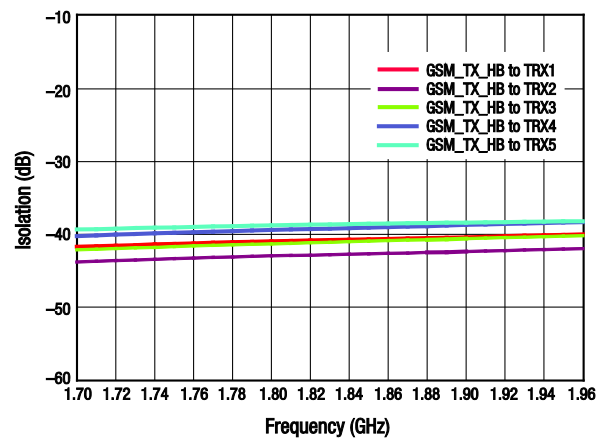
**Figure 7. Attenuation vs Frequency
(ANT to GSM_TX_HB/LB Ports)**



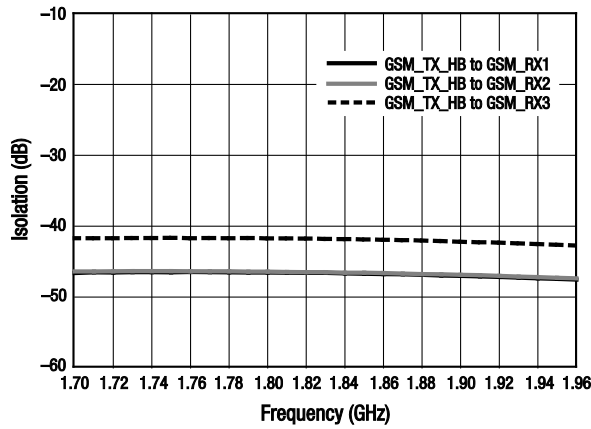
**Figure 8. Isolation vs Frequency
(GSM_TX_LB to TRX Ports)**



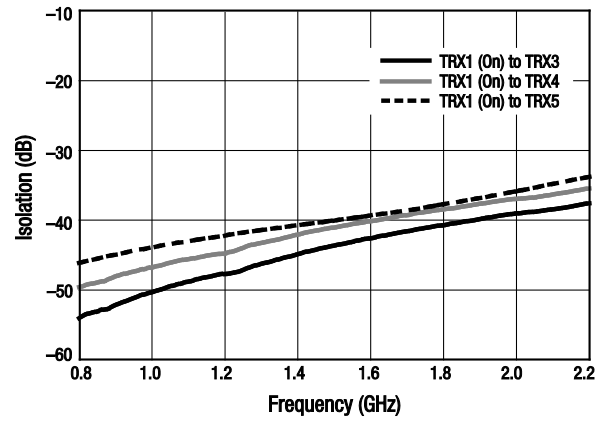
**Figure 9. Isolation vs Frequency
(GSM_TX_LB to GSM_RX1/2/3 Ports)**



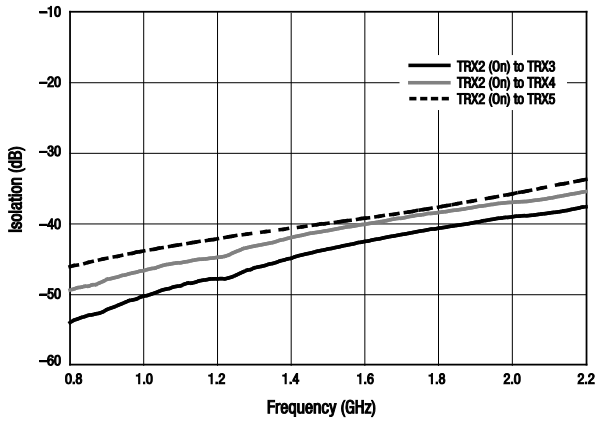
**Figure 10. Isolation vs Frequency
(GSM_TX_HB to TRX Ports)**



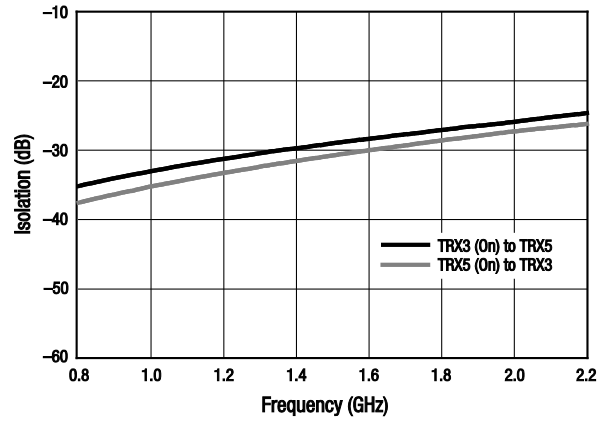
**Figure 11. Isolation vs Frequency
(GSM_TX_HB to GSM_RX1/2/3 Ports)**



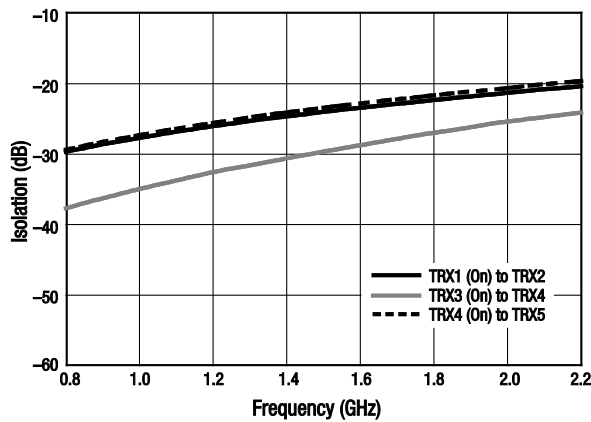
**Figure 12. Isolation vs Frequency
(TRX1 to TRX3/4/5 Ports)**



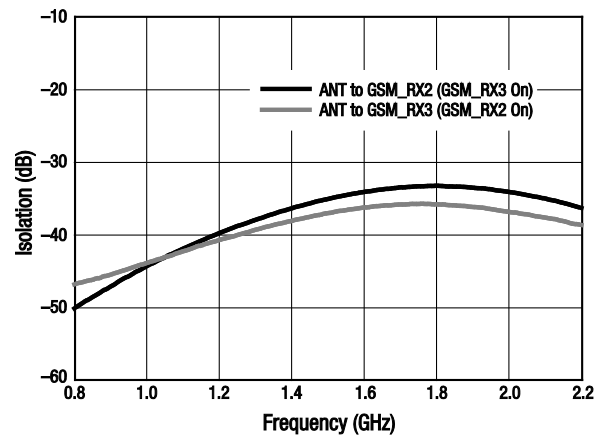
**Figure 13. Isolation vs Frequency
(TRX2 to TRX3/4/5 Ports)**



**Figure 14. Isolation vs Frequency
(TRX3 to TRX5 Port)**



**Figure 15. Isolation vs Frequency
(TRX Adjacent Ports)**



**Figure 16. Isolation vs Frequency
(ANT to GSM_RX1/2/3 Ports)**

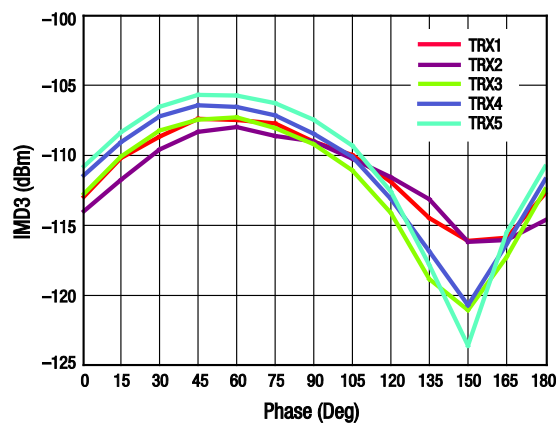


Figure 17. 3rd Order Intermodulation Distortion vs Phase, TRX Ports ($f_{\text{FUND}} = 1.95 \text{ GHz}$, $f_{\text{BLK}} = 1.76 \text{ GHz}$, $f_{\text{RX}} = 2.14 \text{ GHz}$)

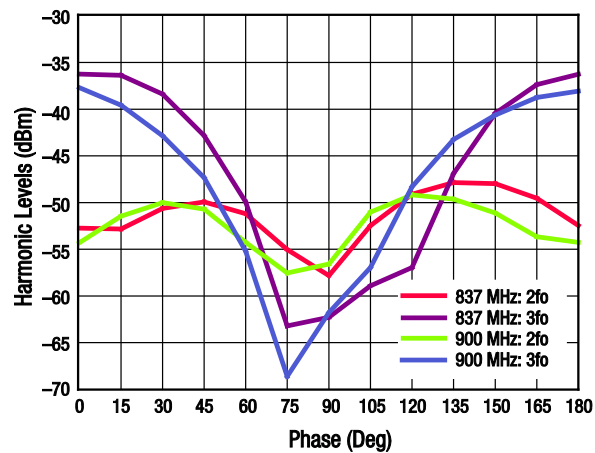


Figure 18. Harmonics vs Phase
(ANT to GSM_TX_LB, $P_{\text{IN}} = +35 \text{ dBm}$, 5:1 VSWR Mismatch)

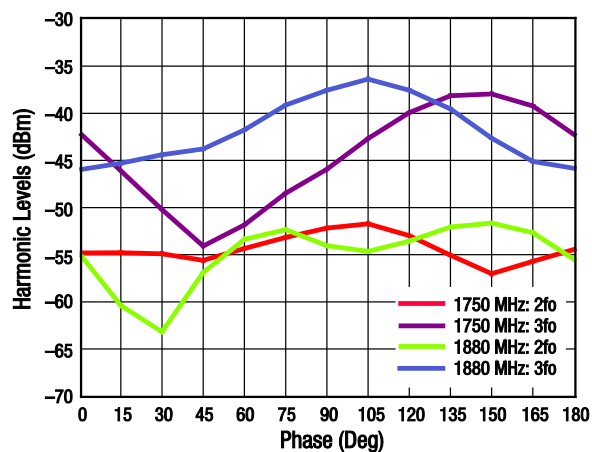
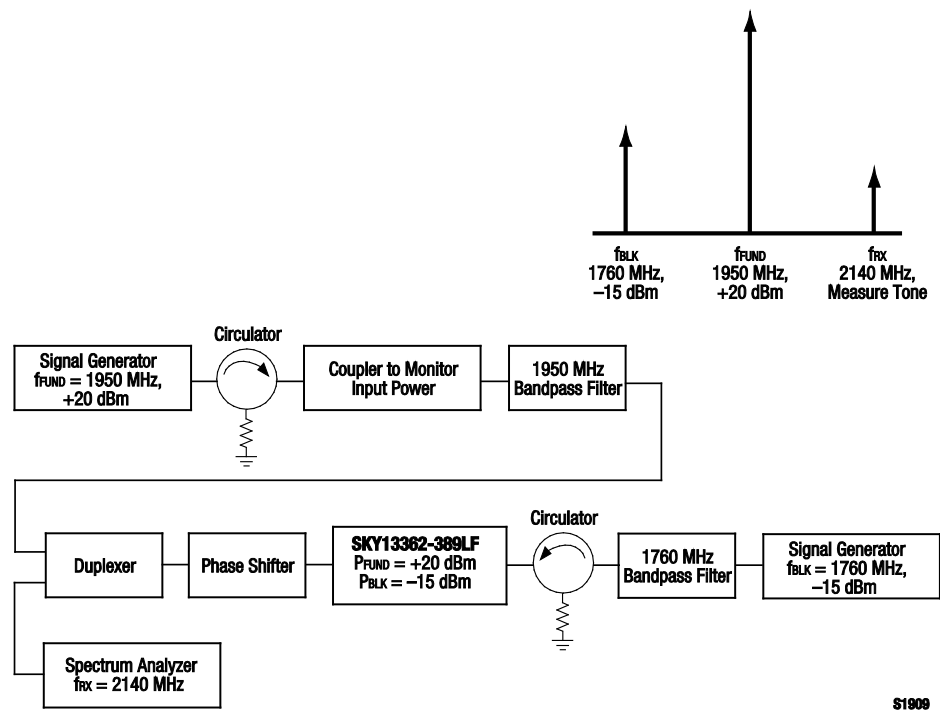


Figure 19. Harmonics vs Phase
(ANT to GSM_TX_HB, $P_{\text{IN}} = +33 \text{ dBm}$, 5:1 VSWR Mismatch)

Table 4. SKY13362-389LF Truth Table

Insertion Loss State	V1 (Pin 26)	V2 (Pin 25)	V3 (Pin 24)	V4 (Pin 23)
Sleep state (all ports in isolation state)	0	0	0	0
ANT to GSM_TX_LB	1	1	0	0
ANT to GSM_TX_HB	1	0	0	0
ANT to GSM_RX1	0	0	1	0
ANT to GSM_RX2	0	1	1	0
ANT to GSM_RX3	0	1	0	0
ANT to TRX1	1	0	1	0
ANT to TRX2	1	1	1	0
ANT to TRX3	1	0	1	1
ANT to TRX4	1	1	1	1
ANT to TRX5	1	0	0	1

Note: “1” = +1.35 V to +3.10 V (1.8 V typical). “0” = 0 V to +0.3 V. Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.



Evaluation Board Description

The SKY13362-389LF Evaluation Board is used to test the performance of the SKY13362-389LF SP10T Switch. An Evaluation Board schematic diagram is provided in Figure 21. Recommended ESD protection circuits are illustrated in Figure 22. An assembly drawing for the Evaluation Board is shown in Figure 23.

Package Dimensions

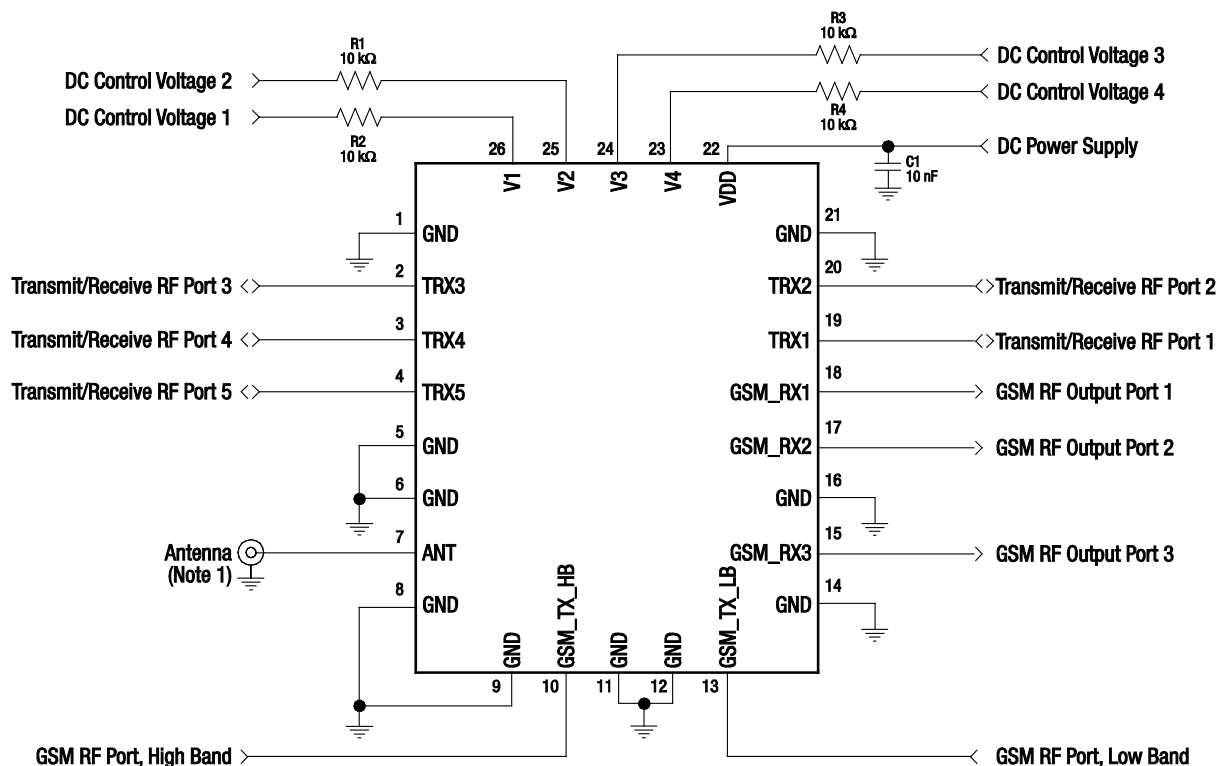
The PCB layout footprint for the SKY13362-389LF is provided in Figure 24. Typical case markings are shown in Figure 25. Package dimensions for the 26-pin QFN are shown in Figure 26, and tape and reel dimensions are provided in Figure 27.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY13362-389LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

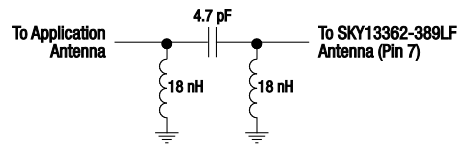
Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



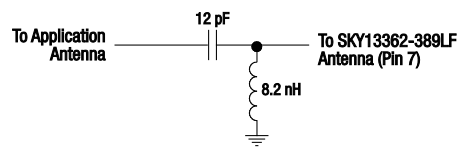
Note 1: See Figure 22 for recommended ESD protection circuit.

S1906

Figure 21. SKY13362-389LF Evaluation Board Schematic



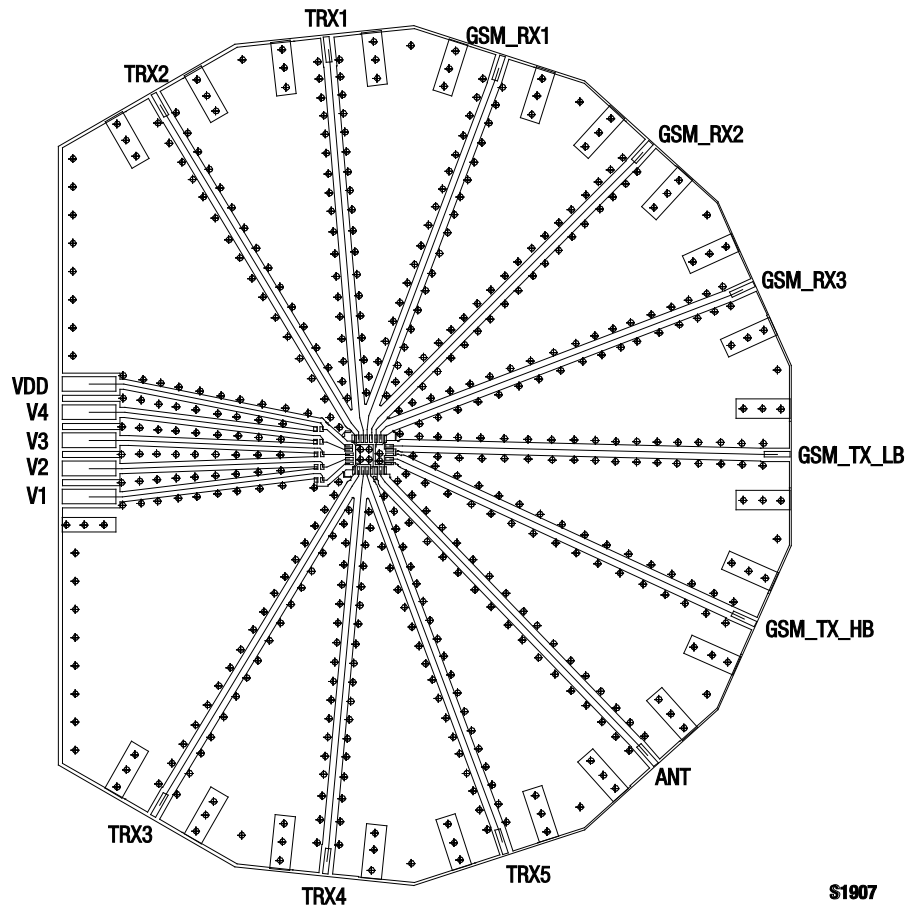
ESD Circuit 1



ESD Circuit 2

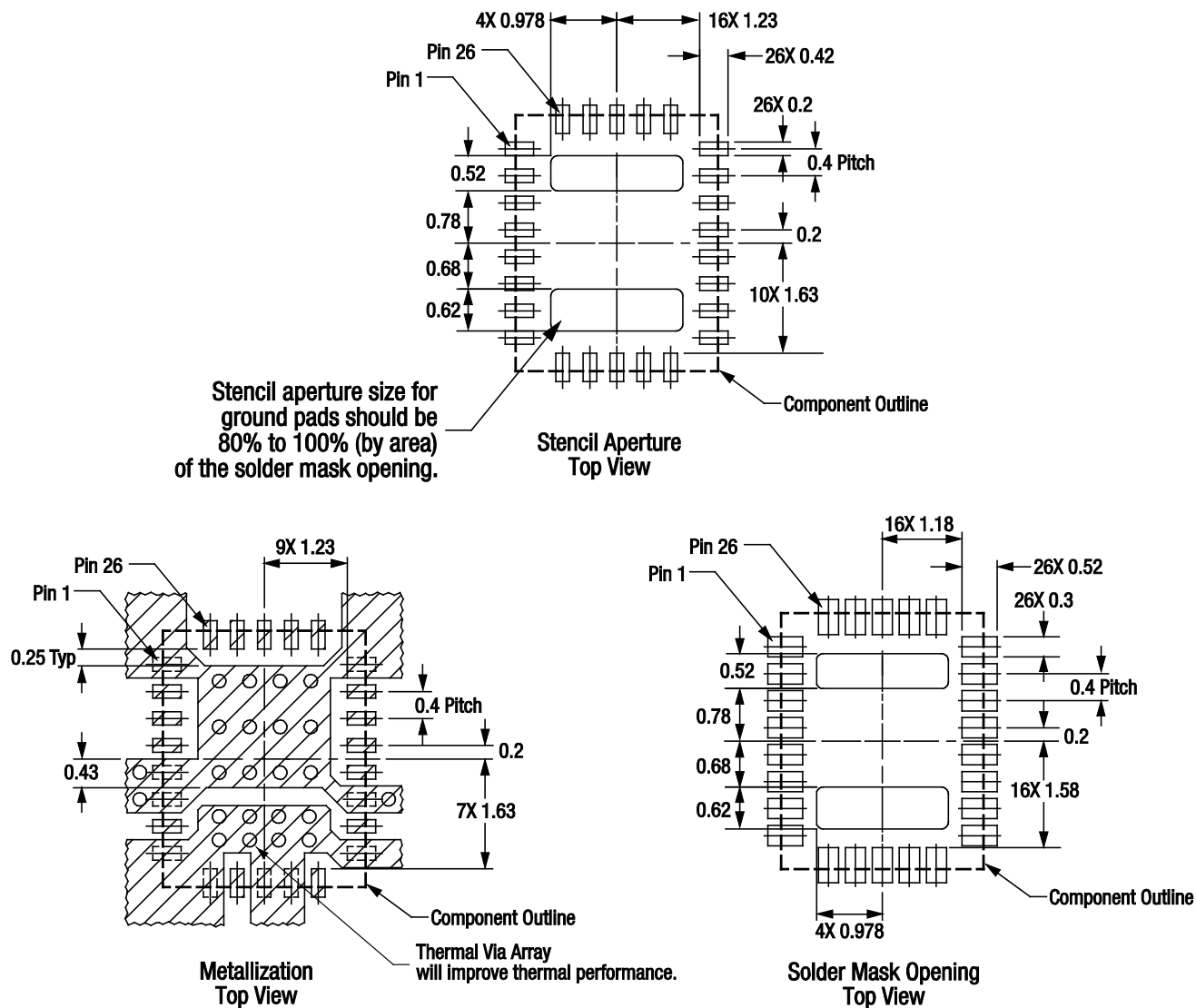
S2417

Figure 22. Recommended ESD Protection Circuits



S1907

Figure 23. SKY13362-389LF Evaluation Board Assembly Diagram



All dimensions are in millimeters

S2144

Figure 24. SKY13362-389LF PCB Layout Footprint (Top View)

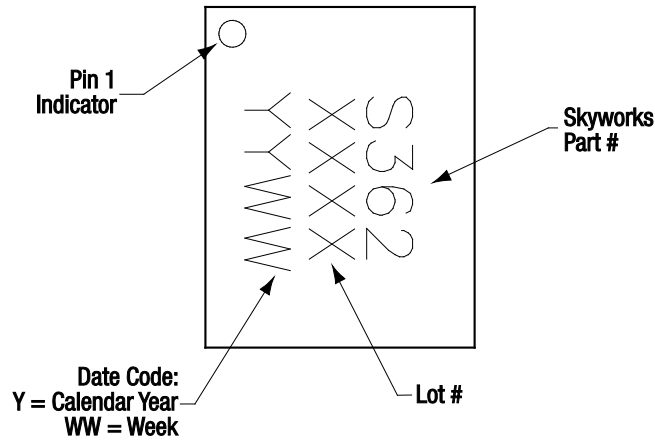
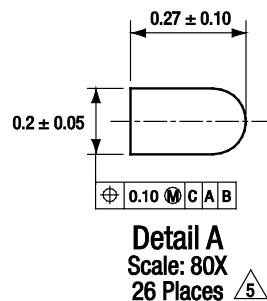
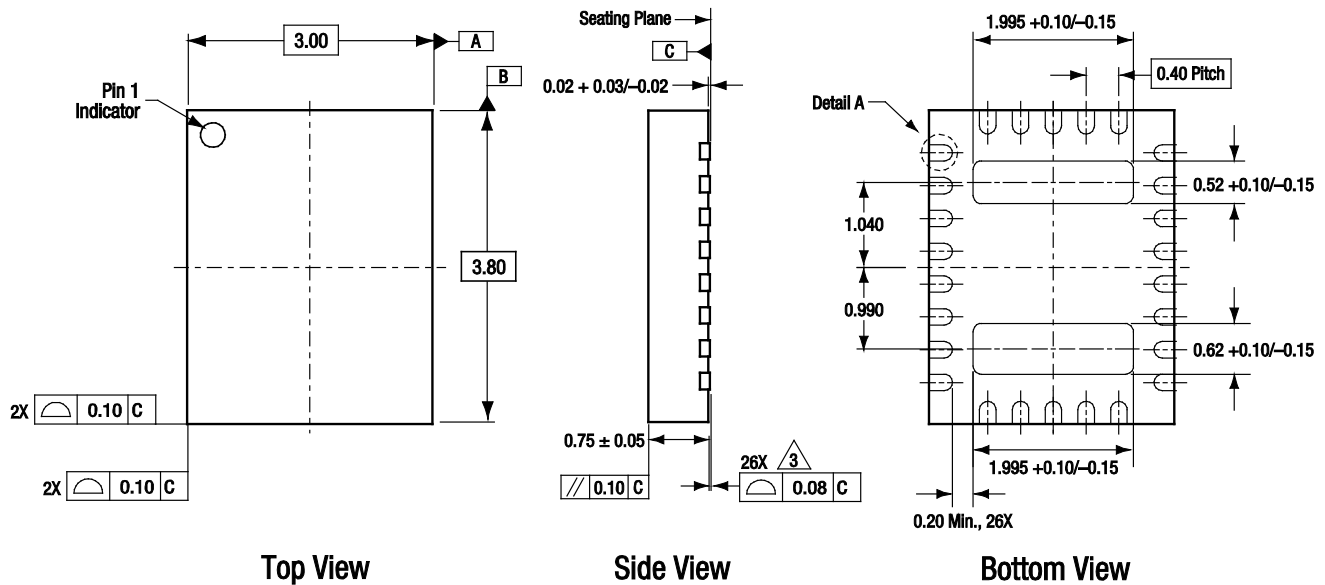


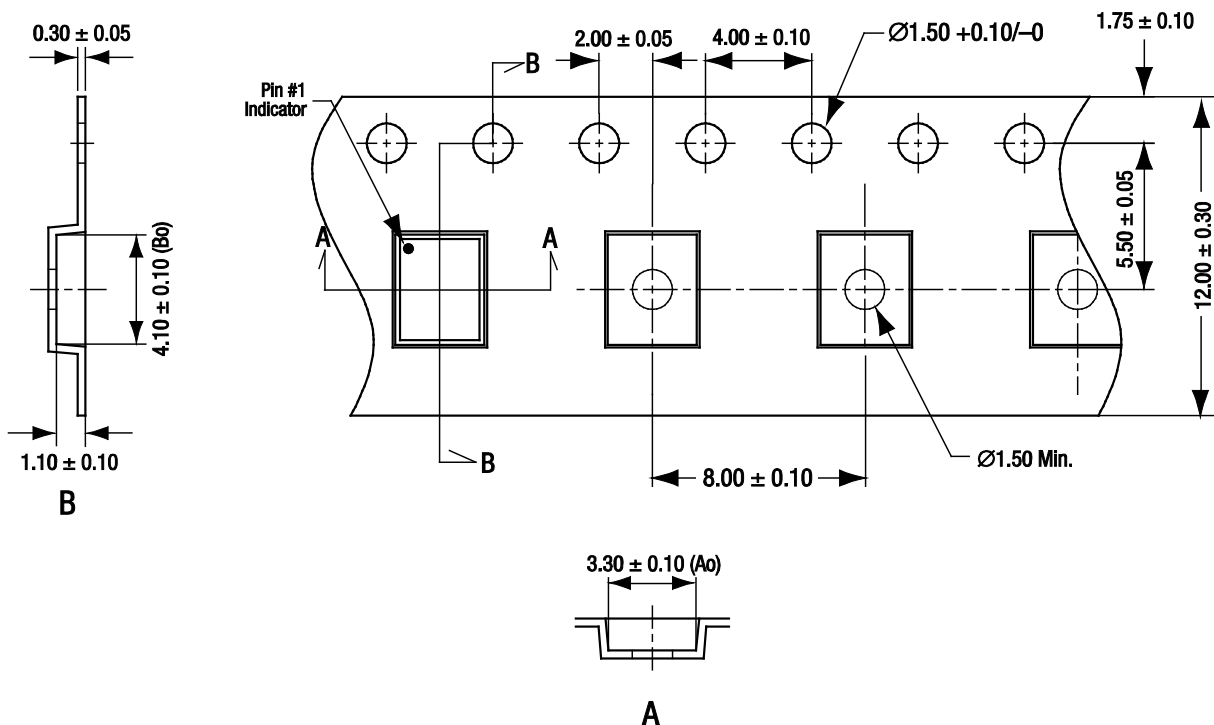
Figure 25. Typical Part Markings (Top View)



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed bottom surface metalization, as well as the terminals.
Plating requirement per source control drawing (SCD) 2504.

S1904

Figure 26. SKY13362-389LF 26-Pin QFN Package Dimensions



Notes:

1. Carrier tape: black conductive polystyrene.
2. Cover tape material: transparent conductive PSA.
3. ESD-surface resistivity is $\leq 1 \times 10^{10}$ Ohms/square per EIA, JEDEC TNR Specification.
4. Ten sprocket hole pitch cumulative tolerance: ± 0.20 mm.
5. Ao and Bo measured on plane 0.30 mm above the bottom of the pocket.
6. All measurements are in millimeters.

S2141

Figure 27. SKY13362-389LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13362-389LF 0.4-2.2 GHz SP10T Switch	SKY13362-389LF	SKY13362-389LF-EVB

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