

SL6601

FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

FEATURES

- High Sensitivity: 2 μ V Typical
- Low Power: 2-3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

ORDERING INFORMATION

SL6601 C DG
SL6601 C DP
SL6601 C LC

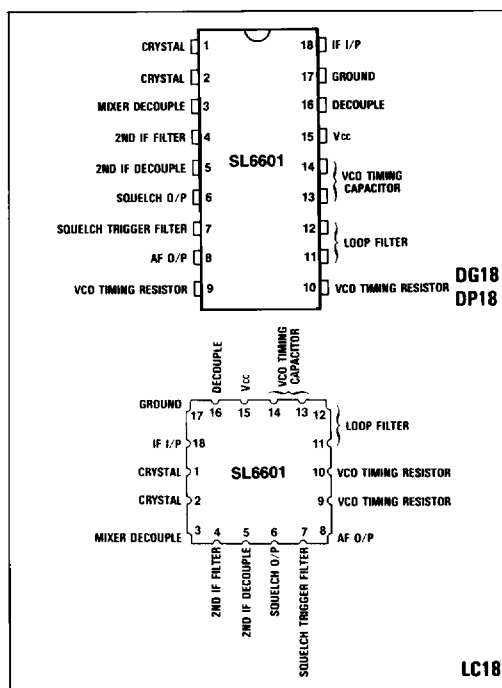


Fig.1 Pin connections - top view

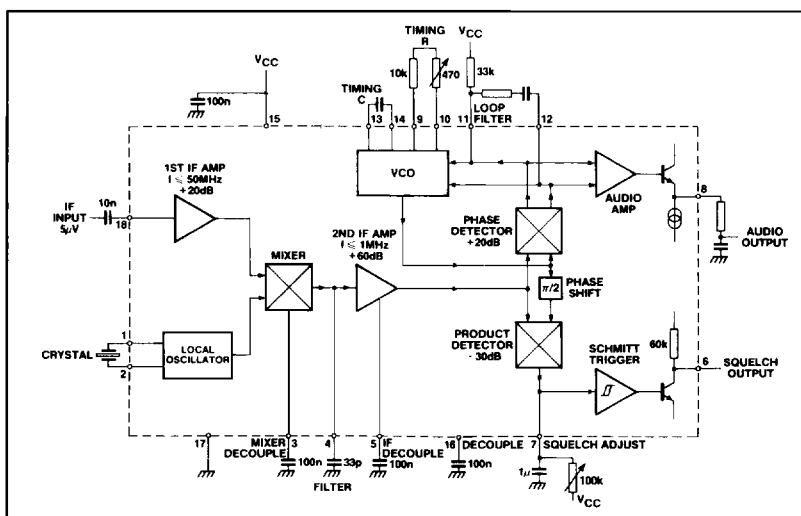


Fig.2 SL6601 block diagram

SL6601

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let $f_n = 6\text{kHz}$ and $D = 0.5$

Then from the graph

$$\frac{\Phi_{efn}}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85 \Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5 \frac{\Phi_{efn}}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set $f_n = 7.5\text{kHz}$

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_{efn}}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$K_o K_D = 0.3f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu\text{s}$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu\text{s}$$

$$t_1 = 22.5\mu\text{s}$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125\text{nF (use 1nF)}$$

$$R = \frac{t_2}{\frac{1}{20 \times 10^3}} = \frac{4.5}{22.5} \times 20 \times 10^3 = 4\text{k}\Omega \text{ (use 3.9k)}$$

Actual loop parameters can now be recalculated

$$t_1 = 20\mu\text{s} \quad t_2 = 3.9\mu\text{s}$$

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$$2\pi f_n = \frac{(K_o K_D)}{(t_1 \times t_2)} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1\text{k rad/sec} = 7.97\text{kHz}$$

$$D = f_n(t_2 + \frac{1}{K_o K_D}) = \frac{0.515}{K_o K_D}$$

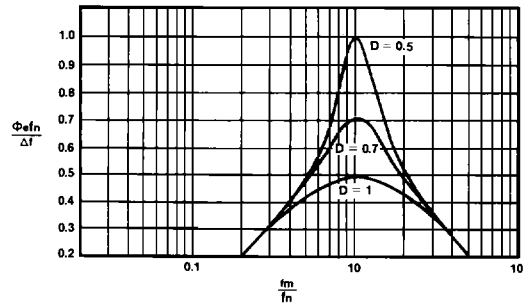


Fig.3 Damping factor

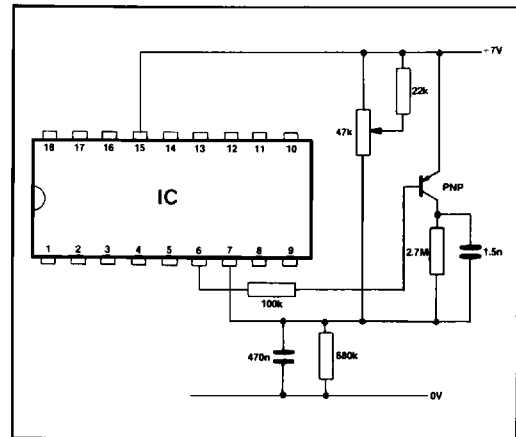


Fig.4 Using an external PNP in the squelch circuit

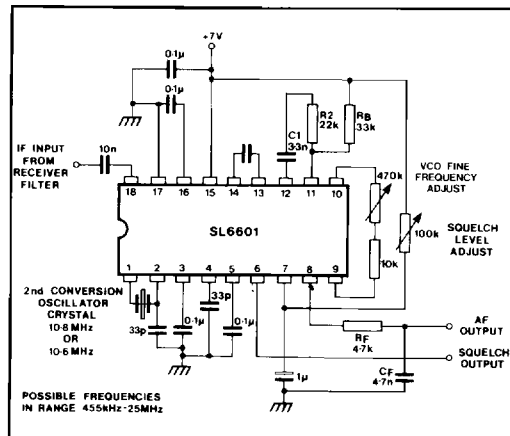


Fig.5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

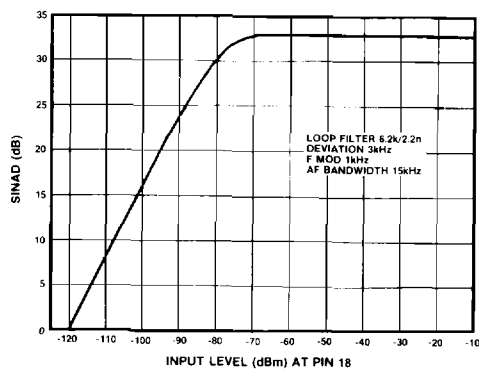


Fig. 6 Typical SINAD
(signal + noise + distortion/noise - distortion)

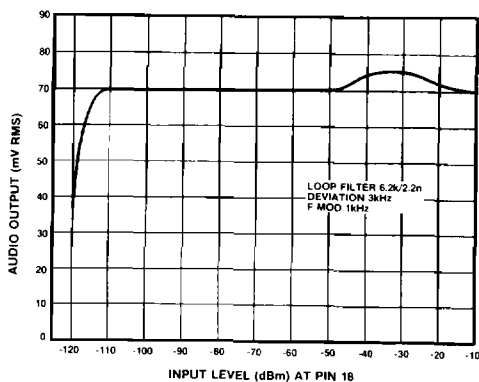


Fig. 7 Typical recovered audio v. input level (3kHz deviation)

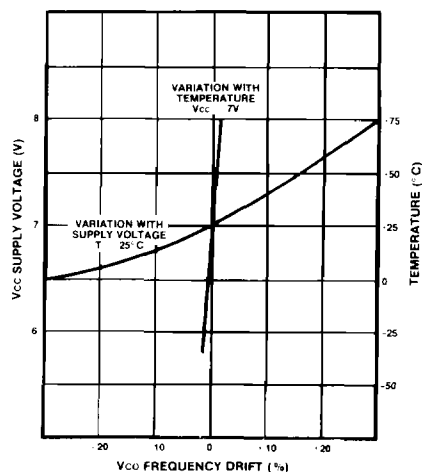


Fig. 9 Typical VCO characteristics

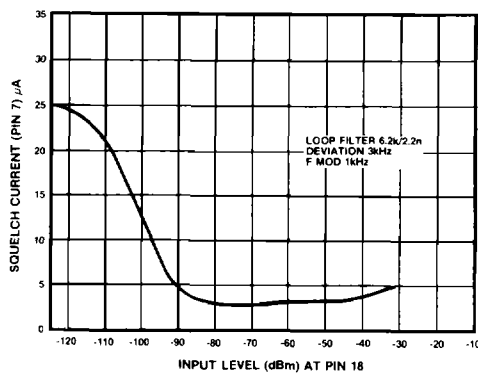


Fig. 10 Typical squelch current v. input level

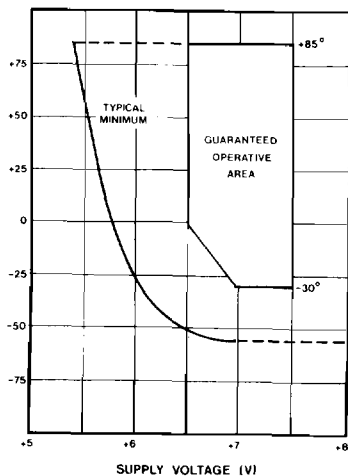


Fig. 8 Supply voltage v. temperature

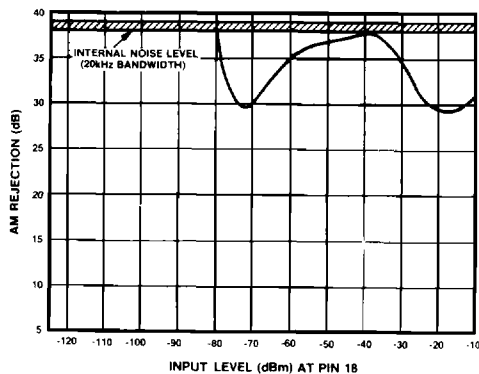


Fig. 11 Typical AM rejection

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

ELECTRICAL CHARACTERISTICS**Test conditions (unless otherwise stated):**Supply voltage V_{cc} : 7VInput signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ± 2.5 kHz frequency deviationAmbient temperature: -30°C to $+85^{\circ}\text{C}$; IF = 100kHz; AF bandwidth = 15kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200 Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		$\mu\text{V rms}$	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100 $\mu\text{V rms}$ input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20 $\mu\text{V rms}$ input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3 μV input at pin 18
Noise figure		6		dB	50 Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		$\mu\text{V rms}$	Pin 18 to pin 4, 1dB compression
Squelch output load	250			k Ω	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input
Grade 2	95		110	kHz	
Grade 3	105		120	kHz	
Source impedance (pin 4)		25	40	k Ω	
AF output impedance		4	10	k Ω	
Lock-in dynamic range	± 8			kHz	20 μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES**IF Amplifiers and Mixer**

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01 μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an

external capacitor equal to $(40 \pm 7)/f$ pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and V_{cc} .

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601C' and a '1', '2', '3' to indicate the selection.

Frequency tolerances are:

- /1 85 - 100kHz (or uncoded)
- /2 95 - 110kHz
- /3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 5-18dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig 4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choice of f_n , the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio f_m/f_n highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_e f_n}{\Delta f}$$

can be established for the desired damping factor.

Φ_e - peak phase error

f_n - loop natural frequency

Δf - maximum deviation of the input signal

and as f_n and Δf are known, Φ_e is easily calculated. Values for Φ_e should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at $\pm\pi/2$ radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of Φ_e achieved is far removed from this value, a new value of f_n should be chosen and the process repeated.

With f_n and D established, the time constants are derived from

$$t_1 + t_2 = \frac{K_0 K_D}{(2\pi f_n)^2}$$

$$\text{and } t_2 = \frac{D}{\pi f_n} - \frac{1}{K_0 K_D}$$

$K_0 K_D$ is $0.3f_0$, where f_0 is the operating frequency of the VCO. t_1 is fixed by the capacitor and an internal 20kΩ resistor; t_2 is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{\text{ext}} = \frac{t_2 \times 20 \times 10^3}{t_1}$$

In order that standard values may be used, it is better to establish a value of C and use the next lowest standard value e.g. $C_{\text{calc}} = 238\text{pF}$, use 220pF , as it is better to widen the loop bandwidth rather than narrow it.

The value of R_{ext} is then 'rounded up' by a similar process. It is, however, better to increase R_{ext} to the nearest preferred value as loop bandwidth is proportional $(R_{\text{ext}})^{-1/2}$ while damping factor is proportional to R: thus damping factor is increasing more quickly which gives a more level response.

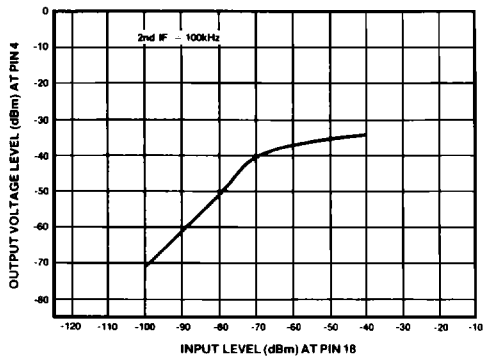


Fig.12 Typical conversion gain (to pin 4)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55° C to +125° C (DP package)
	-55° C to +150° C (DG)
Operating temperature	-55° C to +125° C
(see Electrical Characteristics)	
Input voltage	1V RMS at pin 18