SLG59M1709V

An Ultra-small, 4 mΩ / 4 A Integrated Power Switch with Multiple Protection Features

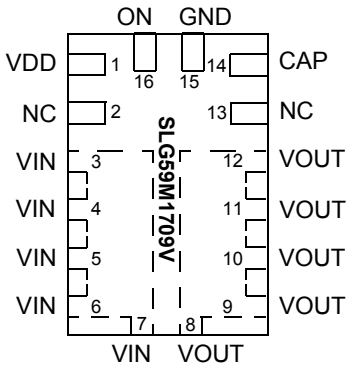
General Description

Operating from a 2.5 V to 5.5 V power supply and fully specified over the -40 °C to 85 °C temperature range, the SLG59M1709V is a high-performance 4 mΩ, 4 A single-channel nFET integrated power switch with programmable inrush current control. Inrush current control is achieved by programming the VOUT slew rate with an external capacitor. Using a proprietary MOSFET design, the SLG59M1709V achieves a stable 4 mΩ RDSON across a wide input/supply voltage range and over temperature. Incorporating two-stage current protection as well as thermal protection, the SLG59M1709V is designed for all 0.8 V to 5.5 V power rail applications. Using Silego's proprietary CuFET™ technology for high-current operation, the SLG59M1709V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.6 mm x 2.5 mm STQFN package

Features

- Low Typical RDSON nFET: 4 mΩ
- Maximum Continuous Switch Current: Up to 4 A
- Supply Voltage: 2.5 V ≤ VDD ≤ 5.5 V
- Wide Input Voltage Range: 0.8 V ≤ VIN ≤ VDD
- Capacitor-programmable Start-up and Inrush Current Control
- Two-stage Overcurrent Protection:
  - Fixed threshold, 8 A Active Current Limit
  - Fixed 0.5 A Short-circuit Current Limit
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 16-pin 1.6 mm x 2.5 mm STQFN Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

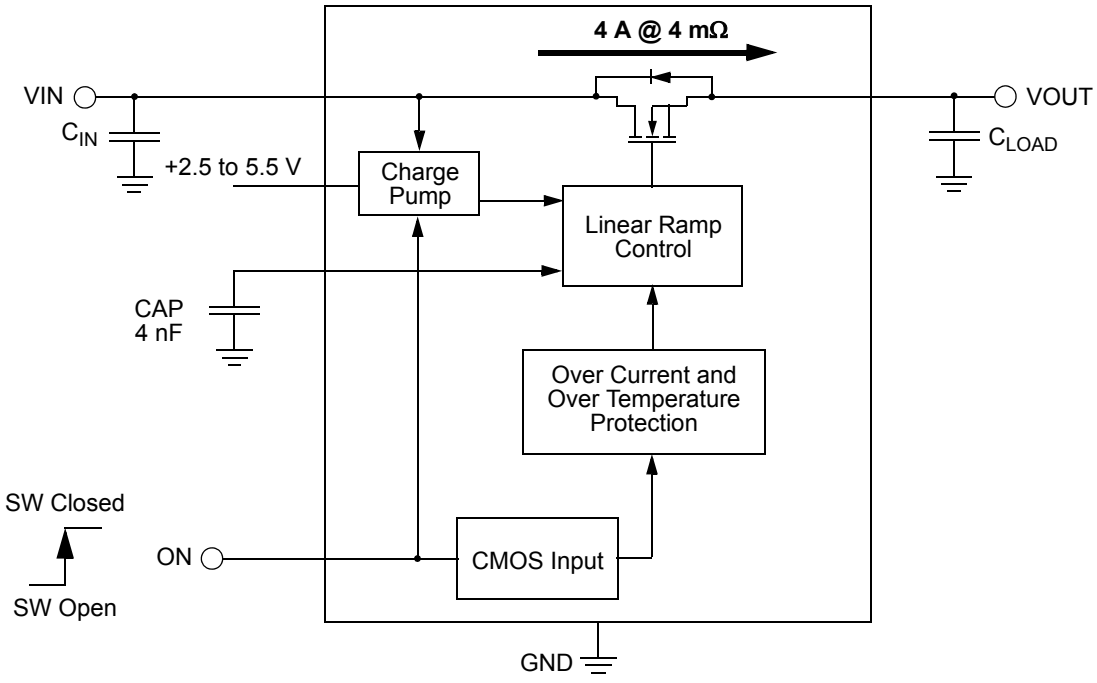


16-pin FC-STQFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Preliminary

Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	With an internal 1.9 V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry where its range is 2.5 V ≤ VDD ≤ 5.5 V. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor
2	NC	NC	No Connect
3-7	VIN	MOSFET	Drain terminal of Power MOSFET (Pins 3-7 fused together). Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at VIN should be rated at 10 V or higher.
8-12	VOUT	MOSFET	Source terminal of Power MOSFET (Pins 8-12 fused together) Connect a low ESR capacitor (up to 500 µF) from this pin to GND. Capacitors used at VOUT should be rated at 10 V or higher.
13	NC	NC	No Connect
14	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the VOUT slew rate and overall turn-on time of the SLG59M1709V. For best performance, the range for CAP values are 2 nF ≤ CAP ≤ 22 nF. Capacitors used at the CAP pin should be rated at 10 V or higher.
15	GND	GND	Ground
16	ON	Input	A low-to-high transition on this pin closes the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with VIL < 0.3 V and VIH > 0.85 V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. While there is an internal pull down circuit to ground (~4 MΩ), do not allow this pin to be open-circuited.

Ordering Information

Part Number	Type	Production Flow
SLG59M1709V	STQFN 16L	Industrial, -40 °C to 85 °C
SLG59M1709VTR	STQFN 16L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Pin to GND		--	--	6	V
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	6	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON, CAP to GND	ON and CAP Pin Voltages to GND		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.6 x 2.5 mm 16L STQFN; Determined using 1 in^2, 1.2 oz. copper pads under each VIN and VOUT on FR4 pcb material	--	35	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1.2	W
IDS_{MAX}	Max Continuous Switch Current		--	--	4	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.5	--	5.5	V
VDD_{UVLO}	VDD Undervoltage Lockout Threshold	VDD ↑	--	1.9	--	V
I_{DD}	Power Supply Current when OFF	V_{DD} = V_{IN} = 5.5 V; ON = 0	--	1	2	µA
	Power Supply Current, ON (Steady State)	V_{DD} = V_{IN} = ON = 5.5 V; No Load	--	120	170	µA
RDS_{ON}	ON Resistance	V_{DD} = V_{IN} = 5 V; T_A 25°C MOSFET @100 mA	--	4	5.5	mΩ
		V_{DD} = V_{IN} = 5 V; T_A 85°C MOSFET @100 mA		5	6.8	mΩ
I_{FET_OFF}	MOSFET OFF Leakage Current	V_{DD} = V_{IN} = 5.5 V; V_{OUT} = 0 V; ON = 0	--	--	2	µA
V_{IN}	Drain Voltage		0.8	--	V_{DD}	V
I_{LIMIT}	Active Current Limit, I_{ACL}	V_{OUT} > 0.3 V	6	8	10	A
	Short-circuit Current Limit, I_{SCL}	V_{OUT} < 0.3 V	--	0.5	--	A
T_{ON_Delay}	ON pin Delay Time	50% ON to V_{OUT} Ramp Start V_{DD} = V_{IN} = 5V; CAP = 4nF; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	--	200	--	µs

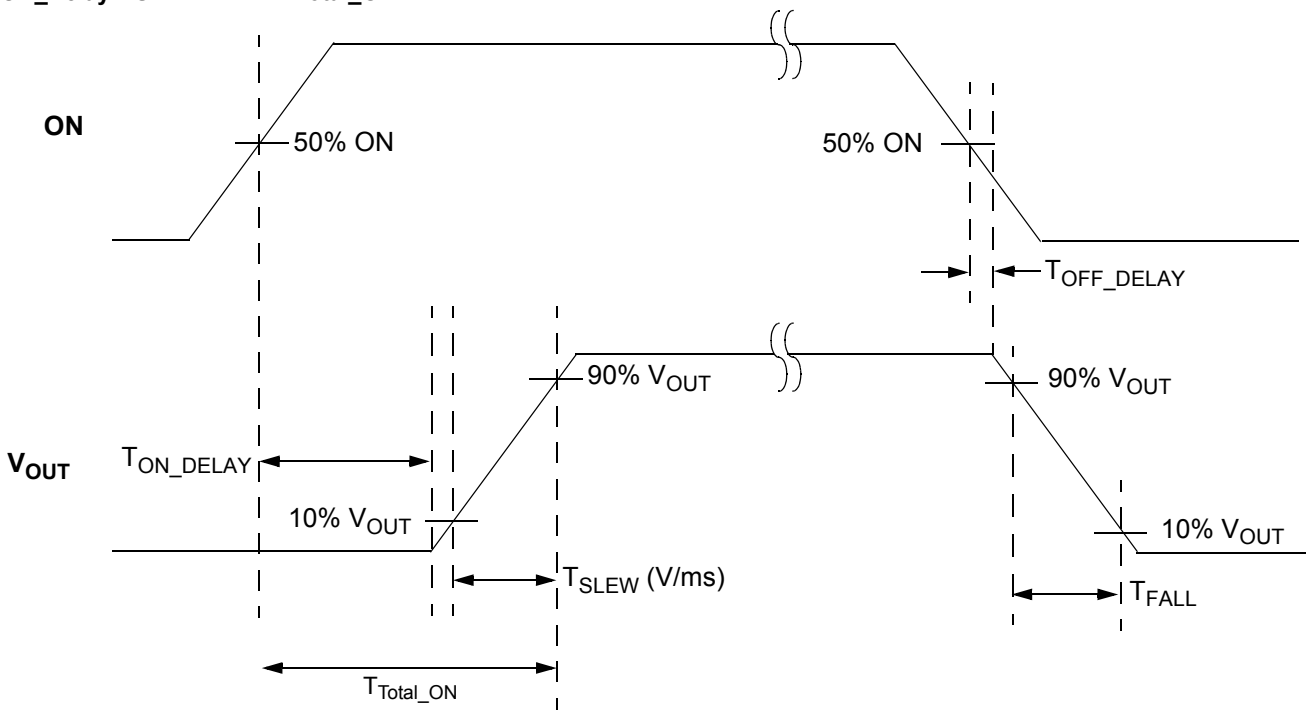
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$T_{SLEWRATE}$	V_{OUT} Slew Rate	10% V_{OUT} to 90% V_{OUT} ↑	Set by External CAP[1]			V/ms
		Example: CAP = 4 nF; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	2.5	2.9	3.5	V/ms
T_{Total_ON}	Total Turn-on Time	50% ON to 90% V_{OUT} ↑	Set by External CAP[1]			ms
		Example: CAP = 4 nF; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	1.4	1.7	2	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, no C_{LOAD}	--	8	15	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	--	--	500	µF
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
$I_{ON(LKG)}$	ON Pin Leakage Current	ON = ON_V_{IH} or ON = GND	--	1.5	--	µA
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C

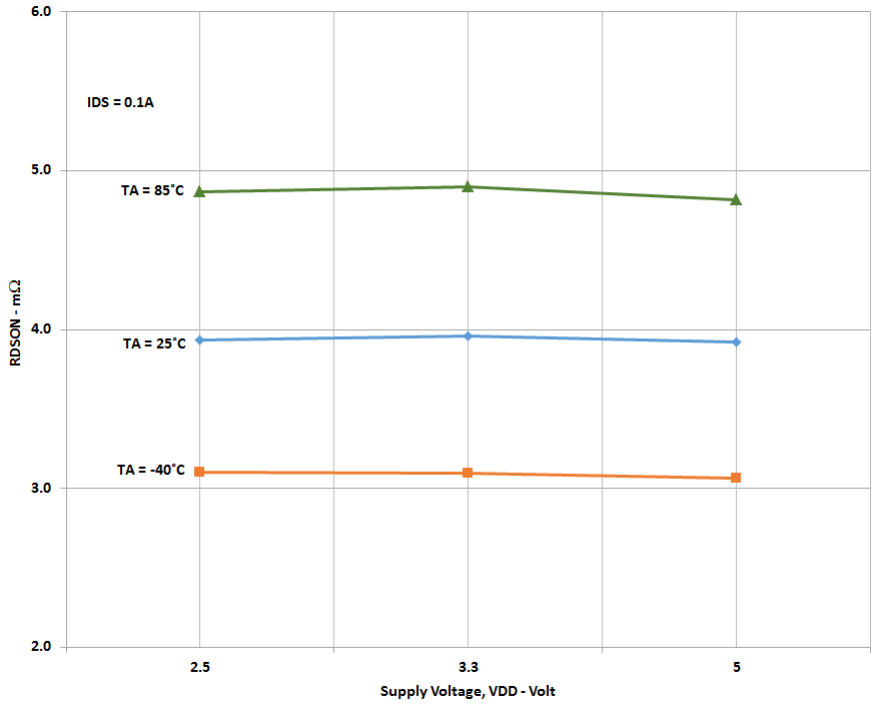
Notes:
1. Refer to typical Timing Parameter vs. CAP performance charts for additional information when available.

T_{ON_Delay}, T_{SLEW}, and T_{Total_ON} Timing Details

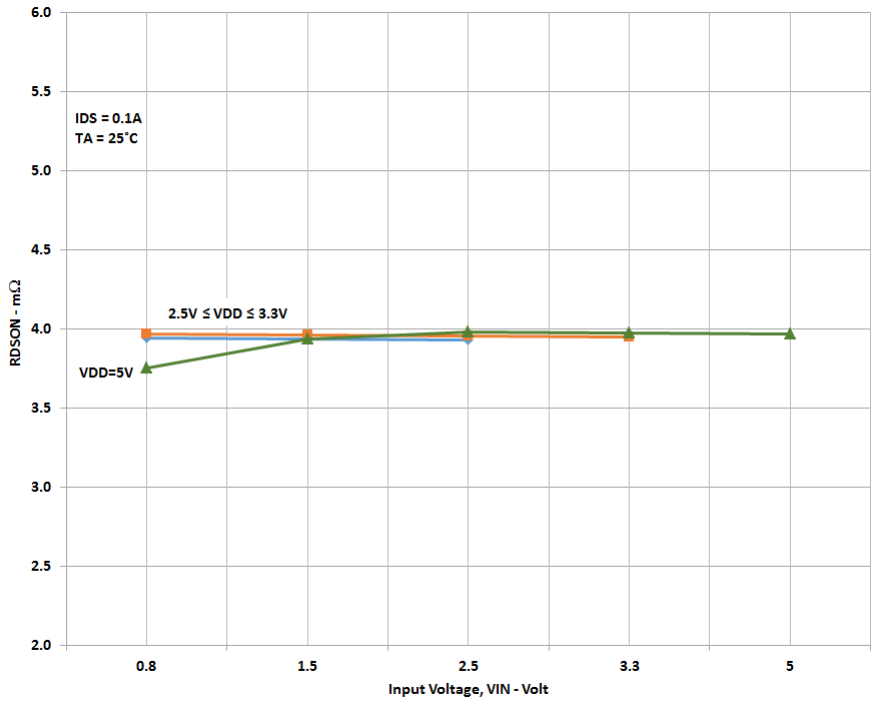


Typical Performance Characteristics

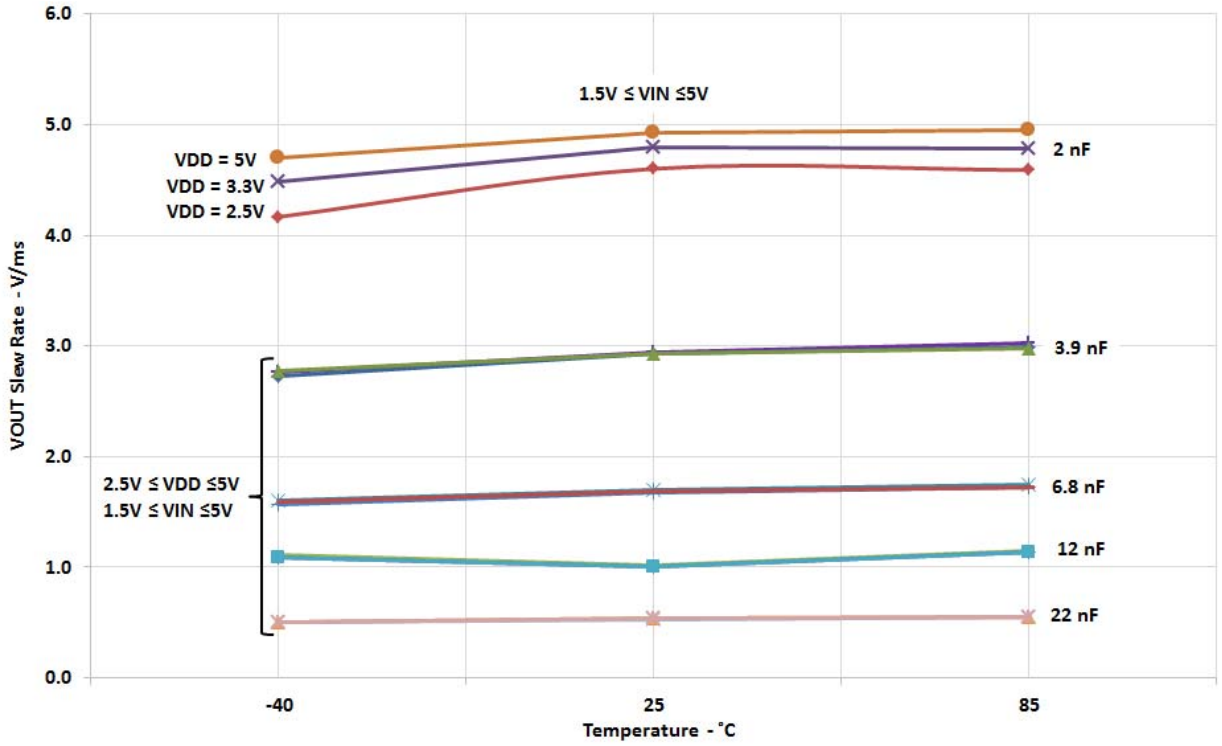
RDS_{ON} vs. V_{DD} and Temperature



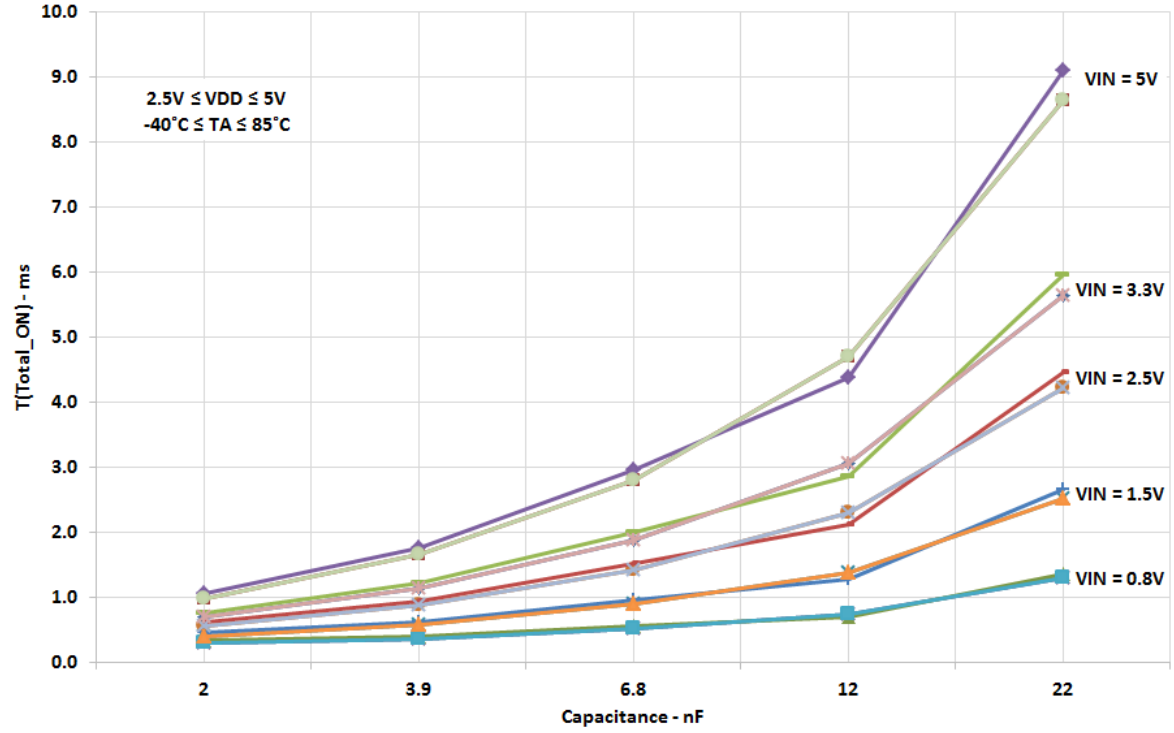
RDS_{ON} vs. V_{IN} and V_{DD}



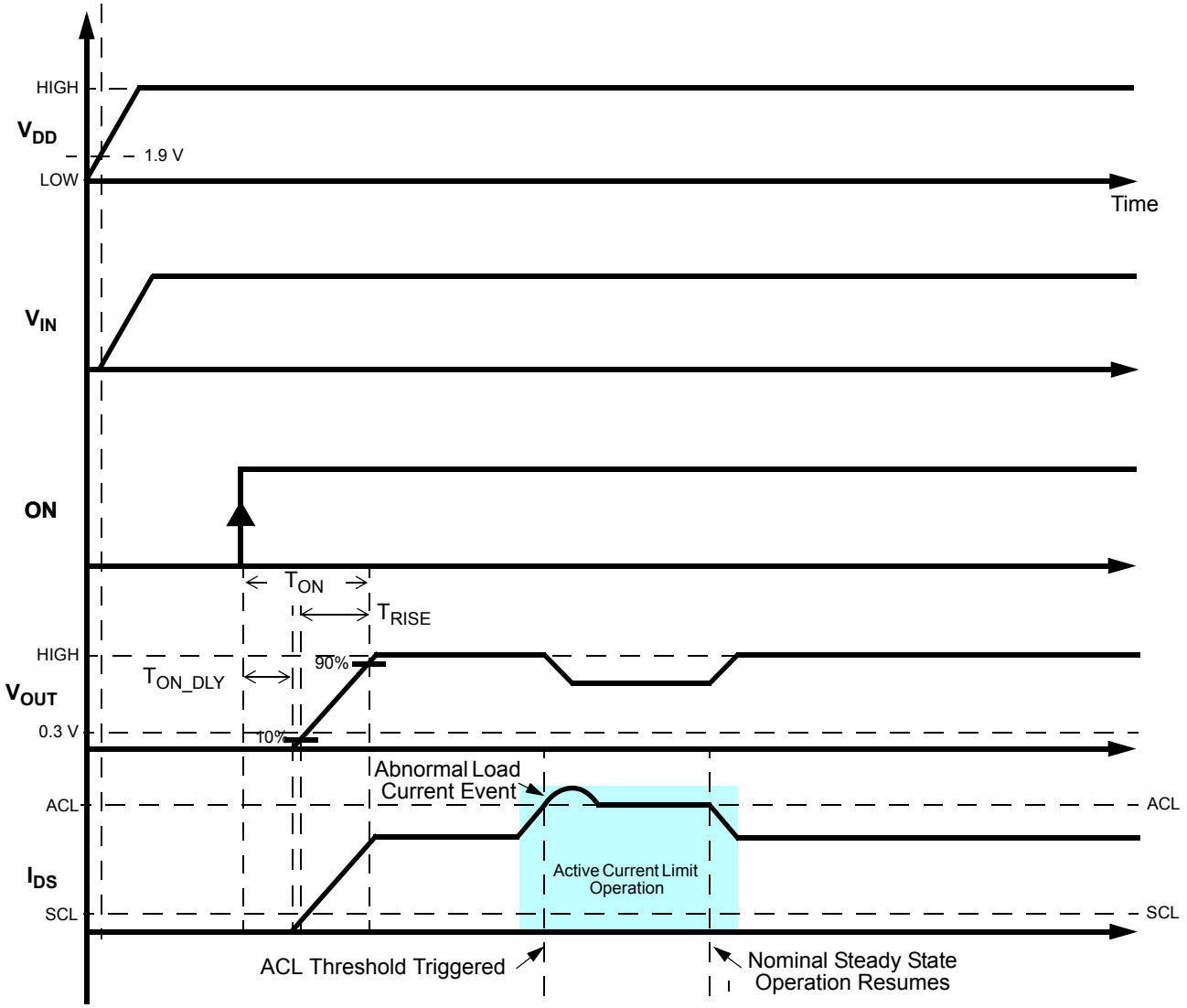
VOUT Slew Rate vs. Temperature, V_{DD}, V_{IN}, and CAP



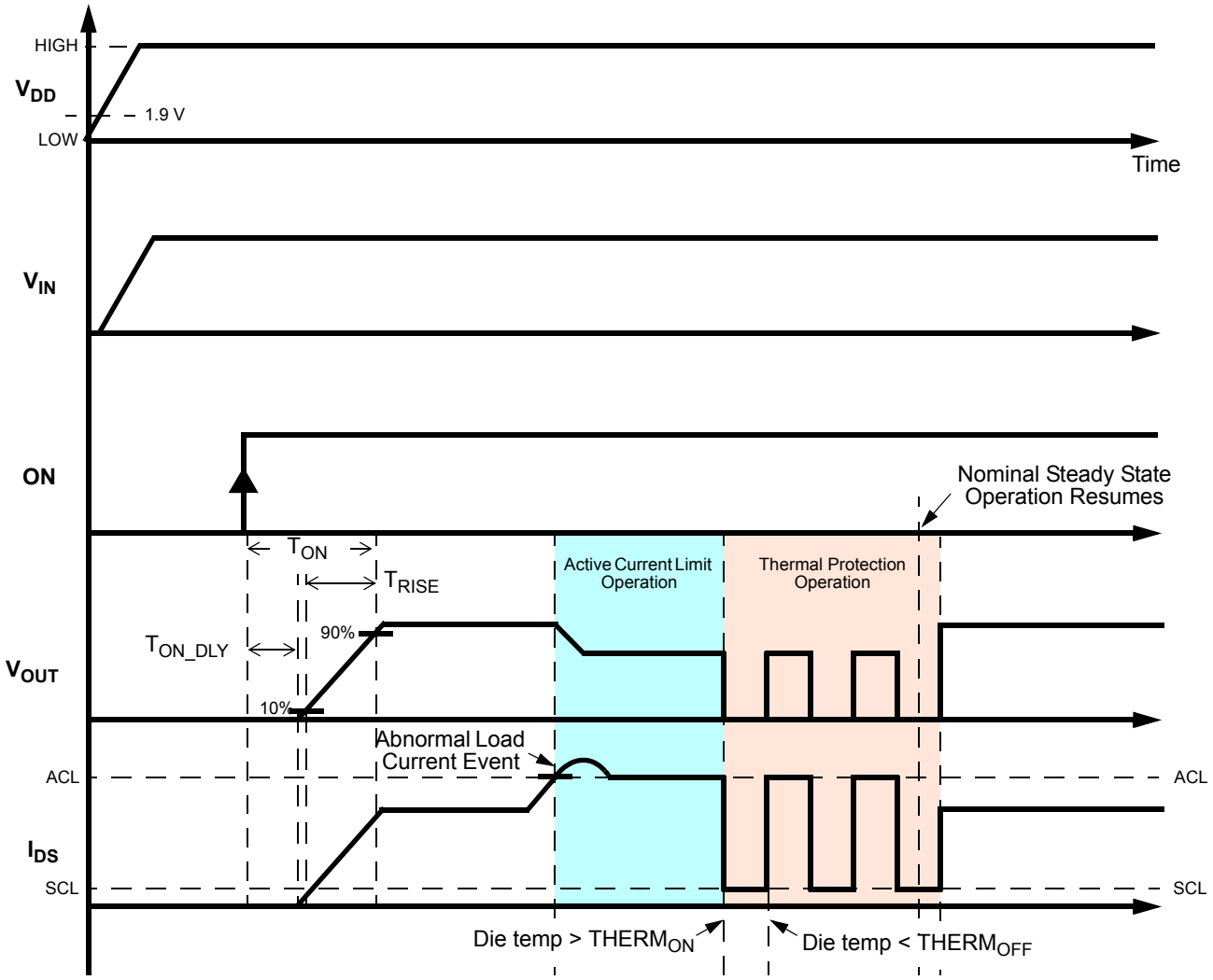
T_{TOTAL_ON} vs. CAP, V_{IN}, V_{DD}, and Temperature



Timing Diagram - Basic Operation including Active Current Limit Protection



Timing Diagram - Active Current Limit & Thermal Protection Operation



SLG59M1709V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{DD} first, followed by V_{IN} only after V_{DD} is > 1.9 V, and finally toggling the ON pin LOW-to-HIGH after V_{IN} is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order. It is important that the SLG59M1709V's ON pin is toggled HIGH only after V_{DD} and V_{IN} have reached their steady-state values; otherwise, the power switch will spend an undesirable amount of time in high-resistance mode while powering up, heating up, and possibly reaching its thermal shutdown before ever fully turning on.

If V_{DD} and V_{IN} are applied at the same time, a voltage glitch may appear on the output pin at V_{OUT}. To prevent glitches at the output, it is recommended to connect a 10 µF capacitor from the V_{OUT} pin to GND and to keep the V_{DD} & V_{IN} ramp times less than 2 ms.

The V_{OUT} output follows a linear ramp when the power switch is turned on, provided that the V_{OUT} slew time set by CAP is less than the RC time constant formed by the RDS_{ON} of the power switch and load capacitance C_{LOAD}.

SLG59M1709V Current Limiting Operation

The SLG59M1709V has two types of current limiting triggered by the output V_{OUT} pin voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} pin voltage > 250 mV, the output current is initially limited to the Active Current Limit (ACL) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's ACL threshold. During active current-limit operation, V_{OUT} is also reduced by I_{ACL} x $RDSON_{ACL}$. This observed behavior is illustrated in the timing diagrams on Pages 7 and 8.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} pin voltage < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the SCL threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the SCL threshold is much lower than the ACL threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

SLG59M1709V Start-up Inrush Current Considerations with Capacitive Loads

In distributed power applications, the SLG59M1709V is generally implemented on the outboard or downstream side of switching regulator dc/dc converters with internal overcurrent protection. As an adjustable output voltage slew-rate, integrated power switch, it is important to understand the start-up operation of the SLG59M1709V with capacitive loads. An equivalent circuit of the SLG59M1709V's slew-rate control loop with capacitors at its V_{IN} and V_{OUT} terminals is shown in Figure 1:

SLG59M1709V Start-up Inrush Current Considerations with Capacitive Loads (continued)

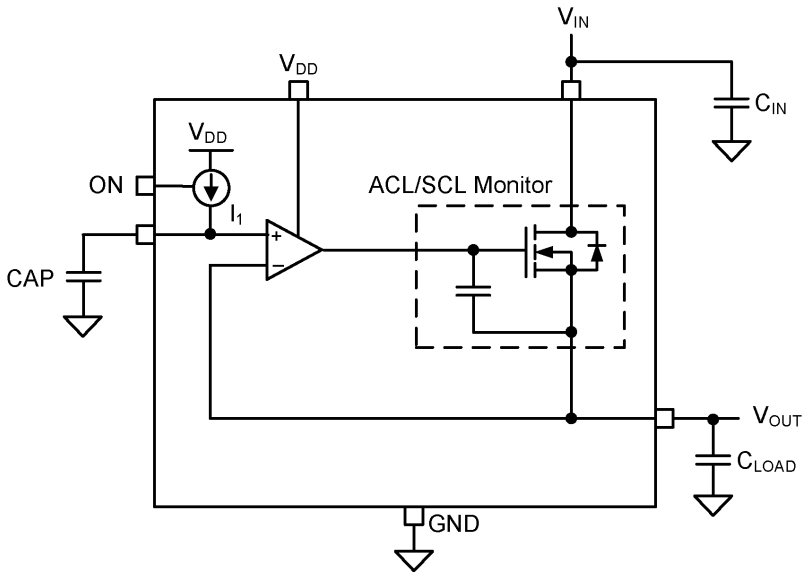


Figure 1. SLG59M1709V's Equivalent Slew-rate Control Loop Circuit.

For a desired V_{OUT} slew-rate ($V_{OUT(SR)}$), a corresponding CAP value is selected. At the V_{OUT} terminal and with ON = LOW, the internal FET is OFF, V_{OUT} is initially at 0V, and there is no stored charge on C_{LOAD}. When a low-to-high transition is applied to the IC's ON pin, an internal current source (I_1) is enabled which, in turn, charges the external slew-rate capacitor, CAP. The SLG59M1709V's internal micropower op amp sets the circuit's $V_{OUT(SR)}$ based on the slew rate of the nodal voltage at its non-inverting terminal (the voltage at the CAP terminal).

As a function of $V_{OUT(SR)}$ and C_{LOAD}, a 1st-order expression for the circuit's FET current (and inrush current) when a low-to-high transition on the ON pin is applied becomes:

$$\text{Start-up Current } I_{DS} \text{ or } I_{INRUSH} = V_{OUT(SR)} \times C_{LOAD}$$

From the expression above and for a given $V_{OUT(SR)}$, C_{LOAD} determines the magnitude of the inrush current; that is, for large values of C_{LOAD}, large inrush currents can result. If the inrush currents are large enough to trigger the overcurrent protection of an upstream dc/dc converter, the system can be shut down.

In applications where the desired $V_{OUT(SR)}$ is fast and C_{LOAD} is very large (>200µF), there is a secondary effect on the observed $V_{OUT(SR)}$ attributed to the SLG59M1709V's internal short-circuit current limit monitor (its SCL monitor). If the resultant inrush current is larger than the IC's SCL threshold, the SCL current monitor limits the inrush current and the current to charge C_{LOAD} until the SCL OFF threshold is crossed (~0.3V). During the time the SCL monitor's been activated, the inrush current profile may exhibit an observable reduction in $V_{OUT(SR)}$ as shown in Figure 2 where CAP was set to 4nF and 470µF was chosen for C_{LOAD}.

SLG59M1709V Start-up Inrush Current Considerations with Capacitive Loads (continued)

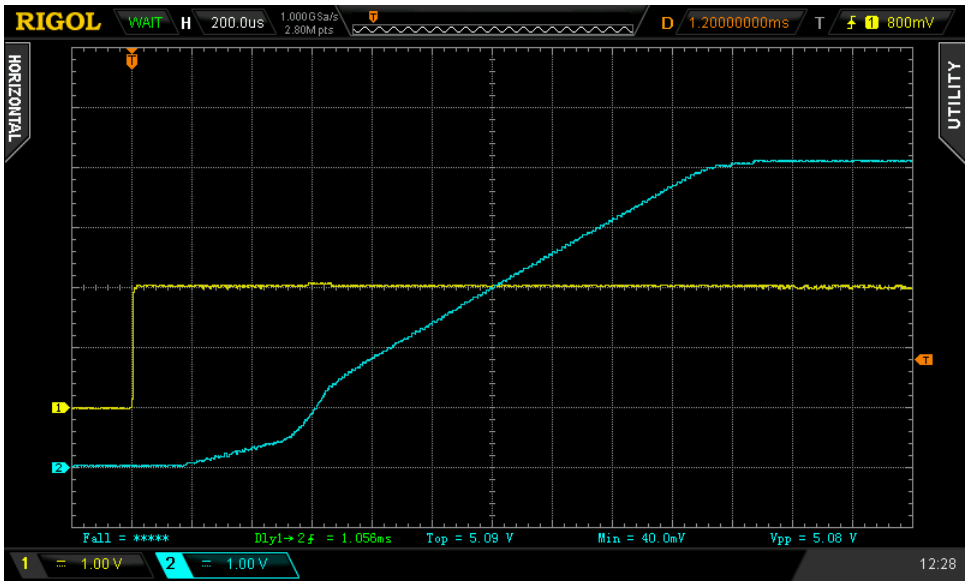


Figure 2. A SLG59M1709V with CAP set to 4nF and 470µF for C_{LOAD}. C_{LOAD}-to-CAP ratio is greater than 33,600. Note that the internal SCL monitor's been triggered and $V_{OUT(SR)}$ is reduced until V_{OUT} reaches ~0.3V.

A closer analysis of the IC's internal slew-control large-scale yields the following:

$$\frac{SCL}{C_{LOAD}} = M_{SR} \times \frac{I_1}{CAP}$$

where

SCL = IC's short-circuit current limit threshold, typically 0.5A;
M_{SR} = An internal slew-rate multiplier from the IC's CAP terminal to the V_{OUT} terminal;
I_1 = An internal current source to charge the external CAP.

Rearranging the equation to isolate both C_{LOAD} and CAP yields the following:

$$\frac{C_{LOAD}}{CAP} = \frac{SCL}{I_1 \times M_{SR}}$$

For the SLG59M1709V device, the right-hand side of the expression is approximately 33,600 after taking into account part-to-part variations because of process, voltage, and temperature.

Referring to the configuration of Figure 2's scope capture, the C_{LOAD}-to-CAP ratio is 117,500 (470µF/4nF) where it is evident that the SCL monitor circuit is charging C_{LOAD} shortly after a low-to-high ON transition. If it is desired to avoid a reduction in $V_{OUT(SR)}$, the choices are decreasing C_{LOAD} and/or increasing CAP so that the ratio is always less than 33,600 including taking into account external capacitor tolerances for initial accuracy and temperature.

As shown in Figure 3, it was chosen to reduce $V_{OUT(SR)}$ by increasing CAP to 15nF while keeping C_{LOAD} at 470µF. With this configuration, the ratio of C_{LOAD} to CAP is about 31,333 (smaller than 33,600). Upon a low-to-high transition on the ON pin, the V_{OUT} increases smoothly with no evidence of SCL monitor's interaction.

SLG59M1709V Start-up Inrush Current Considerations with Capacitive Loads (continued)

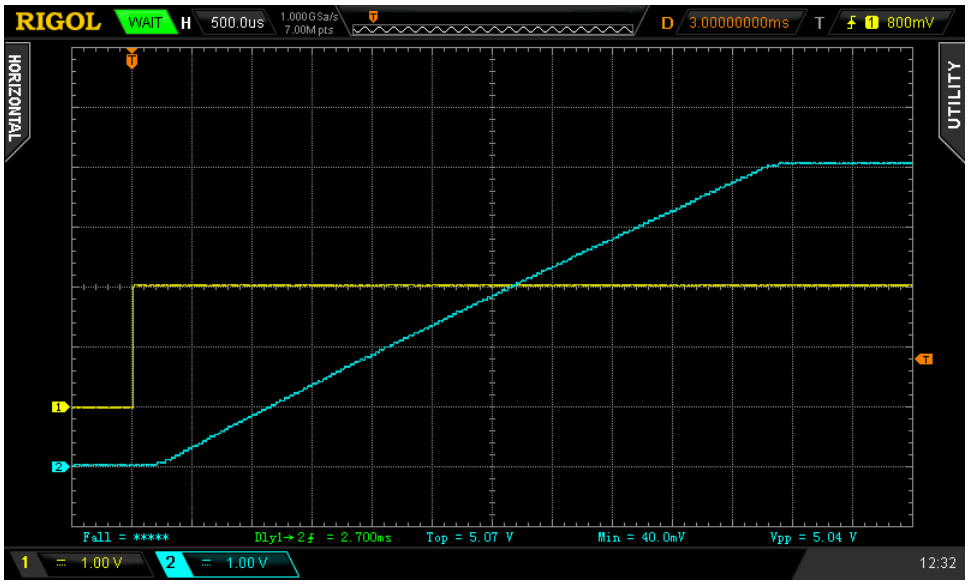


Figure 3. A SLG59M1709V with CAP set to 15nF and 470µF retained for C_{LOAD}. C_{LOAD}-to-CAP ratio is smaller than 33,600. Note smooth V_{OUT} transition.

Power Dissipation

The junction temperature of the SLG59M1709V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1709V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{OUT}^2$$

where:

PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{OUT} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:
T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

During active current-limit operation, the SLG59M1709V's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN}-V_{OUT}) and the magnitude of the output current in active current-limit operation (I_{ACL}):

$$PD = (V_{IN}-V_{OUT}) \times I_{ACL} \text{ or}$$

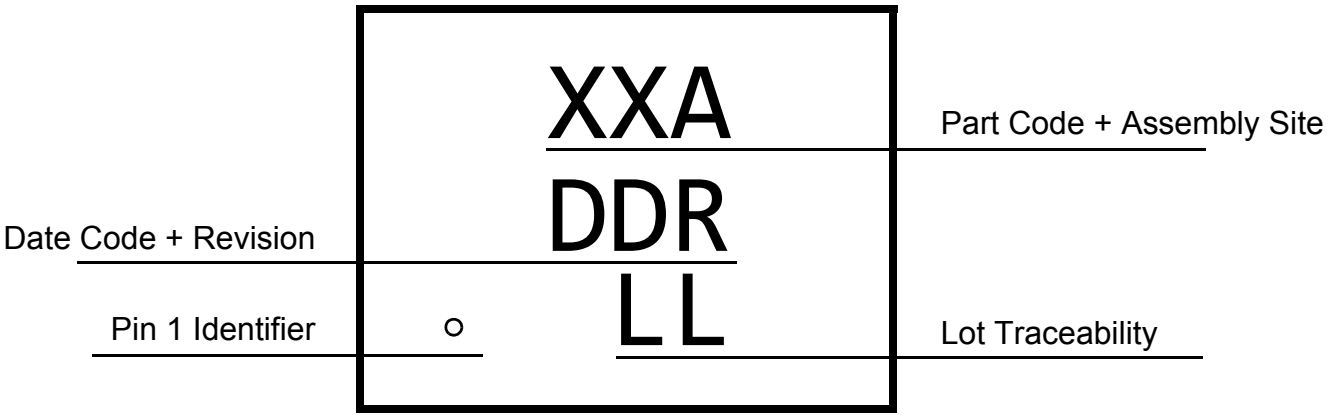
$$PD = (V_{IN} – (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$

For more information on Silego GreenFET3 integrated power switch features, please visit our Application Notes page at our website and see App Note "AN-1068 GreenFET3 Integrated Power Switch Basics".

Package Top Marking System Definition

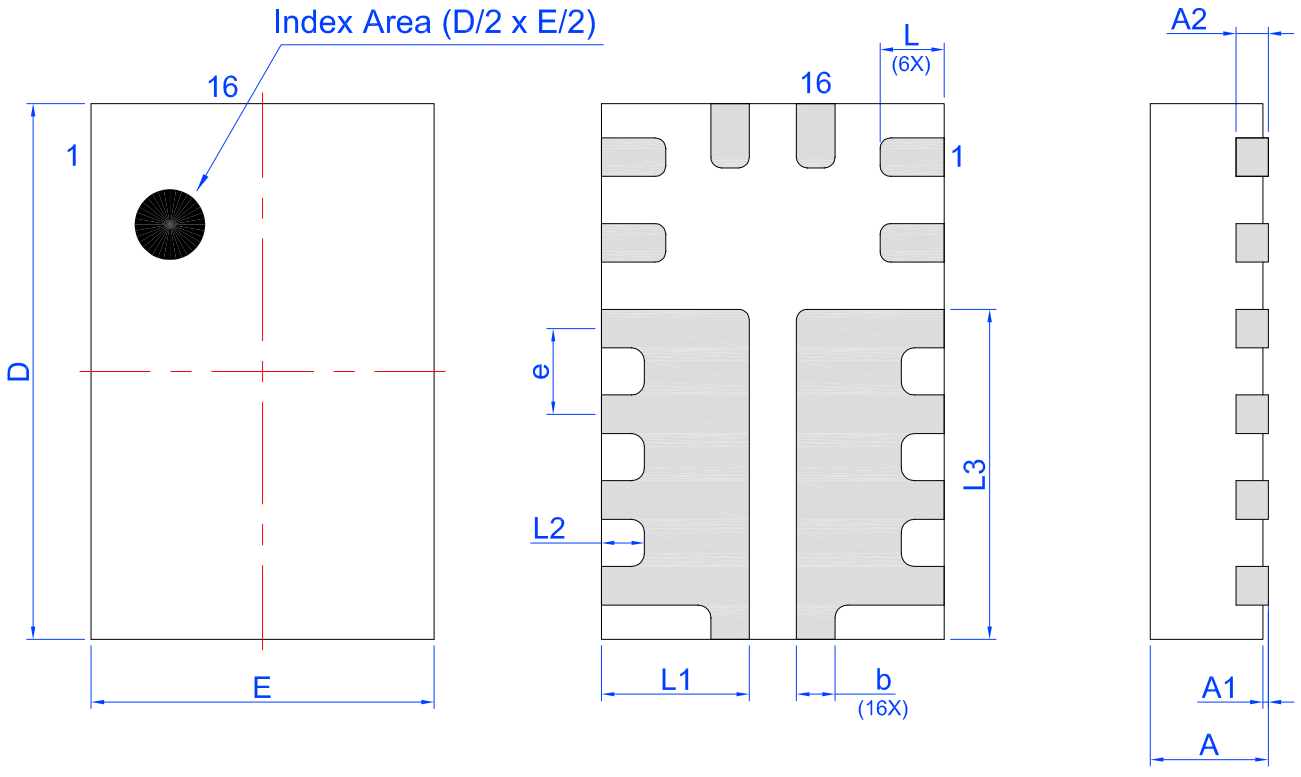


XX - Part Code Field[1]
A - Assembly Site Code Field[2]
DD - Date Code Field[1]
R - Part Revision Code Field[2]
LL - Lot Traceability Field[1]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

16 Lead STQFN Package 1.6 mm x 2.5 mm (Fused Lead)

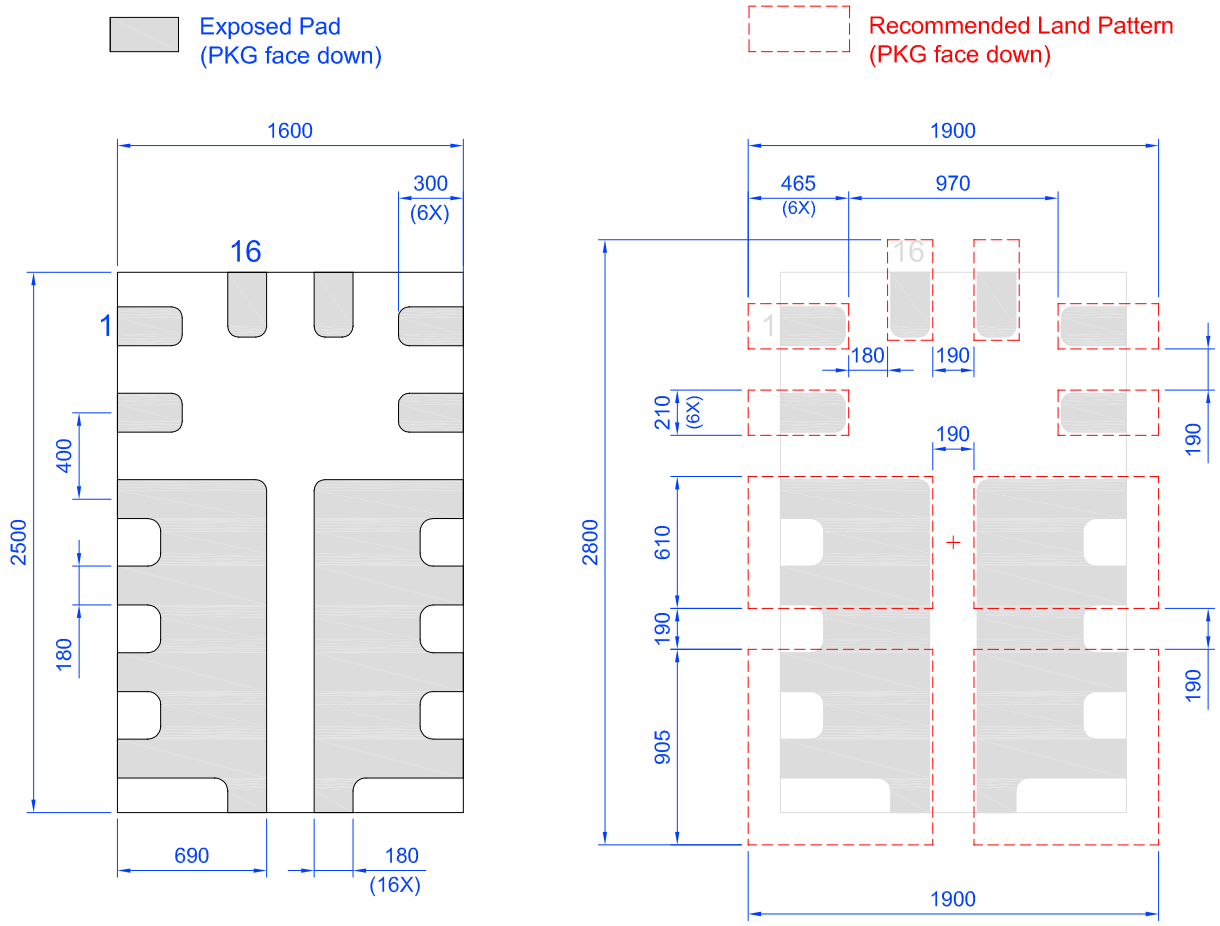


Top View BTM View Side View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
				L3	1.49	1.54	1.59

SLG59M1709V 16-pin STQFN PCB Landing Pattern



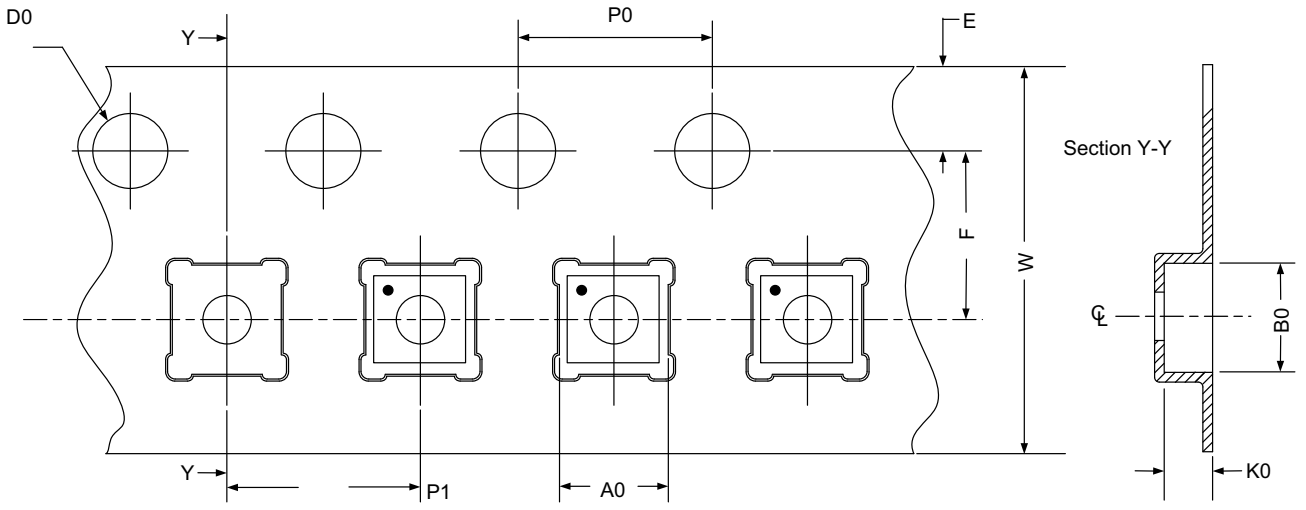
Unit: um

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 1.6x2.5mm 0.4P FCA Green	16	1.6x2.5x 0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 1.6x2.5mm 0.4P FCA Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
6/20/2016	0.56	Added section regarding Start up Considerations
6/3/2016	0.55	Updated naming convention for Cload Updated EC table Updated Power Up and Current Limiting descriptions
5/3/2016	0.54	Updated Pin Configuration Diagram
4/25/2016	0.53	Updated Toff_delay
4/22/2016	0.52	Updated Performance Charts Updated Iacl and Toff_delay
4/18/2016	0.51	Added Performance Charts
3/21/2016	0.50	Preliminary Release

Mouser Electronics

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SLG59M1709V