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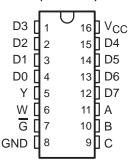
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Jameco Part Number 835358

SCLS110E - DECEMBER 1982 - REVISED SEPTEMBER 2003

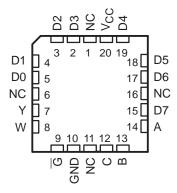
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 13 ns
- ±6-mA Output Drive at 5 V

SN54HC151 . . . J OR W PACKAGE SN74HC151 . . . D, N, NS, OR PW PACKAGE (TOP VIEW)



- Low Input Current of 1 μA Max
- 8-Line to 1-Line Multiplexers Can Perform as:
 - Boolean-Function Generators
 - Parallel-to-Serial Converters
 - Data Source Selectors

SN54HC151 ... FK PACKAGE (TOP VIEW)



NC - No internal connection

description/ordering information

These data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe (\overline{G}) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N	Tube of 25	SN74HC151N	SN74HC151N	
		Tube of 40	SN74HC151D		
	SOIC - D	Reel of 2500	SN74HC151DR	HC151	
4000 / 0500		Reel of 250	SN74HC151DT		
-40°C to 85°C	SOP - NS	Reel of 2000	SN74HC151NSR	HC151	
		Tube of 90	SN74HC151PW		
	TSSOP - PW	Reel of 2000	SN74HC151PWR	HC151	
		Reel of 250	SN74HC151PWT		
	CDIP – J	Tube of 25	SNJ54HC151J	SNJ54HC151J	
−55°C to 125°C	CFP – W	Tube of 150	SNJ54HC151W	SNJ54HC151W	
	LCCC – FK	Tube of 55	SNJ54HC151FK	SNJ54HC151FK	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



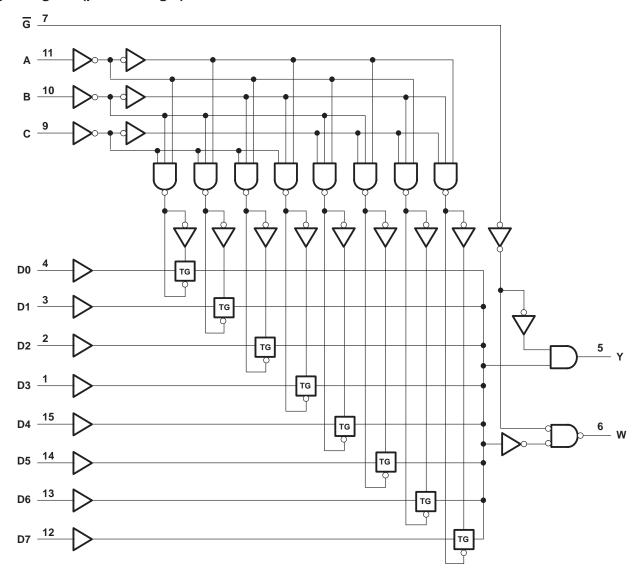
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FUNCTION TABLE

	II	OUTI	PUTS		
	SELECT	-	STROBE		W
С	В	Α	G	T	VV
Х	Χ	Χ	Н	L	Н
L	L	L	L	D0	D0
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	L	D3	D3
Н	L	L	L	D4	D4
Н	L	Н	L	D5	D5
Н	Н	L	L	D6	D6
Н	Н	Н	L	D7	D7

D0, D1 . . . D7 = the level of the respective D input

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (se	ee Note 1)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCO	c) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	- 	±35 mA
Continuous current through V _{CC} or GND		±70 mA
Package thermal impedance, θ _{JA} (see Note 2):	: D package	73°C/W
	N package	67°C/W
	NS package	64°C/W
	PW package	108°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			SI	SN54HC151		SN	174HC15	i1	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
ViH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V _{CC} = 2 V			0.5			0.5	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V			1000			1000	
Δt/Δν	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns
		V _{CC} = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	PARAMETER TEST CONDITIONS		.,	T _A = 25°C			SN54H	IC151	SN74HC151			
PARAMETER			vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			2 V	1.9	1.998		1.9		1.9			
		$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4			
Voн	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V	
		$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84			
		$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34			
			2 V		0.002	0.1		0.1		0.1		
			I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
VoL	VI = VIH or VIL		6 V		0.001	0.1		0.1		0.1	V	
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33		
		$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33		
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA	
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ	
Ci		_	2 V to 6 V		3	10	·	10		10	pF	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то		T _A = 25°C			SN54HC151		SN74HC151		
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		94	250		360		312	
	A, B, or C	Y or W	4.5 V		30	50		73		63	
			6 V		25	43		62		54	
			2 V		74	195		283		244	
^t pd	Any D	Y or W	4.5 V		23	39		57	49 ns	ns	
·			6 V		20	33		48		41	ns
			2 V		49	127		185		159	
	G	Y or W	4.5 V		15	25		37		32	
			6 V		13	22		32		28	
			2 V		22	75		110	·	95	
t _t		Y or W	4.5 V		9	15		22	·	19	ns
			6 V		8	13		19		16	

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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

242445	METER FROM TO (OUTPUT) VCC		.,	T	λ = 25°C	;	SN54H	IC151	SN74H	IC151	
PARAMETER			vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		107	350		525		440	
	A, B, or C	Y or W	4.5 V		33	70		105		88	
			6 V		30	59		89		76	
	Any D	Y or W	2 V		90	275		415		345	ns
^t pd			4.5 V		29	51		83		69	
			6 V		25	47		72		59	
			2 V		67	205		310		255	
	G	Y or W	4.5 V		21	41		62		51	
			6 V		18	35		53		43	
		Y or W	2 V		51	210		315		265	
t _t			4.5 V		16	42		63		53	ns
				6 V		14	36		53		45

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	70	pF

PARAMETER MEASUREMENT INFORMATION From Output VCC Test Input 50% 50% **Under Test Point** CL tPLH → (see Note A) VOH In-Phase 90% 50% Output **LOAD CIRCUIT** VoL **⋖**─ tpHL - VCC Input 90% **Out-of-Phase** 50% 10% Output v_{OL} **VOLTAGE WAVEFORM VOLTAGE WAVEFORMS** PROPAGATION DELAY AND OUTPUT TRANSITION TIMES **INPUT RISE AND FALL TIMES**

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 6$ ns, $t_f = 6$ ns.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms







12-Sep-2006

PACKAGING INFORMATION

SN74HC151DE4	Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54HC151J ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type	84128012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SN74HC151D	8412801EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74HC151DE4 ACTIVE SOIC D 16 40 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/Br)	SN54HC151J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74HC151DG4	SN74HC151D	ACTIVE	SOIC	D	16	40		CU NIPDAU	Level-1-260C-UNLIM
No Sb/Br SN74HC151DR	SN74HC151DE4	ACTIVE	SOIC	D	16	40		CU NIPDAU	Level-1-260C-UNLIM
SN74HC151DRE4 ACTIVE SOIC D 16 2500 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/Br)	SN74HC151DG4	ACTIVE	SOIC	D	16	40	,	CU NIPDAU	Level-1-260C-UNLIM
SN74HC151DRG4	SN74HC151DR	ACTIVE	SOIC	D	16	2500	,	CU NIPDAU	Level-1-260C-UNLIM
SN74HC151DT	SN74HC151DRE4	ACTIVE	SOIC	D	16	2500	,	CU NIPDAU	Level-1-260C-UNLIM
SN74HC151DTE4	SN74HC151DRG4	ACTIVE	SOIC	D	16	2500		CU NIPDAU	Level-1-260C-UNLIM
SN74HC151N	SN74HC151DT	ACTIVE	SOIC	D	16	250		CU NIPDAU	Level-1-260C-UNLIM
SN74HC151NE4	SN74HC151DTE4	ACTIVE	SOIC	D	16	250	,	CU NIPDAU	Level-1-260C-UNLIM
SN74HC151NSR	SN74HC151N	ACTIVE	PDIP	N	16	25		CU NIPDAU	N / A for Pkg Type
SN74HC151NSRE4 ACTIVE SO	SN74HC151NE4	ACTIVE	PDIP	N	16	25		CU NIPDAU	N / A for Pkg Type
SN74HC151PW	SN74HC151NSR	ACTIVE	SO	NS	16	2000	,	CU NIPDAU	Level-1-260C-UNLIM
SN74HC151PWE4 ACTIVE TSSOP PW 16 90 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/Br)	SN74HC151NSRE4	ACTIVE	SO	NS	16	2000		CU NIPDAU	Level-1-260C-UNLIM
SN74HC151PWR	SN74HC151PW	ACTIVE	TSSOP	PW	16	90	,	CU NIPDAU	Level-1-260C-UNLIM
N74HC151PWRE4 ACTIVE TSSOP PW 16 2000 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/Br)	SN74HC151PWE4	ACTIVE	TSSOP	PW	16	90	,	CU NIPDAU	Level-1-260C-UNLIM
no Sb/Br) SN74HC151PWT ACTIVE TSSOP PW 16 250 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/Br) SN74HC151PWTE4 ACTIVE TSSOP PW 16 250 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM CONTINUE)	SN74HC151PWR	ACTIVE	TSSOP	PW	16	2000	,	CU NIPDAU	Level-1-260C-UNLIM
no Sb/Br) SN74HC151PWTE4 ACTIVE TSSOP PW 16 250 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM	SN74HC151PWRE4	ACTIVE	TSSOP	PW	16	2000	`	CU NIPDAU	Level-1-260C-UNLIM
	SN74HC151PWT	ACTIVE	TSSOP	PW	16	250	,	CU NIPDAU	Level-1-260C-UNLIM
no SD/Br)	SN74HC151PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC151FK ACTIVE LCCC FK 20 1 TBD POST-PLATE N / A for Pkg Type	SNJ54HC151FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC151J ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type	SNJ54HC151J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

12-Sep-2006

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

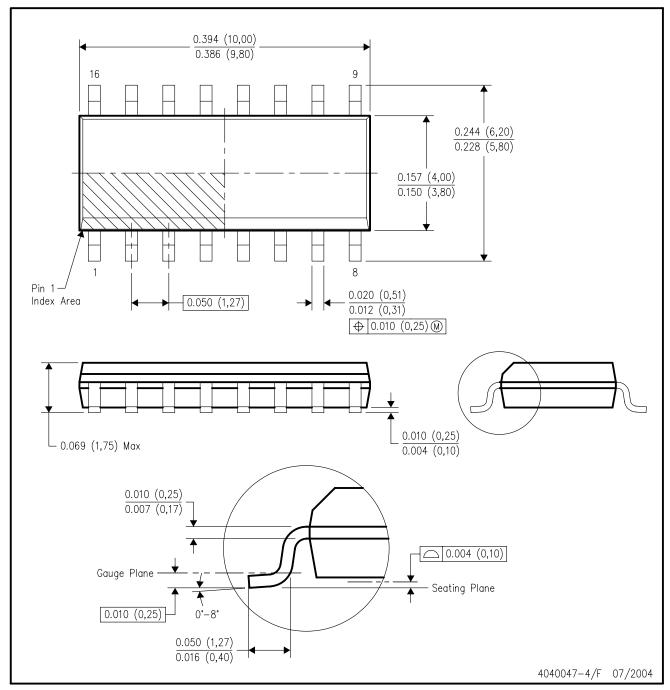


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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